

TOSHIBA PHOTOCOUPLER GaAlAs IRED & PHOTO IC

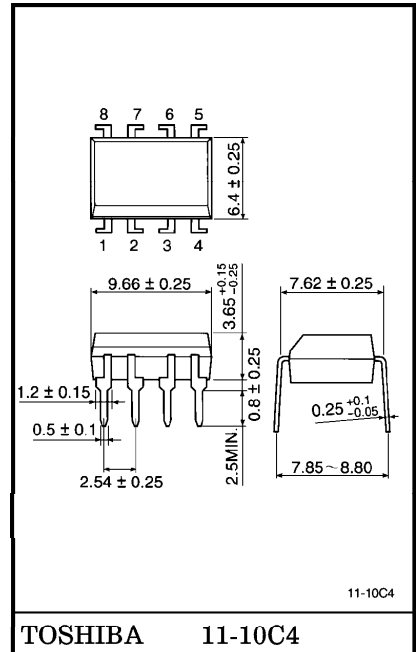
TLP2530, TLP2531

DEGITAL LOGIC ISOLATION
 LINE RECEIVER
 POWER SUPPLY CONTROL
 SWITCHING POWER SUPPLY
 TRANSISTOR INVERTER

Unit in mm

The TOSHIBA TLP2530 and TLP2531 dual photocouplers consist of a pair of GaAlAs light emitting diode and integrated photodetector. This unit is 8-lead DIP.

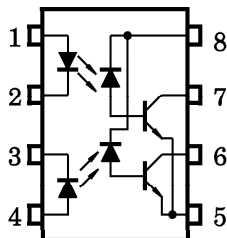
Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.



Weight : 0.54g

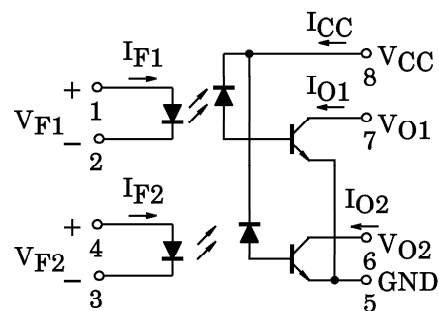
- TTL Compatibel
- Switching Speed : $t_{pHL} = 0.3 \mu s$, $t_{pLH} = 0.3 \mu s$ (Typ.)
 (@ $R_L = 1.9 k\Omega$)
- Guaranteed Performance Over Temp : 0~70°C
- Isolation Voltage : 2500Vrms (Min.)
- UL Recognized : UL1577, File No. E67349

PIN CONFIGURATION (TOP VIEW)



- 1. : ANODE.1
- 2. : CATHODE.1
- 3. : CATHODE.2
- 4. : ANODE.2
- 5. : GND
- 6. : V_{O2} (OUTPUT 2)
- 7. : V_{O1} (OUTPUT 1)
- 8. : V_{CC}

SCHEMATIC



980508EBC2

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● Gallium arsenide (GaAs) is a substance used in the products described in this document. GaAs dust and fumes are toxic. Do not break, cut or pulverize the product, or use chemicals to dissolve them. When disposing of the products, follow the appropriate regulations. Do not dispose of the products with other industrial waste or with domestic garbage.

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● The information contained herein is subject to change without notice.

MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Each channel) (Note 1)	I_F	25	mA
	Pulse Forward Current (Each channel) (Note 2)	I_{FP}	50	mA
	Total Pulse Forward Current (Each channel) (Note 3)	I_{FPT}	1	A
	Reverse Voltage (Each channel)	V_R	5	V
	Diode Power Dissipation (Each channel) (Note 4)	P_D	45	mW
DETECTOR	Output Current (Each channel)	I_O	8	mA
	Peak Output Current (Each channel)	I_{OP}	16	mA
	Supply Voltage	V_{CC}	-0.5~15	V
	Output Voltage (Each channel)	V_O	-0.5~15	V
	Output Power Dissipation (Each channel) (Note 5)	P_O	35	mW
Operating Temperature Range		T_{opr}	-55~100	°C
Storage Temperature Range		T_{stg}	-55~125	°C
Lead Solder Temperature (10s)**		T_{sol}	260	°C
Isolation Voltage (AC, 1min., R.H. ≤ 60%) (Note 7)		BVS	2500	V _{rms}

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width. Derate 1.6mA/°C above 70°C.

(Note 3) Pulse width 1μs, 300pps.

(Note 4) Derate 0.9mW/°C above 70°C.

(Note 5) Derate 1mW/°C above 70°C.

** 2mm below seating plane.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	0	—	12	V
Forward Current, Each Channel	I_F	—	16	25	mA
Operating Temperature	T_{opr}	-25	—	85	°C

ELECTRICAL CHARACTERISTICS

OVER RECOMMENDED TEMPERATURE (Ta = 0°C~70°C, Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.**	MAX.	UNIT
Current Transfer Ratio (Each Channel)	TLP2530	CTR	I _F = 16mA, V _O = 0.4V V _{CC} = 4.5V, Ta = 25°C (Note 6)	7	30	—	%
	TLP2531			19	30	—	
	TLP2530	CTR	I _F = 16mA, V _O = 0.5V V _{CC} = 4.5V (Note 6)	5	—	—	%
	TLP2531			15	—	—	
Logic Low Output Voltage (Each Channel)	TLP2530	V _{OL}	I _F = 16mA, I _O = 1.1mA V _{CC} = 4.5V	—	0.1	0.4	V
	TLP2531		I _F = 16mA, I _O = 2.4mA V _{CC} = 4.5V	—	0.1	0.4	V
Logic High Output Current (Each Channel)		I _{OH}	I _F = 0mA, V _O = V _{CC} = 5.5V Ta = 25°C	—	3	500	nA
			I _F = 0mA, V _O = V _{CC} = 15V	—	—	50	μA
Logic Low Supply Current		I _{CCL}	I _{F1} = I _{F2} = 16mA V _{O1} = V _{O2} = Open V _{CC} = 15V	—	160	—	μA
Logic High Supply Current		I _{CCH}	I _{F1} = I _{F2} = 0mA V _{O1} = V _{O2} = Open V _{CC} = 15V	—	0.05	4	μA
Input Forward Voltage (Each Channel)		V _F	I _F = 16mA, Ta = 25°C	—	1.65	1.7	V
Temperature Coefficient of Forward Voltage (Each Channel)		ΔV _F / ΔTa	I _F = 16mA	—	-2	—	mV / °C
Input Reverse Breakdown Voltage (Each Channel)		BV _R	I _R = 10 μA, Ta = 25°C	5	—	—	V
Input Capacitance (Each Channel)		C _{IN}	f = 1MHz, V _F = 0	—	60	—	pF
Input-Output Insulation Leakage Current		I _{I-O}	Relative Humidity = 45% t = 5s, V _{I-O} = 3000V _{dc} Ta = 25°C (Note 7)	—	—	1.0	μA
Resistance (Input-Output)		R _{I-O}	V _{I-O} = 500V _{dc} (Note 7)	—	10 ¹²	—	Ω
Capacitance (Input-Output)		C _{I-O}	f = 1MHz (Note 7)	—	0.6	—	pF
Input-Input Leakage Current		I _{I-I}	Relative Humidity = 45% t = 5s, V _{I-I} = 500V (Note 8)	—	0.005	—	μA
Resistance (Input-Input)		R _{I-I}	V _{I-I} = 500V _{dc} (Note 8)	—	10 ¹¹	—	Ω
Capacitance (Input-Input)		C _{I-I}	f = 1MHz (Note 8)	—	0.25	—	pF

** All typicals at Ta = 25°C.

SWITCHING CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, VCC = 5V, IF = 16mA)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Propagation Delay Time to Logic Low at Output (Each Channel)	TLP2530	t _{pHL}	1	R _L = 4.1kΩ	—	0.3	1.5	μs
	TLP2531			R _L = 1.9kΩ	—	0.2	0.8	
Propagation Delay Time to Logic High at Output (Each Channel)	TLP2530	t _{pLH}	1	R _L = 4.1kΩ	—	0.5	1.5	μs
	TLP2531			R _L = 1.9kΩ	—	0.3	0.8	
Common Mode Transient Immunity at Logic High Level Output (Each Channel, Note 9)	TLP2530	CM _H	2	I _F = 0mA, V _{CM} = 400V _{p-p} R _L = 4.1kΩ	—	1500	—	V / μs
	TLP2531			I _F = 0mA, V _{CM} = 400V _{p-p} R _L = 1.9kΩ	—	1500	—	
Common Mode Transient Immunity at Logic Low Level Output (Each Channel, Note 9)	TLP2530	CM _L	2	V _{CM} = 400V _{p-p} R _L = 4.1kΩ, I _F = 16mA	—	-1500	—	V / μs
	TLP2531			V _{CM} = 400 _{p-p} R _L = 1.9kΩ, I _F = 16mA	—	-1500	—	
Bandwidth (Each Channel, Note 10)	BW	3	R _L = 100Ω	—	2	—	MHz	

(Note 6) DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

(Note 7) Device considered a two-terminal device : Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.

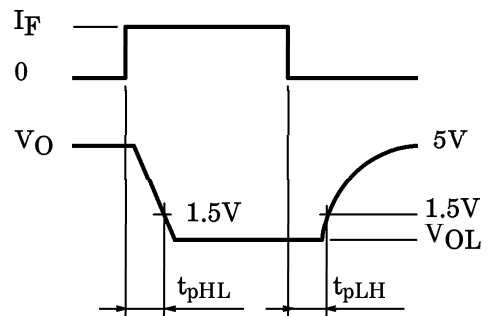
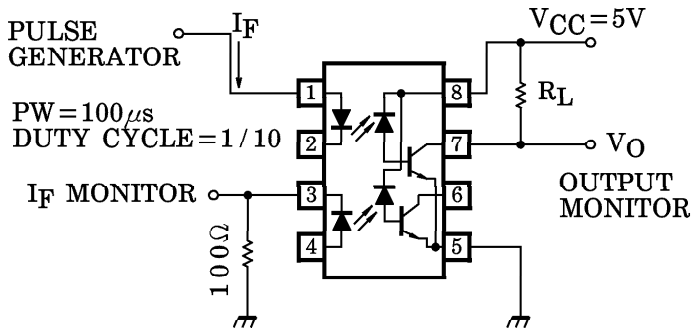
(Note 8) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

(Note 9) Common mode transient immunity in Logic High level is the maximum tolerable (Positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V).

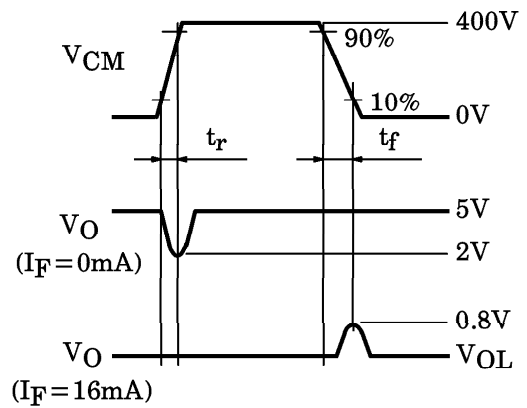
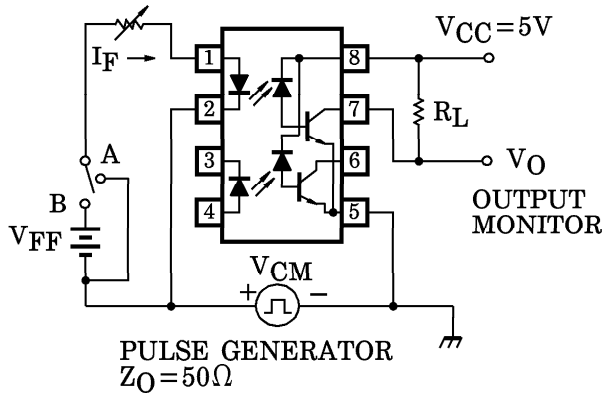
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O > 0.8V).

(Note 10) The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

TEST CIRCUIT 1 : SWITCHING TIME, t_{pHL} , t_{pLH}



TEST CIRCUIT 2 : TRANSIENT IMMUNITY AND TYPICAL WAVEFORM



$$CM_H = \frac{320 (V)}{t_r (\mu s)}, \quad CM_L = \frac{320 (V)}{t_f (\mu s)}$$

TEST CIRCUIT 3 : FREQUENCY RESPONSE

