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SEMICONDUCTOR
TECHNICAL DATA

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by MCM6147A/D

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MCM6147A
MCM61L47A

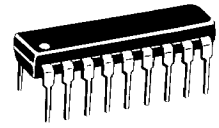
4K Bit Static Random Access Memory

The MCM6147A is a 4096-bit static random access memory organized as 4096 words by 1-bit, fabricated using Motorola's high performance CMOS silicon gate technology (HCMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock, but rather a chip control that affects power consumption. After $\overline{E}$ goes high, initiating deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high.

The MCM6147A is in an 18-pin dual in-line package with the industry standard pin out. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Single +5 V Supply
- Fully Static Memory—No Clock or Timing Strobe Required
- Maximum Access Time
  - MCM6147A-55 and MCM61L47A-55 = 55 ns
  - MCM6147A-70 and MCM61L47A-70 = 70 ns
- Automatic Power Down
- Low Power Supply Current Drain
  - 35 mA Maximum (Active)
  - 12 mA Maximum (Standby—TTL Levels)
  - 800 μA Maximum (Standby—Full Rail, MCM6147A)
  - 100 μA Maximum (Standby—Full Rail, MCM61L47A)
- Low Standby Power Version Available—MCM61L47A
- Directly TTL Compatible—All Inputs and Output
- Separate Data Input and Three-State Output
- Equal Access and Cycle Time
- High Density 18-Pin Package
- Improved ESD Protection



P PACKAGE
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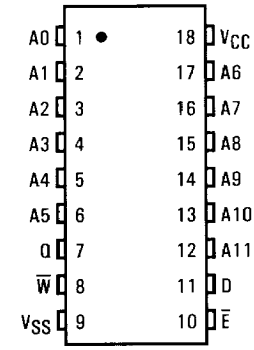
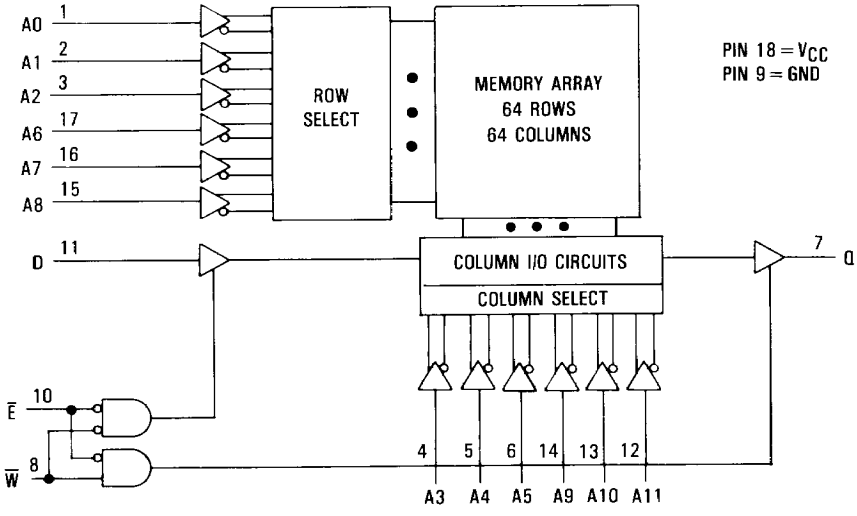
PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
$\overline{W}$	Write
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



MOTOROLA

DS9874R1

ABSOLUTE MAXIMUM RATING (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +85	°C
Voltage on Any Pin with Respect to V_{CC}	−0.5 to +7.0	V
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Input High Voltage, All Inputs	V_{IH}	2.0	—	6.0	V
Input Low Voltage, All Inputs	V_{IL}	−0.3	—	0.8	V

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ*	Max	Unit
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)		I_{IL}	—	0.01	1.0	μA
Output Leakage Current ($\overline{E}$ = 2.0 V, V_{out} = 0 to 5.5 V)		I_{OL}	—	0.1	1.0	μA
Power Supply Current ($\overline{E} = V_{IL}$, Output Open)		I_{CC}	—	15	35	mA
Standby Current ($\overline{E} = V_{IH}$)		I_{SB}	—	5	12	mA
Standby Current ($\overline{E} = V_{CC} - 0.2$ V, 0.2 V ≥ V_{in} ≥ $V_{CC} - 0.2$ V)	MCM6147A MCM61L47A	I_{SB1}	— —	200 25	800 100	μA
Input Low Voltage		V_{IL}	−0.3	—	0.8	V
Input High Voltage		V_{IH}	2.0	—	6.0	V
Output Low Voltage (I_{OL} = 12.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage** (I_{OH} = −8.0 mA)		V_{OH}	2.4	—	—	V

*Typical values are for T_A = 25°C and V_{CC} = 5.0 V.

**Output voltages are compatible with Motorola's High-Speed CMOS Logic Family if the same power supply voltage is used.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	7.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

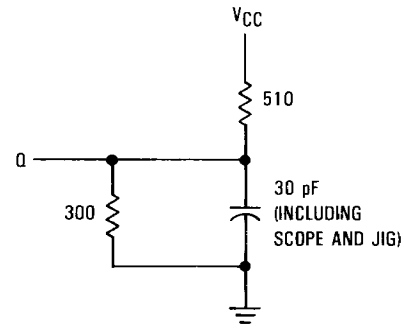


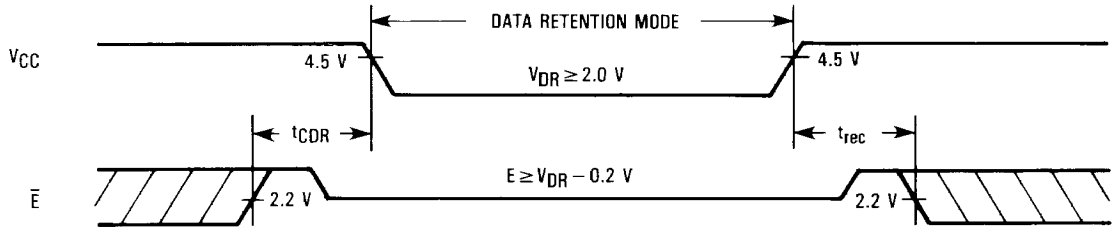
Figure 1. Output Load

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L47A Only)

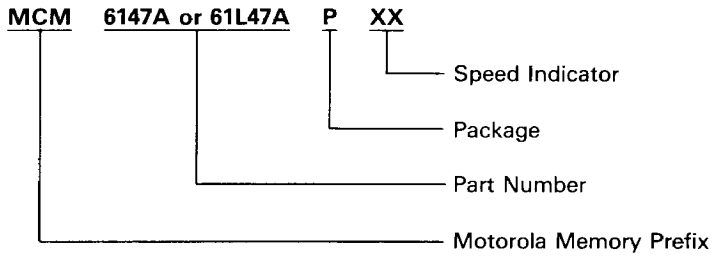
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2V$ $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V	V_{DR}	2.0	—	—	V
Data Retention Current	V_{CC} = 3.0 V, $\overline{E} \geq 2.8$ V $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V	I_{CCDR}	—	—	40	μA
Chip Disable to Data Retention Time	See Retention Waveform	t_{CDR}	0	—	—	ns
Operation Recovery Time		t_{rec}	*t_{AVAX}	—	—	ns

*t_{AVAX} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM

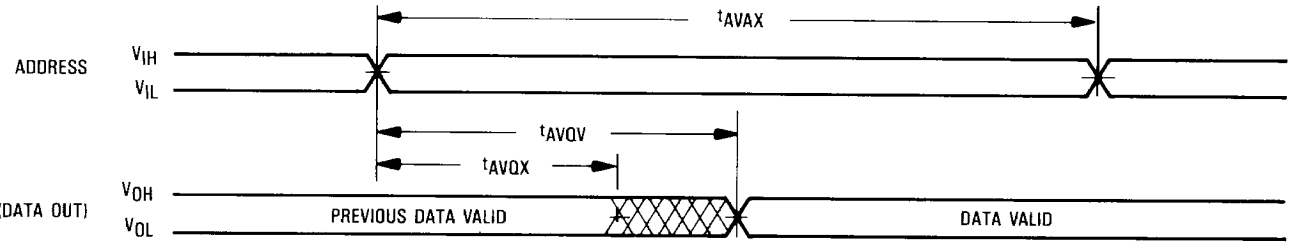


ORDERING INFORMATION
(Order by Full Part Number)

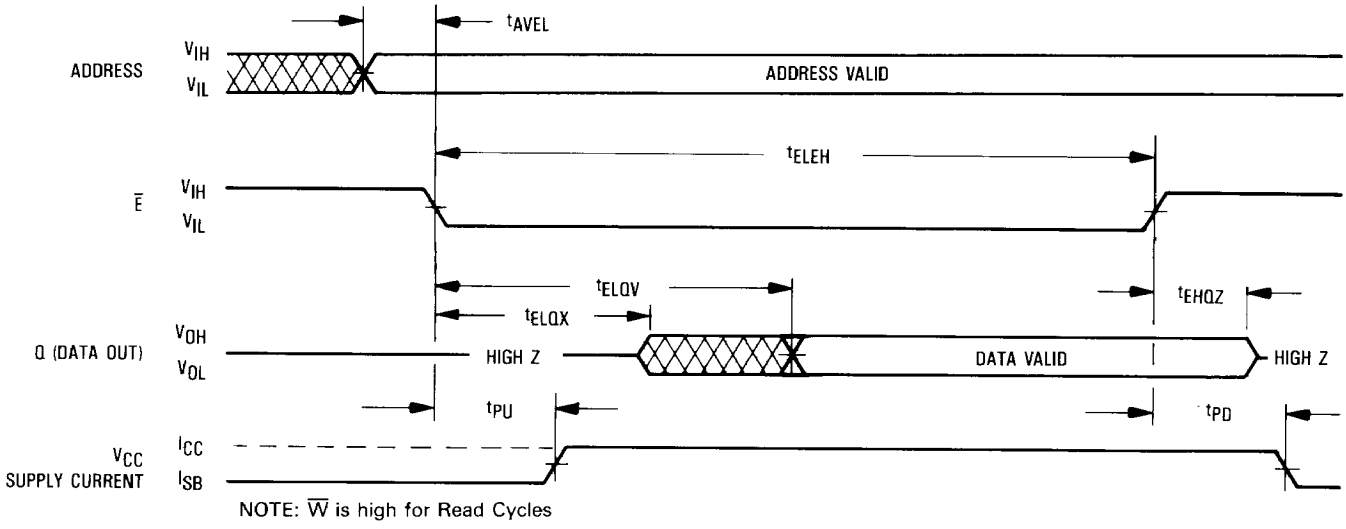


Full Part Numbers— MCM6147AP55
MCM61L47AP55
MCM6147AP70
MCM61L47AP70

READ CYCLE TIMING 1
($\overline{E}$ Held Low)

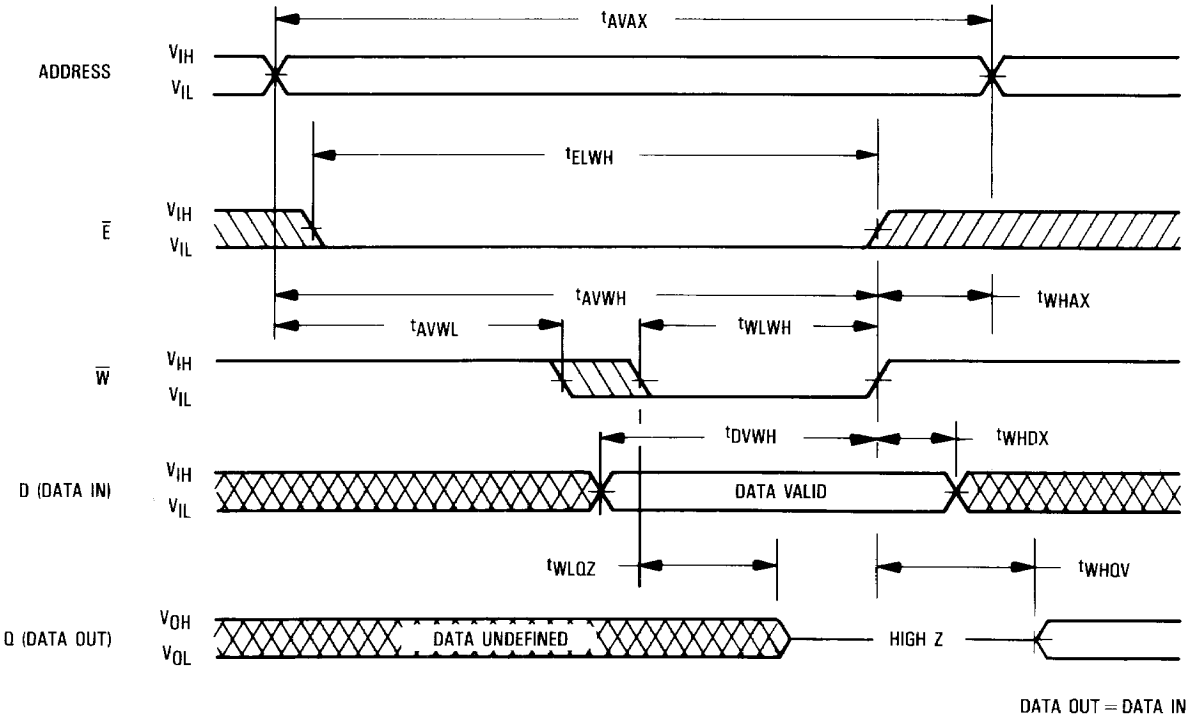


READ CYCLE TIMING 2



NOTE: $\overline{W}$ is high for Read Cycles

WRITE CYCLE TIMING



DATA OUT = DATA IN

AC OPERATING CONDITIONS AND CHARACTERISTICS

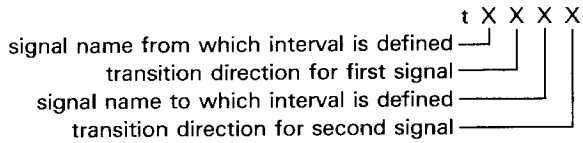
(Full Operating Voltage and Temperature Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 Volt to 3.5 Volts
Input Rise and Fall Times . . . . . 10 ns
Input and Output Timing Reference Levels . . . . . 1.5 Volts
Output Load . . . . . See Figure 1

READ, WRITE CYCLES

Parameter	Symbol	MCM6147A-55 MCM61L47A-55		MCM6147A-70 MCM61L47A-70		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	55	—	70	—	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	—	70	—	ns
Address Valid to Output Valid (Access)	t_{AVQV}	—	55	—	70	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	—	55	—	70	ns
Address Valid to Output Invalid	t_{AVQX}	5	—	5	—	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	—	10	—	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	—	0	—	ns
Chip Enable Low to Write High	t_{ELWH}	45	—	55	—	ns
Address Valid to Write High	t_{AVWH}	45	—	55	—	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	—	0	—	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	—	40	—	ns
Write High to Address Don't Care	t_{WHAX}	10	—	15	—	ns
Data Valid to Write High	t_{DVWH}	25	—	30	—	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	—	10	—	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	ns
Write High to Output Valid	t_{WHQV}	0	—	0	—	ns

TIMING PARAMETER ABBREVIATIONS



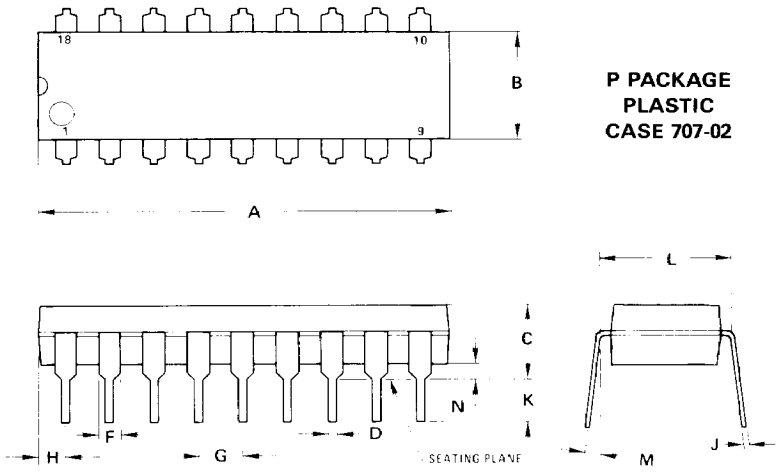
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

PACKAGE DIMENSIONS



P PACKAGE
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NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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