CY2276A-12
CY2276A-13

Pentium®II Clock Synthesizer/Driver for Desktop PCs with Intel 82440LX and 4 DIMMs

Features

- **Mixed 2.5V and 3.3V operation**
- **Complete clock solution to meet requirements of Pentium® and Pentium® II motherboards**
  - **— Five CPU clocks at 2.5V**
  - **— Sixteen 3.3V SDRAM clocks**
  - **— Seven synchronous PCI clocks, one free-running**
  - **— Three 2.5V IOAPIC clocks at 14.318 MHz**
  - **— One 3.3V Ref. clock at 14.318 MHz**
- **1 ns–6 ns CPU-PCI delay (-12 option)**
- **1 ns–4.8 ns CPU-PCI delay (-13 option)**
- **I^2C™ Serial Configuration Interface**
- **Dedicated OE input**
- **Factory-EPROM programmable output drive and slew rate for EMI customization**
- **Factory-EPROM programmable CPU clock frequencies for custom configurations**
- **High drive, low skew, and low jitter outputs**
- **Intel® Test Mode support**
- **Available in space-saving 56-pin SSOP package**

Functional Description

The CY2276A-12 and CY2276A-13 are Clock Synthesizer/Drivers for Pentium or Pentium II-based PCs designed with an Intel 82440LX or similar core-logic chipset.

The CY2276A-12 and CY2276A-13 output five CPU clocks at 2.5V. There are seven PCI clocks, at one half the CPU clock frequency, one of which is free-running. Additionally, the parts drive out sixteen 3.3V SDRAM clocks at the CPU clock frequency, three 2.5V IOAPIC clocks at 14.318 MHz, and one 3.3V reference clock at 14.318 MHz.

The CY2276A-12 and CY2276A-13 can be used with a peripheral clock generator (CY2030) which can generate USB, I/O, reference, and Audio clocks, thus providing a complete solution for motherboard manufacturers.

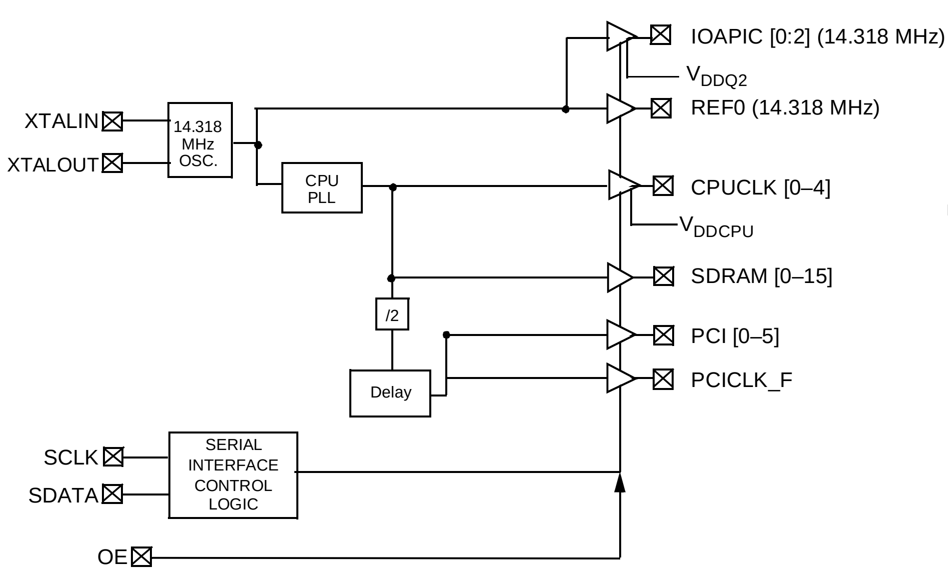
The CY2276A-12 and CY2276A-13 outputs are designed for low EMI emission. Controlled rise and fall times, unique output driver circuits and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

CY2276A Selector Guide

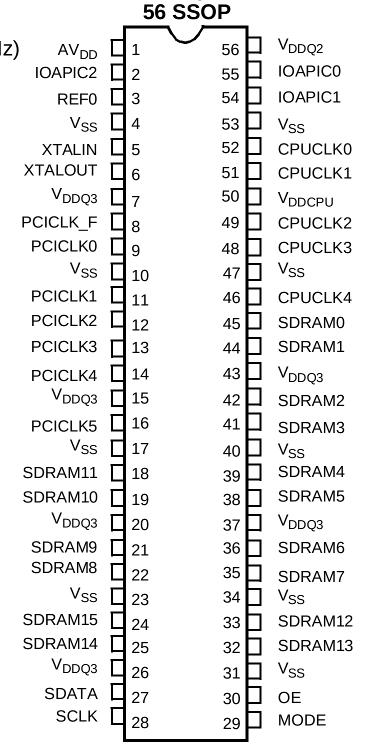
Clocks Outputs	-12	-13
CPU@2.5V (66.6 MHz)	5	5
SDRAM	16	15
PCI (33.3 MHz)	7[1]	7[1]
IOAPIC (14.318 MHz)	3	3
Ref (14.318MHz)	1	1
CPU-PCI delay	1–6 ns	1–4.8 ns

Note:
1. One free-running PCI clock.

Logic Block Diagram



Pin Configuration



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Pin Summary

Name	Pins	Description
V_{DDQ3}	7, 15, 20, 26, 37, 43	3.3V Digital voltage supply
V_{DDQ2}	56	IOAPIC Digital voltage supply, 2.5V
V_{DDCPU}	50	CPU Digital voltage supply, 2.5V
AV_{DD}	1	Analog voltage supply, 3.3V
V_{SS}	4, 10, 17, 23, 31, 34, 40, 47, 53	Ground
XTALIN[2]	5	Reference crystal input
XTALOUT[2]	6	Reference crystal feedback
SDRAM[0–15]	45, 44, 42, 41, 39, 38, 36, 35, 22, 21, 19, 18, 33, 32, 25, 24	SDRAM clock outputs
OE	30	Active HIGH Output Enable (see table below)
CPUCLK[0–4]	52, 51, 49, 48, 46	CPU clock outputs
PCICLK[0–5]	9, 11, 12, 13, 14, 16	PCI clock outputs, running at one-half the CPU frequency
PCICLK_F	8	Free-running PCI clock output
IOAPIC[0–2]	55, 54, 2	IOAPIC clock outputs
REF0	3	Reference clock outputs, 14.318 MHz, drives 45 pF load
SDATA	27	Serial data input for serial configuration port
SCLK	28	Serial clock input for serial configuration port
MODE	29	Mode input, not used on this configuration, tie to V_{SS}

Note:
2. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Function Table

OE	XTALIN	CPUCLK[0–4] SDRAM[0–15]	PCICLK[0–5] PCICLK_F	REF0 IOAPIC[0–2]
0	14.318 MHz	Hi-Z	Hi-Z	Hi-Z
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to “0”.
- I^2C Address for the CY2276A-12 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)

Bit	Pin #	Description	
Bit 7	--	(Reserved) drive to ‘0’	
Bit 6	--	(Reserved) drive to ‘0’	
Bit 5	--	(Reserved) drive to ‘0’	
Bit 4	--	(Reserved) drive to ‘0’	
Bit 3	--	(Reserved) drive to ‘0’	
Bit 2	--	(Reserved) drive to ‘0’	
Bit 1 Bit 0	--	Bit 1 1 1 0 0	Bit 0 1 - N/A 0 - N/A 1 - Testmode 0 - Normal Operation

Select Functions

Functional Description	Outputs				
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC
Test Mode	TCLK/2[3]	TCLK/4	TCLK/2	TCLK	TCLK

Note:

3. TCLK supplied on the XTALIN pin in Test Mode.

Byte 1: CPU Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	(Reserved) drive to ‘0’
Bit 6	N/A	(Reserved) drive to ‘0’
Bit 5	N/A	(Reserved) drive to ‘0’
Bit 4	46	CPUCLK4 (Active/Inactive)
Bit 3	48	CPUCLK3 (Active/Inactive)
Bit 2	49	CPUCLK2 (Active/Inactive)
Bit 1	51	CPUCLK1 (Active/Inactive)
Bit 0	52	CPUCLK0 (Active/Inactive)

Byte 2: PCI Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to ‘0’
Bit 6	8	PCICLK_F (Active/Inactive)
Bit 5	16	PCICLK5 (Active/Inactive)
Bit 4	14	PCICLK4 (Active/Inactive)
Bit 3	13	PCICLK3 (Active/Inactive)
Bit 2	12	PCICLK2 (Active/Inactive)
Bit 1	11	PCICLK1 (Active/Inactive)
Bit 0	9	PCICLK0 (Active/Inactive)

Byte 3: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	35	SDRAM7 (Active/Inactive)
Bit 6	36	SDRAM6 (Active/Inactive)
Bit 5	38	SDRAM5 (Active/Inactive)
Bit 4	39	SDRAM4 (Active/Inactive)
Bit 3	41	SDRAM3 (Active/Inactive)
Bit 2	42	SDRAM2 (Active/Inactive)
Bit 1	44	SDRAM1 (Active/Inactive)
Bit 0	45	SDRAM0 (Active/Inactive)

Byte 4: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	24	SDRAM15 (Active/Inactive)
Bit 6	25	SDRAM14 (Active/Inactive)
Bit 5	32	SDRAM13 (Active/Inactive)
Bit 4	33	SDRAM12 (Active/Inactive)
Bit 3	18	SDRAM11 (Active/Inactive)
Bit 2	19	SDRAM10 (Active/Inactive)
Bit 1	21	SDRAM9 (Active/Inactive)
Bit 0	22	SDRAM8 (Active/Inactive)

Byte 5: Peripheral Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	(Reserved) drive to ‘0’
Bit 6	2	IOAPIC2 (Active/Inactive)
Bit 5	54	IOAPIC1 (Active/Inactive)
Bit 4	55	IOAPIC0 (Active/Inactive)
Bit 3	N/A	(Reserved) drive to ‘0’
Bit 2	N/A	(Reserved) drive to ‘0’
Bit 1	N/A	(Reserved) drive to ‘0’
Bit 0	3	REF0 (Active/Inactive)

Byte 6: Reserved, for future use

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ....–0.5 to +7.0V

Input Voltage ....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ....>2000V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDQ3}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.9	V
V_{DDQ2}	IOAPIC Supply Voltage	2.375	2.9	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK, IOAPIC[0:2] PCICLK, SDRAM REF0	 10 30, 20 20	 20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{ILiic}	Low-level Input Voltage	I^2C inputs only				0.7	V
V_{OH}	High-level Output Voltage[5]	V_{DDCPU} = 2.375V, V_{DDQ2} = 2.375V	I_{OH} = 16 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	IOAPIC			
V_{OL}	Low-level Output Voltage[5]	V_{DDCPU} = 2.375V, V_{DDQ2} = 2.375V	I_{OL} = 27 mA	CPUCLK		0.4	V
			I_{OL} = 29 mA	IOAPIC			
V_{OH}	High-level Output Voltage[5]	V_{DDQ3}, AV_{DD} = 3.135V	I_{OH} = 36 mA	SDRAM	2.4		V
			I_{OH} = 32 mA	PCICLK			
			I_{OH} = 36 mA	REF0			
V_{OL}	Low-level Output Voltage[5]	V_{DDQ3}, AV_{DD} = 3.135V	I_{OL} = 29 mA	SDRAM		0.4	V
			I_{OL} = 26 mA	PCICLK			
			I_{OL} = 29 mA	REF0			
I_{IH}	Input High Current	$V_{IH} = V_{DD}$			–10	+10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				10	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current[5, 6]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				310	mA
I_{DD}	Power Supply Current[5, 6]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				120	mA

Notes:

4. Electrical parameters are guaranteed with these operating conditions.
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.
6. Power supply current will vary with number of outputs which are running.

Switching Characteristics[5,7] Over the Operating Range

Parameter	Output	Description	Test Conditions		Min.	Typ.	Max.	Unit
t_1	CPU, APIC, SDRAM, REF0	Output Duty Cycle[8]	$t_1 = t_{1A} \div t_{1B}$		45	50	55	%
t_1	PCI	Output Duty Cycle[8]	$t_1 = t_{1A} \div t_{1B}$		40	50	55	%
t_{1C}	CPUCLK	CPU Clock HIGH Time	Above 2.0V, 66.6 MHz, V_{DDCPU} = 2.5V		5.2			ns
t_{1C}	PCICLK	PCI Clock HIGH Time	Above 2.4V, 33.3 MHz		11.0			ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Below 0.4V, 66.6 MHz, V_{DDCPU} = 2.5V		5.0			ns
t_{1D}	PCICLK	PCI Clock LOW Time	Below 0.4V, 33.3 MHz		12.0			ns
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.7V and 1.7V, V_{DDCPU} = 2.5V		1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.8V and 2.0V		1.0		4.0	V/ns
t_2	REF0	REF Clock Rising and Falling Edge Rate	Between 0.8V and 2.0V		0.8		4.0	V/ns
t_2	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.8V and 2.0V		0.8		4.0	V/ns
t_2	IOAPIC	IOAPIC Clock Rising and Falling Edge Rate	Between 0.7V and 1.7V, V_{DDQ2} = 2.5V		0.8		4.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.7V and 1.7V, V_{DDCPU} = 2.5V		0.25		1.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 1.7V and 0.7V, V_{DDCPU} = 2.5V		0.25		1.0	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V_{DDCPU} = 2.5V			100	275	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	-12 option	1.0	3.0	6.0	ns
				-13 option	1.0		4.8	ns
t_7	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks				700	ps
t_8	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks				250	ps
t_8	SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.5V for 3.3V clocks				400	ps
t_8	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V				500	ps
t_9	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabilization from power-up				3	ms

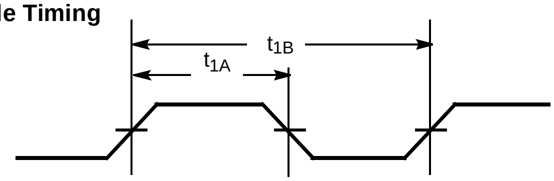
Notes:
7. All parameters specified with loaded outputs.
8. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DDCPU} = 2.5V, CPUCLK duty cycle is measured at 1.25V.

Timing Requirement for the I^{2}C Bus

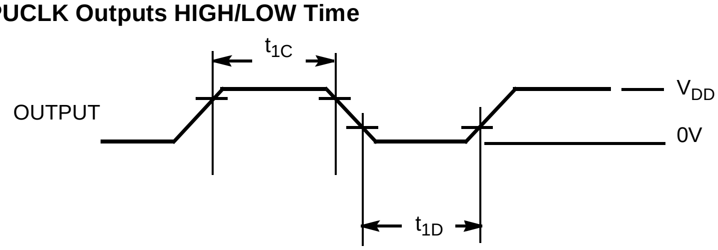
Parameter	Description	Min.	Max.	Unit
t_{10}	SCLK Clock Frequency	0	100	kHz
t_{11}	Time the bus must be free before a new transmission can start	4.7		µs
t_{12}	Hold time start condition. After this period the first clock pulse is generated.	4		µs
t_{13}	The LOW period of the clock.	4.7		µs
t_{14}	The HIGH period of the clock.	4		µs
t_{15}	Setup time for start condition. (Only relevant for a repeated start condition.)	4.7		µs
t_{16}	Hold time DATA for CBUS compatible masters. for I^{2}C devices	 5 0		µs
t_{17}	DATA input set-up time	250		ns
t_{18}	Rise time of both SDATA and SCLK inputs		1	µs
t_{19}	Fall time of both SDATA and SCLK inputs		300	ns
t_{20}	Set-Up time for stop condition	4.0		µs

Switching Waveforms

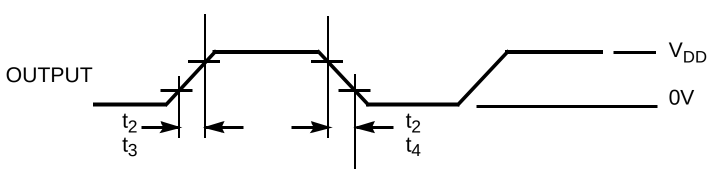
Duty Cycle Timing



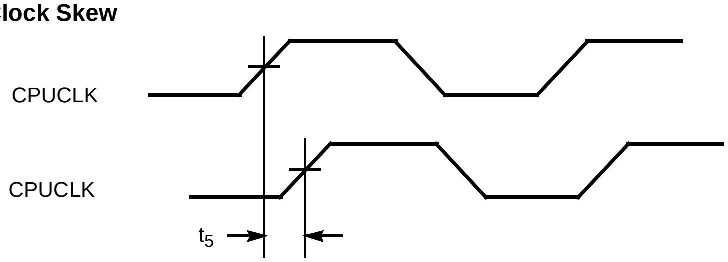
CPUCLK Outputs HIGH/LOW Time



All Outputs Rise/Fall Time

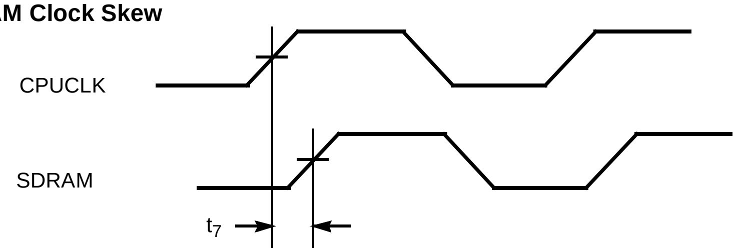


CPU-CPU Clock Skew

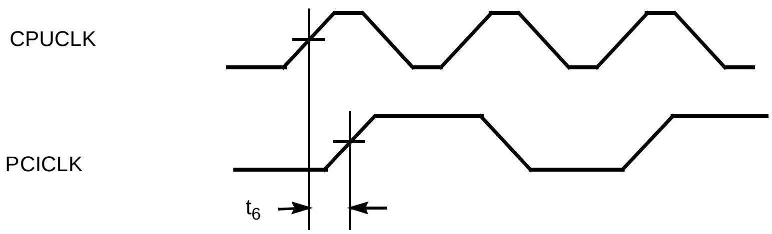


Switching Waveforms (continued)

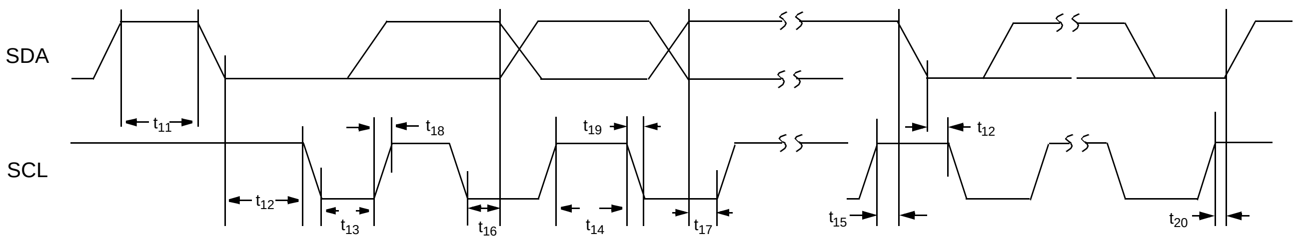
CPU-SDRAM Clock Skew



CPU-PCI Clock Skew



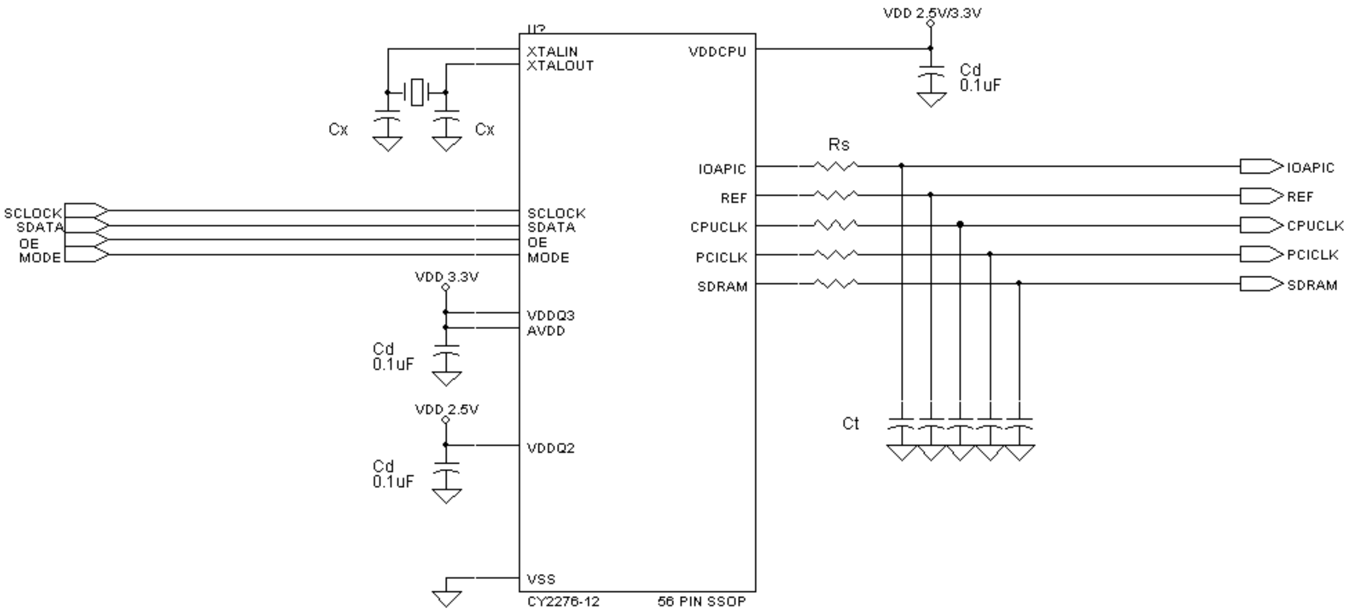
Timing Requirements for the I^2C Bus



Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



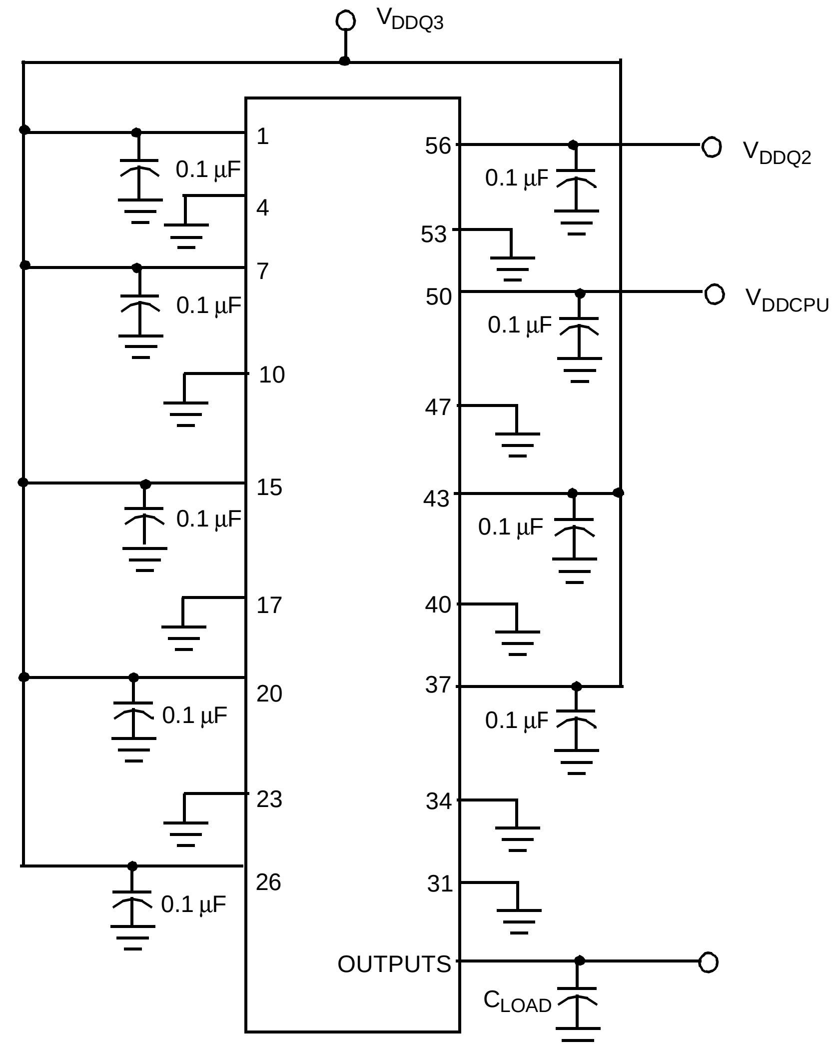
Cd = DECOUPLING CAPACITORS
Ct = OPTIONAL EMI-REDUCING CAPACITORS
Cx = OPTIONAL LOAD MATCHING CAPACITOR
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All Capacitors must be placed as close to the pins as is physically possible

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2276APVC-12	O56	56-Pin SSOP	Commercial
CY2276APVC-13	O56	56-Pin SSOP	Commercial

Document #: 38–00614–D

Package Diagram

56-Lead Shrunk Small Outline Package O56