

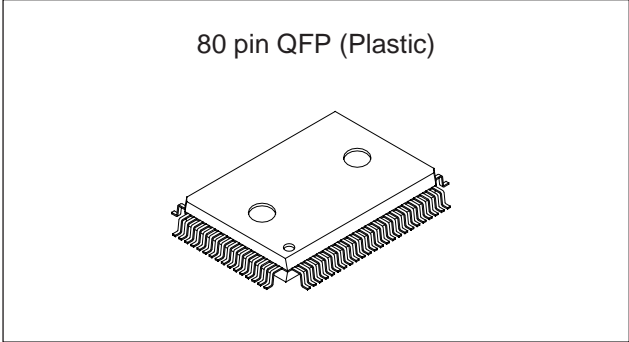
CMOS 8-bit Single Chip Microcomputer

Description

The CXP845F60 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, PWM output and the like besides the basic configurations of 8-bit CPU, flash EEPROM, RAM and I/O port.

The CXP845F60 also provides a sleep/stop functions that enable to execute the power-on reset function or lower the power consumption.

The CXP845F60 is the flash EEPROM-incorporated version of the CXP84540/84548 with a built-in mask ROM. This enables program writing and erasing. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



Features

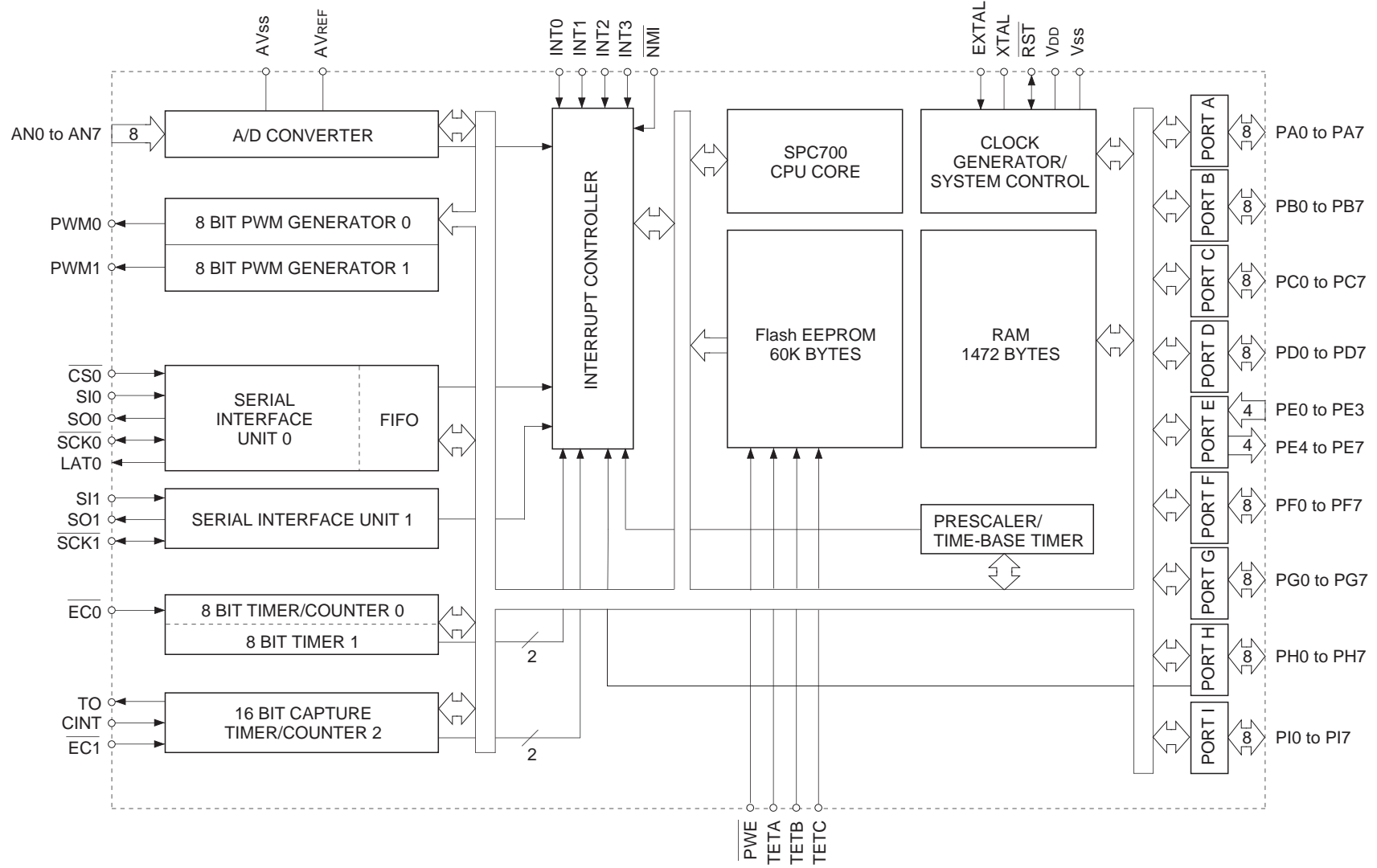
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 143ns at 28MHz operation (4.5 to 5.5V)
- Incorporated flash EEPROM 60K bytes
 - Rewrite time 100 times
- Incorporated RAM 1472 bytes
- Peripheral functions
 - A/D converter 8 bits, 8 channels, successive approximation method
(Conversion time of 1.93µs at 28MHz)
 - Serial interface Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes,
latch output function, MSB/LSB first selectable), 1 channel
 - Timer 8-bit clock sync type, 1 channel
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time-base timer
 - 16-bit capture time/counter
 - PWM output 8 bits, 2 channels
- Interruption 14 factors, 14 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 80-pin plastic QFP

Structure

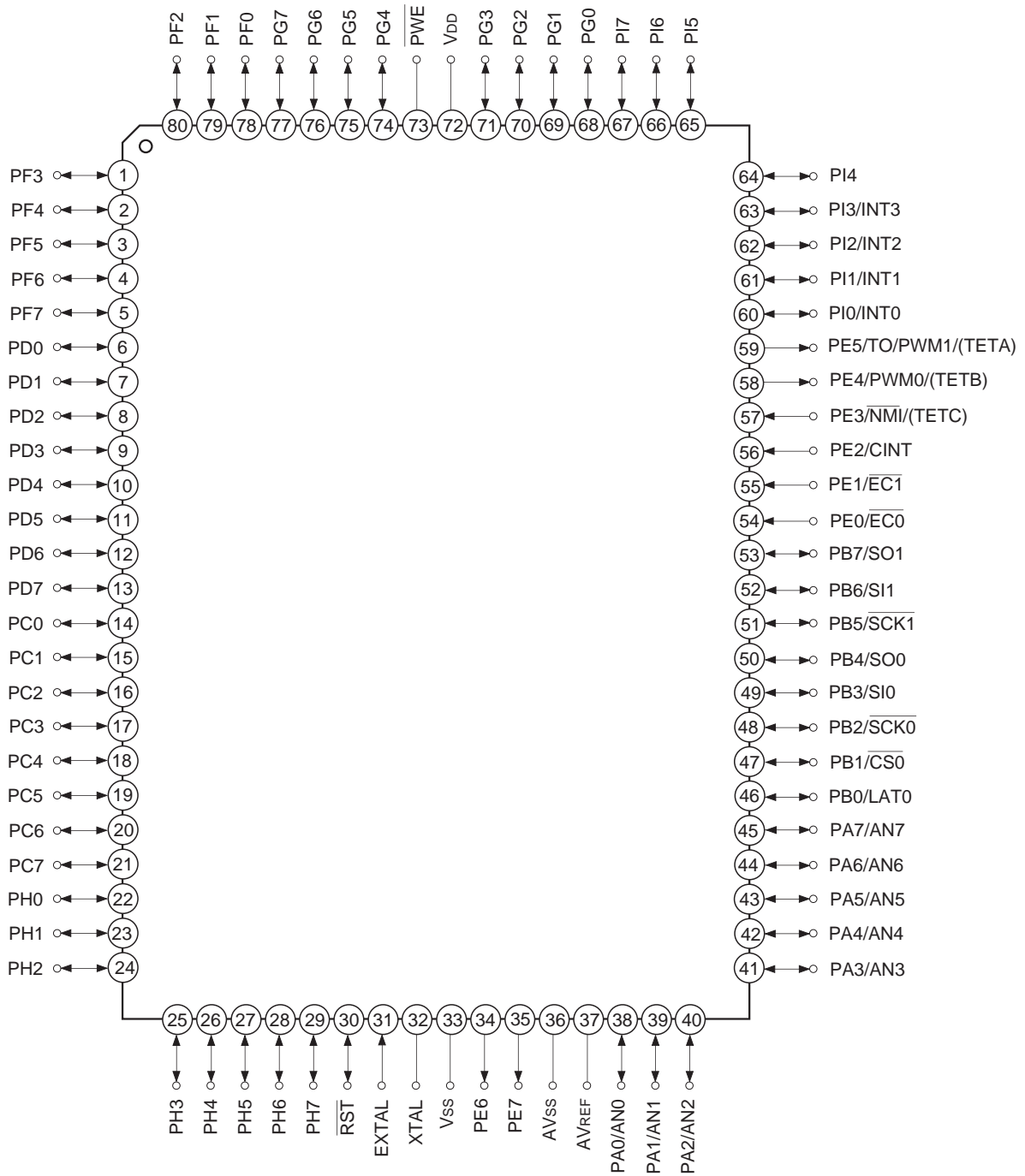
Silicon gate CMOS IC

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Block Diagram



Pin Assignment 1 (Top View)



- Notes)** 1. $\overline{\text{PWE}}$ (Pin 73) is left open during normal operation.
 2. See the Appendix concerning the Pins 57 to 59 (TETA, TETB and TETC).

Pin Description

Symbol	I/O	Description		
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/LAT0	I/O/Output	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Latch output for serial interface (CH0).	
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	I/O/Output		Serial data output (CH1).	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		
PE0/ $\overline{\text{EC}}_0$	Input/Input	(Port E) 8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs. (8 pins)	External event inputs for timer/counter. (2 pins)	
PE1/ $\overline{\text{EC}}_1$	Input/Input			
PE2/CINT	Input/Input		Capture trigger input.	
PE3/ $\overline{\text{NMI}}$ / (TETC)	Input/Input/ (Input)		Non-maskable interruption request input.	Control pins for flash EEPROM write. (3 pins)
PE4/PWM0/ (TETB)	Output/Output/ (Input)		8-bit PWM0 output.	
PE5/TO/ PWM1/(TETA)	Output/Output/ Output/(Input)		Rectangular wave output for 16-bit timer/counter and 8-bit PWM1 output.	
PE6	Output			
PE7	Output			
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		

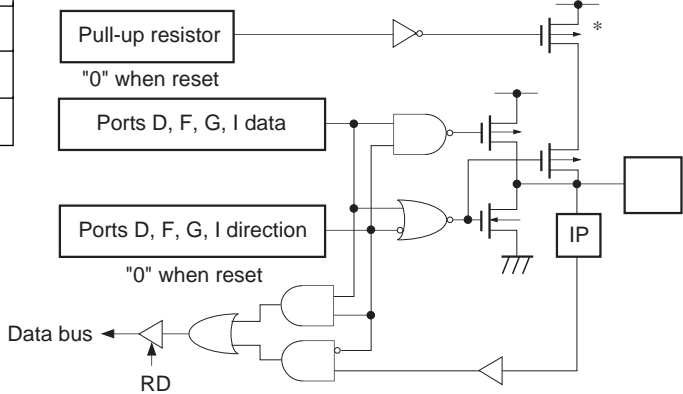
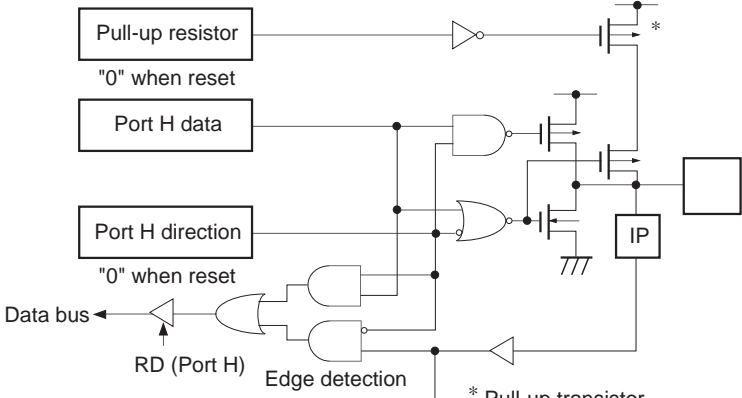
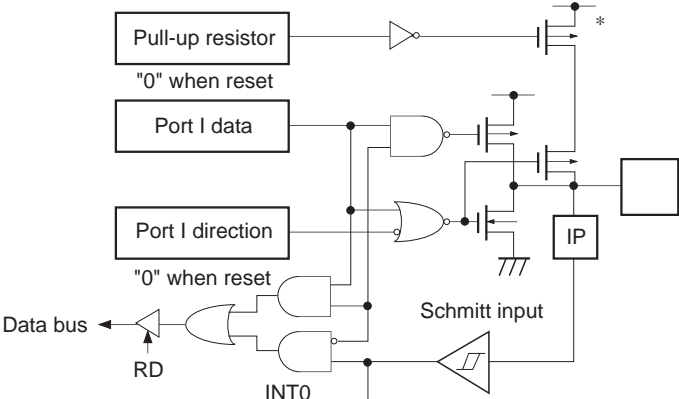
Symbol	I/O	Description	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (4 pins)
PI4 to PI7	I/O		
EXTAL	Input	Connects a crystal for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	System reset for active at Low level. This pin is I/O pin, and outputs Low level at the power on with the power-on reset function executed.	
$\overline{\text{PWE}}$	Input	Flash EEPROM write enable pin. Write is enabled at Low level; write is prohibited at High level. Leave this pin open for normally operation.	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
VDD		Positive power supply.	
Vss		GND	

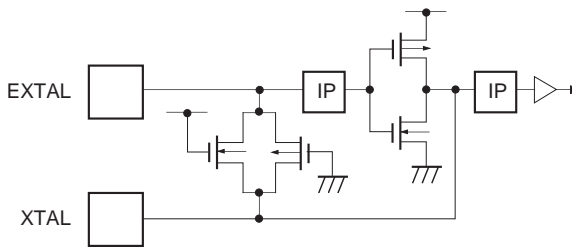
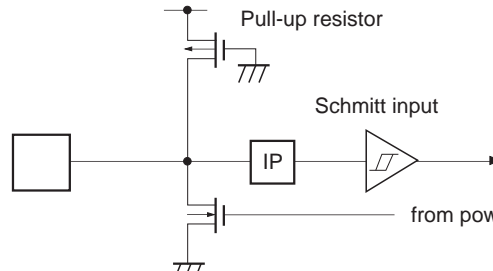
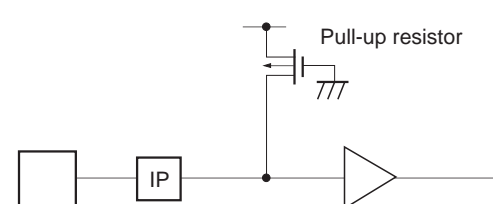
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	<p>Hi-Z</p>
<p>PB0/LAT0</p> <p>1 pin</p>	<p>Port B</p> <p>* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	<p>Hi-Z</p>
<p>PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>3 pins</p>	<p>Port B</p> <p>* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>$\overline{\text{SCK OUT}}$ Serial clock output enable</p> <p>Port B function selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>$\overline{\text{SCK0}}, \overline{\text{SCK1}}$ in</p> <p>* Pull-up transistor Approx. 100kΩ ($V_{DD} = 4.5$ to 5.5V)</p>	<p>Hi-Z</p>
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor</p> <p>SO</p> <p>Serial data output enable</p> <p>Port B function selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>* Pull-up transistor Approx. 100kΩ ($V_{DD} = 4.5$ to 5.5V)</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p> <p>Pull-up resistor "0" when reset</p> <p>Port C data</p> <p>Port C direction "0" when reset</p> <p>Data bus</p> <p>RD (Port C)</p> <p>*1 Large current drive 12mA ($V_{DD} = 4.5$ to 5.5V)</p> <p>*2 Pull-up transistor Approx. 100kΩ ($V_{DD} = 4.5$ to 5.5V)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{EC0}$ PE1/$\overline{EC1}$ PE2/CINT PE3/\overline{NMI}/ (TETC)</p> <p>4 pins</p>	<p>Port E</p> <p>Schmitt input</p> <p>IP</p> <p>$\overline{EC0}$, $\overline{EC1}$ CINT, \overline{NMI} (to flash EEPROM circuit)</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE4/PWM0/ (TETB)</p> <p>1 pin</p>	<p>Port E</p> <p>PWM0</p> <p>Port E function selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus</p> <p>RD (Port E) (to flash EEPROM circuit)</p>	<p>High level</p>
<p>PE5/TO/ PWM1/ (TETA)</p> <p>1 pin</p>	<p>Port E</p> <p>Internal reset signal</p> <p>Port E data "1" when reset</p> <p>TO 01</p> <p>PWM1 1x</p> <p>MPX</p> <p>Port E function selection (upper) Port E function selection (lower) "00" when reset</p> <p>TO output enable</p> <p>(to flash EEPROM circuit)</p> <p>* Pull-up transistor Approx. 150kΩ ($V_{DD} = 4.5$ to 5.5V)</p>	<p>High level High level at ON resistance of pull-up transistor during a reset.</p>
<p>PE6, PE7</p> <p>2 pins</p>	<p>Port E</p> <p>Port E data "0" when reset</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Low level</p>

Pin	Circuit format	When reset
PD0 to PD7 PF0 to PF7 PG0 to PG7 PI4 to PI7 28 pins	<div style="display: flex; flex-direction: column;"> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port D</div> </div> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port F</div> </div> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port G</div> </div> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port I</div> </div> </div>  <p style="text-align: right; font-size: small;">* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	Hi-Z
PH0 to PH7 8 pins	<div style="display: flex; flex-direction: column;"> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port H</div> </div> </div>  <p style="text-align: right; font-size: small;">* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	Hi-Z
PI0/INT0 to PI3/INT3 4 pins	<div style="display: flex; flex-direction: column;"> <div style="display: flex; border-bottom: 1px solid black; margin-bottom: 5px;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">Port I</div> </div> </div>  <p style="text-align: right; font-size: small;">* Pull-up transistor Approx. 100kΩ (V_{DD} = 4.5 to 5.5V)</p>	Hi-Z

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode and XTAL becomes High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p> <p>from power-on reset circuit</p>	<p>Low level</p>
<p>$\overline{\text{PWE}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>to flash EEPROM circuit</p>	<p>High level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
High level output current	I _{OH}	-5	mA	Output (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current outputs (value per pin* ²)
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.*² The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing and sleep modes
		2.0	5.5		Guaranteed data hold range during stop mode
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ¹
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ²
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL* ³
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ¹
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ²
	V _{ILEX}	-0.3	+0.4	V	EXTAL* ³
Operating temperature	T _{opr}	-20	+75	°C	

*¹ Normal input ports (PA, PB0, PB4, PB7, PC, PE0 to PE3, PD, PF to PH, PI4 to PI7)*² \overline{RST} , CINT, $\overline{CS0}$, $\overline{SCK0}$, SCK1, $\overline{EC0}$, $\overline{EC1}$, SI0, SI1, \overline{NMI} , INT0, INT1, INT2, INT3*³ Specifies only during external clock input.

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4 to PE7, PF to PI, RST (only V_{OL})	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE4 to PE7, PF to PI, RST (only V_{OL})	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PC	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		25	μA
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-25	μA
	I_{ILR}	\overline{RST}	$V_{DD} = 5.5V, V_{IL} = 4.0V$	-1.5		-400	μA
	I_{IL}	PA to PD*1 PF to PI*1				-50	μA
			$V_{DD} = 4.5V, V_{IL} = 4.0V$	-2.78			μA
I/O leakage current	I_{IZ}	PA to PD*1 PF to PI*1 PE0 to PE3	$V_{DD} = 5.5V,$ $V_I = 0, 5.5V$			± 10	μA
Supply current *2	I_{DD1}	V_{DD}	For 1/2 frequency dividing mode		38	66	mA
	I_{DD2}		$V_{DD} = 5.5V, 28MHz$ crystal oscillation ($C_1 = C_2 = 1pF$)				
	I_{DDS1}		Sleep mode		2.5	10	mA
	I_{DDS2}		$V_{DD} = 5.5V, 28MHz$ crystal oscillation ($C_1 = C_2 = 1pF$)				
	I_{DDS3}		Stop mode	$V_{DD} = 5.5V, termination of 28MHz$ crystal oscillation			30
Input capacity	C_{IN}	PA to PD, PE0 to PE3, PF to PI, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 For PA to PD and PF to PI pins, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*2 When all output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		28	MHz
System clock input pulse width	tXL, tXH	EXTAL	Fig. 1, Fig. 2 External clock drive	15.6			ns
System clock input rise time, fall time	tCR, tCF	EXTAL	Fig. 1, Fig. 2 External clock drive			100	ns
Event count input clock pulse width	tEH, tEL	$\overline{EC0}$ $\overline{EC1}$	Fig. 3	t _{sys} + 50*1			ns
Event count input clock rise time, fall time	tER, tEF	$\overline{EC0}$ $\overline{EC1}$	Fig. 3			20	ms

*1 t_{sys} indicates the three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

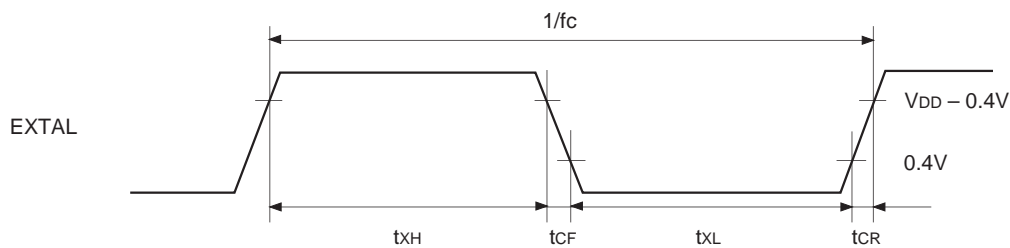


Fig. 1. Clock timing

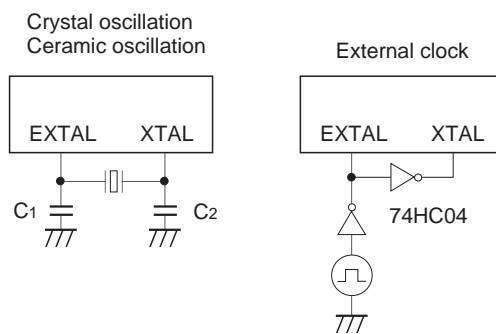


Fig. 2. Clock applied conditions

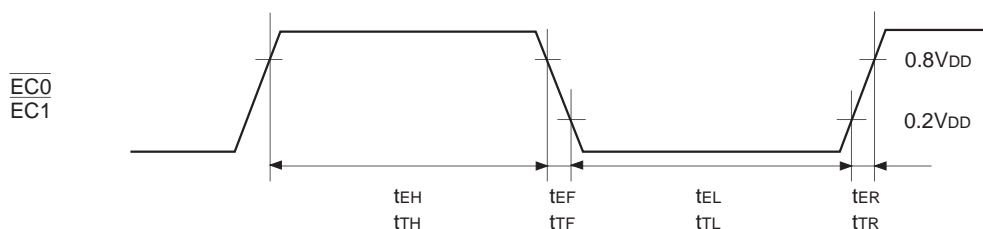


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5t _{sys} + 100	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5t _{sys} + 100	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		1.5t _{sys} + 100	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		1.5t _{sys} + 100	ns
$\overline{CS0}$ High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 150		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK0}$ High, Low level width	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 90		ns
			Output mode	4000/fc - 25		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	50		ns
			$\overline{SCK0}$ output mode	100		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{SI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 100		ns
			$\overline{SCK0}$ output mode	50		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 100	ns
			$\overline{SCK0}$ output mode		50	ns
$\overline{SCK0} \uparrow \rightarrow LAT0$ output delay time	t _{LADLY}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t _{KCY}	t _{KCY} + 50	ns
LAT0 data pulse width	t _{LAPLS}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t _{KCY} - 10	t _{KCY} + 50	ns

Note 1) t_{sys} indicates the three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

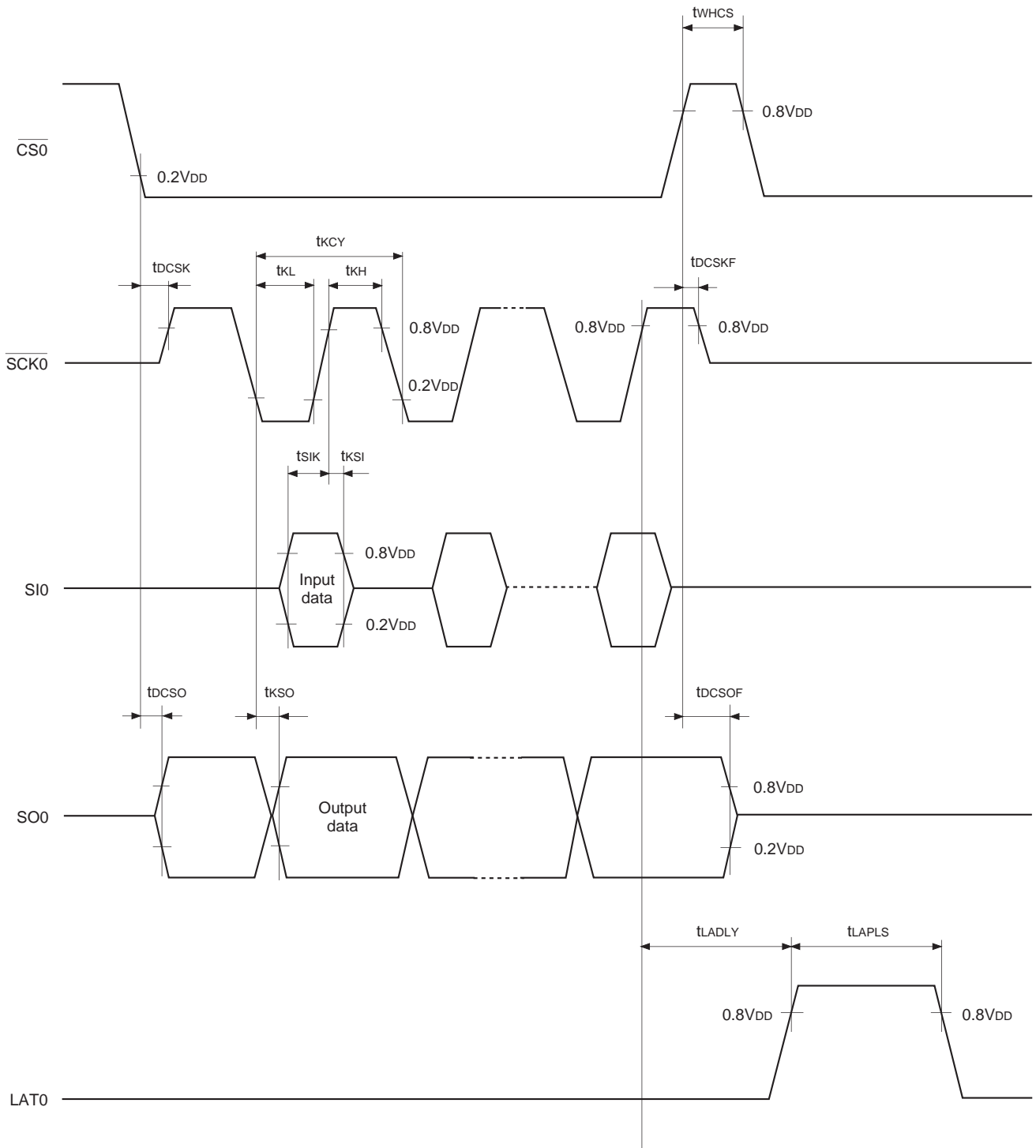


Fig. 4. Serial transfer CH0 timing

(3) Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	500		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	200		ns
			Output mode	$4000/f_c - 25$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	50		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	50		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		100	ns
			$\overline{\text{SCK1}}$ output mode		50	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

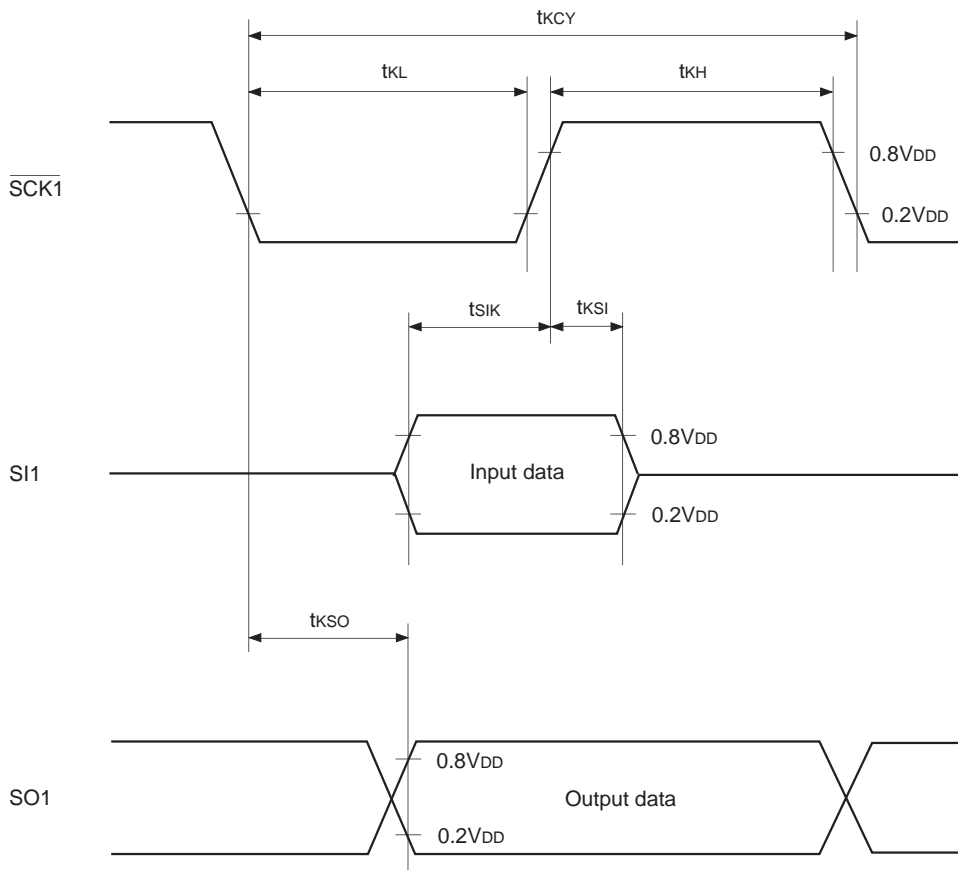
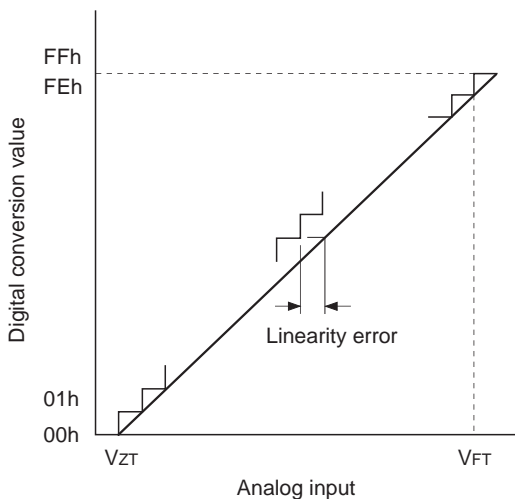


Fig. 5. Serial transfer CH1 timing

(4) A/D converter characteristics (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, AVREF = 4.0 to VDD, VSS = AVSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVREF = 5.0V VSS = AVSS = 0V			±4	LSB
Zero transition voltage	VZT*1			-10	10	70	mV
Full-scale transition voltage	VFT*2			4910	4970	5030	mV
Conversion time	tCONV			27/fADC*3			µs
Sampling time	tSAMP			6/fADC*3			µs
Reference input voltage	VREF	AVREF		VDD - 0.5		VDD	V
Analog input voltage	VIAN	AN0 to AN7		0		AVREF	V
AVREF current	IREF	AVREF	Operation mode		0.6	1.0	mA
	IREFS		Sleep mode Stop mode			10	µA



- *1 VZT: Value at which the digital conversion value changes from 00H to 01H and vice versa.
- *2 VFT: Value at which the digital conversion value changes from FEH to FFH and vice versa.
- *3 fADC indicates the values below due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H).
 $f_{ADC} = f_c$ (CKS = "0"), $f_c/2$ (CKS = "1")
 However, the selection for $f_{ADC} = f_c$ (CKS = "0") is limited in the clock range of $f_c = 1$ to 14MHz (VDD = 4.5 to 5.5V).

Fig. 6. Definition of A/D converter terms

(5) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t _{IH}	INT0 INT1 INT2 INT3		1		μs
	t _{IL}	$\overline{\text{NMI}}$				
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

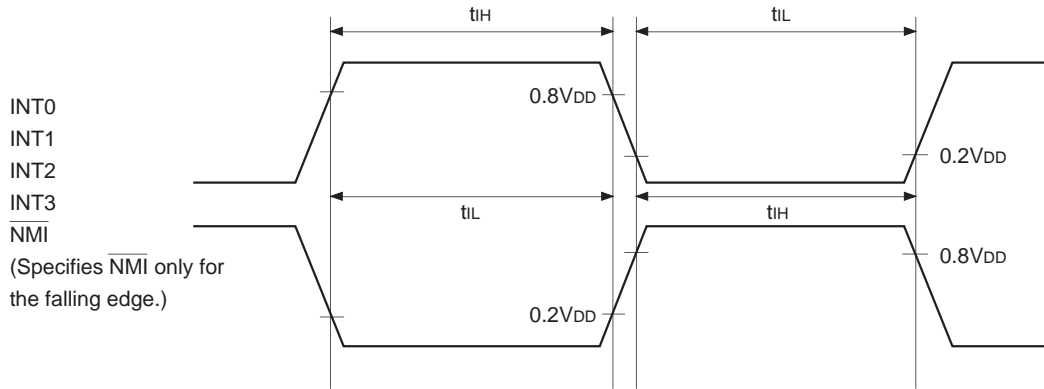


Fig 7. Interruption input timing

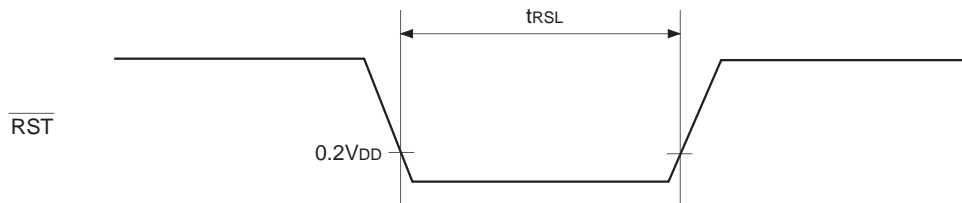
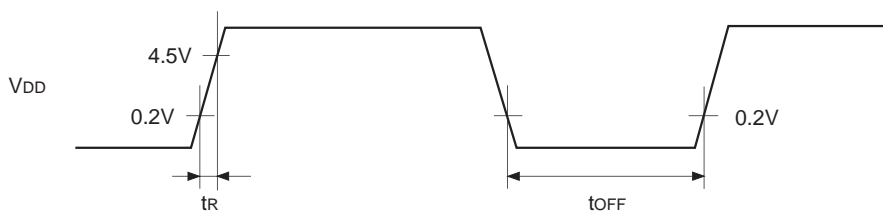


Fig. 8. $\overline{\text{RST}}$ input timing

(6) Power-on reset (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Power supply rise time	t _R	VDD	Power-on reset	0.05	50	ms
Power supply cut-off time	t _{OFF}		Repetitive power-on reset	1		ms



Turn the power on smoothly.

Fig. 9. Power-on reset

Appendix

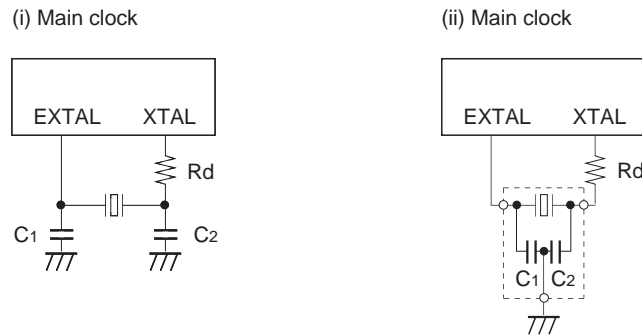


Fig. 10. SPC700 Series recommended oscillation circuit

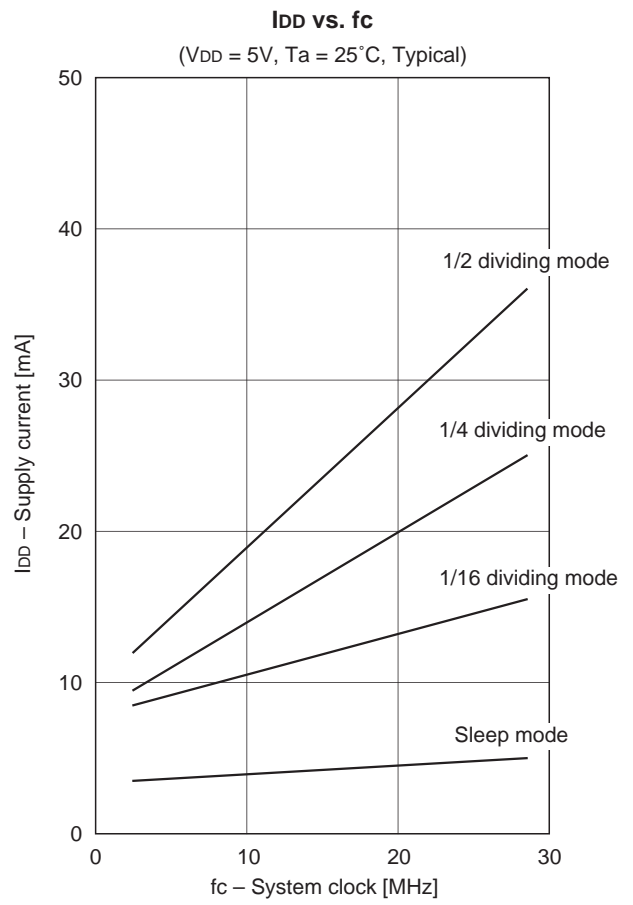
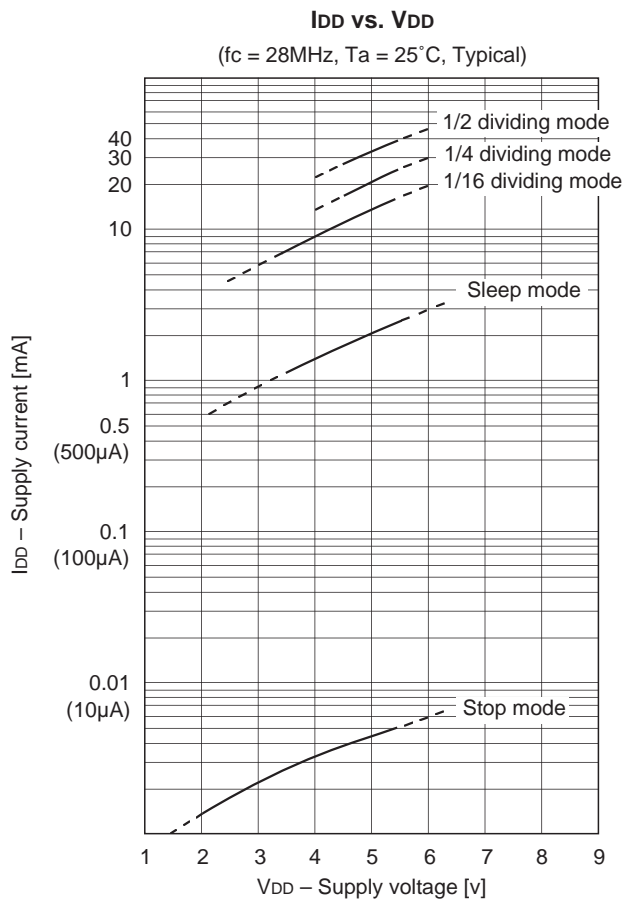
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CSA10.0MTZ	10.00				
	CSA12.00MTZ	12.00				
	CST8.00MTW*1	8.00				(ii)
	CST10.0MT*1	10.00				
	CST12.0MTW*1	12.00				
	CSA16.00MXZ040	16.00	5	5	0	(i)
	CST16.00MXZ0C1*1	16.00	5	5	0	(ii)
	CSA20.00MXZ040	20.00	OPEN	OPEN	0	(i)
	CSA24.00MXZ040	24.00	3	3	0	
CSA28.00MXZ040	28.00	3	3	0		
TDK CORPORATION.	CCR20.0MC6*1	20.00	16	16	0	(ii)
	CCR24.0MC6*1	24.00	16	16	0	
KINSEKI LTD.	HC49/U-S	28.00	1	1	220	(i)
	CX-11F	28.00	1	1	220	

*1 Models with the built-in ground capacitance (C1, C2).

Selection Guide

Option item	Mask	CXP845F60Q-1-□□□
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	40K bytes 48K bytes	Flash EEPROM 60K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent

Characteristics Curves



Writing to Flash EEPROM

The CXP845F60 contains the 60K bytes of flash EEPROM. There are two methods to write to the flash EEPROM; off-board write and on-board write.

The on-board write supports boot mode and user programming mode. Rewriting at the room temperature is recommended.

1. Off-board write

In order to execute the off-board write, the microcomputer is attached on a conversion adaptor and the adaptor is inserted in the socket of the SFP-1 (flash memory programmer) or NICE-SPC700R. (See Fig. 11.)

See the operation manuals for the operation methods of the SFP-1 and NICE-SPC700R. (Mitec SYSTEMS, Inc. manufactures and sells the SFP-1 and NICE-SPC700R.)

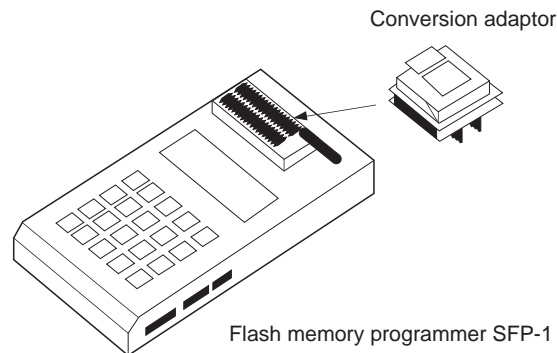


Fig. 11. Off-board write (when writing by using SFP-1)

2. On-board write

This is performed with the microcomputer mounted on the board. The CXP845F60 supports boot mode and user programming mode.

In boot mode, write is performed through the communication with the SFP-1 as shown in Fig. 12.

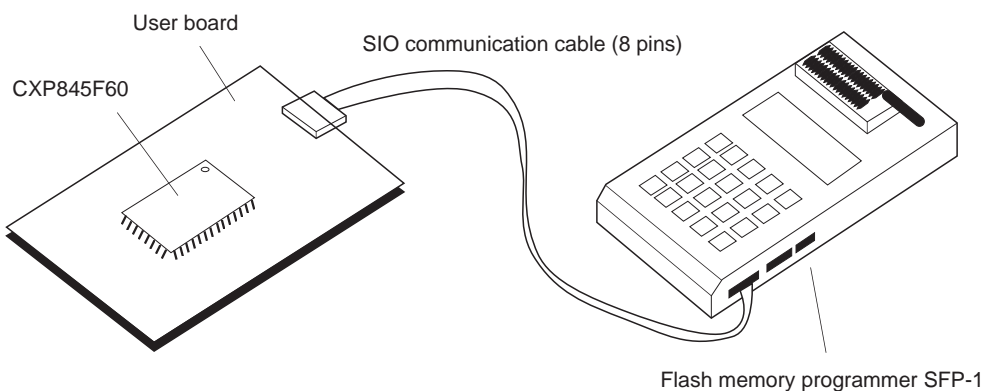


Fig. 12. On-board write boot mode

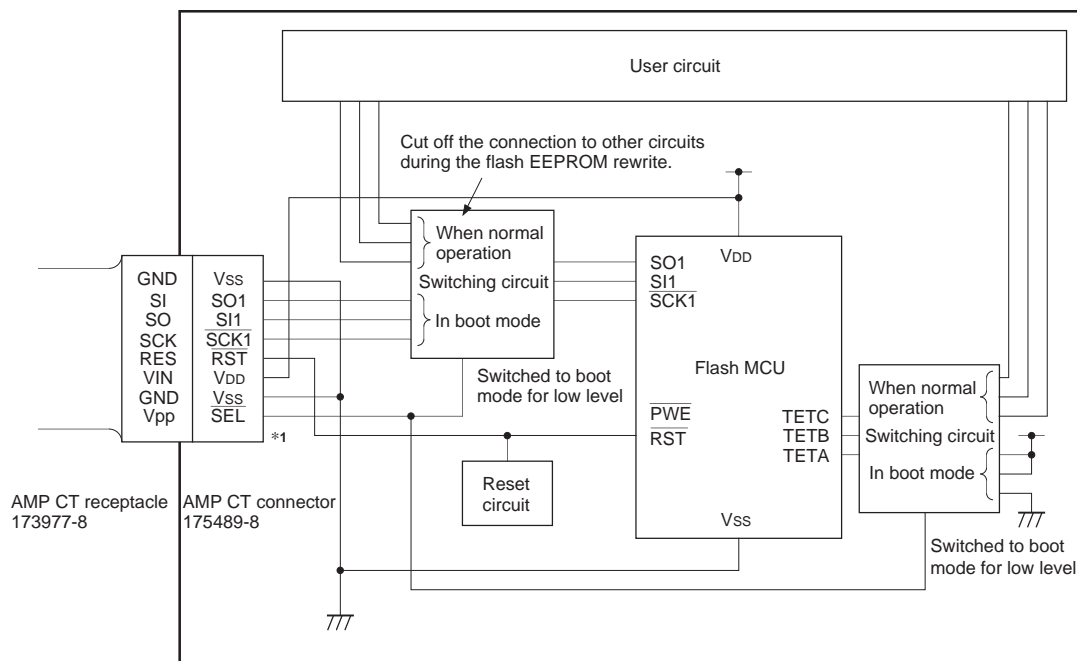
In user programming mode, write is performed in microcomputer mode (normal operation mode) by the communication method (SIO, I/O, etc.) according to the user's application. See the guide of the CXP845F60 write for actual use.

When the on-board write is performed, the pins and flash mode register (FMOD: 01F4h, 0FF0h) should be set as follows.

Mode		Pins					FMOD resister
		RST	TETA	TETB	TETC	PWE	FLMOD bit
On-board write	Boot mode		Low fixed	High output	High fixed	Low fixed	1*1
	User programming mode	High level	X	X	X		1

*1 FLMOD bit is set to "1" automatically in boot mode.

X: don't care



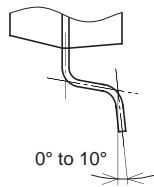
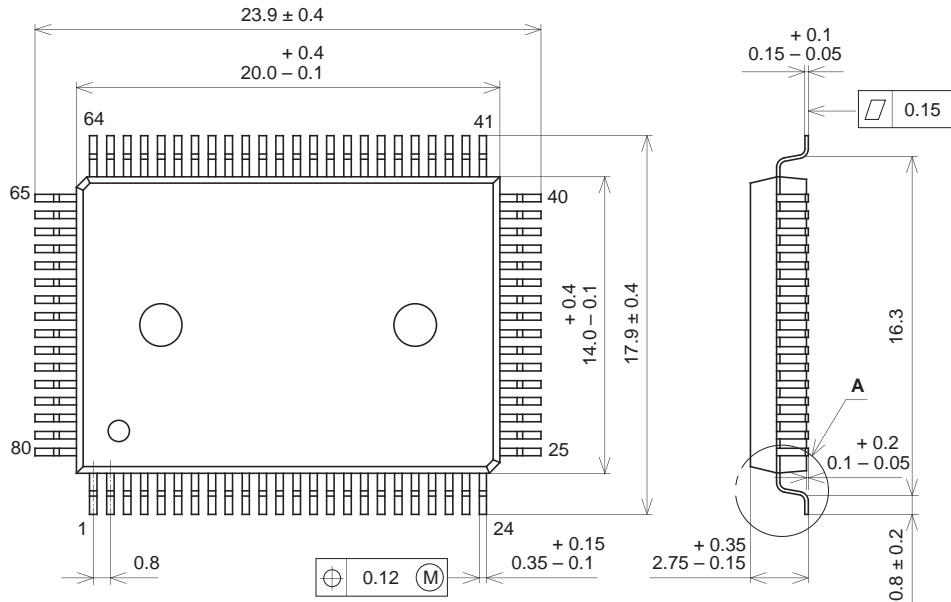
*1 The Vpp signal for the SFP-1 is pulled down with 4.7kΩ. Connecting cable permits writing when PWE pin is fixed at low level. Also, it can be used as select signal of the switching circuit.

Fig. 13. Connection example for boot mode

Pin No.	Connector for SFP-1 (AMP CT receptacle 173977-8)		Signal direction	Connector for user board (AMP CT connector 175489-8)	
	Symbol	Remarks		Symbol	Remarks
1	GND			GND	
2	SI	4.7kΩ pull-up	←	SO1	
3	SO	Open drain, 4.7kΩ pull-up	→	SI1	
4	SCK	Open drain, 4.7kΩ pull-up	↔	SCK1	
5	RST	Open drain, 4.7kΩ pull-up	→	RST	Pull-up in the microcomputer (mask option)
6	VIN		←	VDD	
7	GND			GND	
8	Vpp	4.7kΩ pull-up	→	PWE	Pull-up in the microcomputer

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g