

SYNCHRONIZATION PROCESSOR FOR TELEVISION RECEIVERS

GENERAL DESCRIPTION

The TDA8370 is a sync processor designed to generate and synchronize horizontal and vertical signals in medium and high performance television receivers. The device is particularly suitable for application with teletext decoders and video tape recorders.

A video switch controlled by I²C bus command or analogue switched voltage selects internal or external composite video signals.

The processing of not line-locked vertical sync in non-standard mode is also possible.

Features

- Two separate video inputs adapted to:
 - 1.F. detector (front-end output)
 - or
 - peri-television connector selected by the video switch
- Buffered video output
- Horizontal sync separator with self-aligning levels
- Vertical sync separator 1 with self-aligning levels when standard mode selected
- Vertical sync separator 2 with self-aligning levels when non-standard mode selected (e.g. video tape recorder signal)
- Noise inverter
- Gated phase discriminator with switchable time constant for non-standard applications
- 6 MHz VCO for generation of clock signal for teletext display
- Noise level detector
- Automatic low-current starting circuit
- φ 2 phase control with shift adjustment not affecting gain or time constant
- Horizontal output optimized for operation with self-oscillating power supply
- Vertical divider system with automatic selection of 625 or 525 standard
- 50/60 Hz identification output voltage
- Mute output
- Coincidence detector
- Vertical shaping and feedback system with automatic 60 Hz amplitude correction
- 3-level sandcastle output
- Vertical guard circuit active via sandcastle output
- Scan composite sync (S.C.S.) output as slave input for teletext decoder
- Special "sense" ground pin to ensure correct feedback voltage in the frame deflection circuit
- I²C bus controlled teletext non-interlaced signal (N.I.L.)
- Line and frame frequencies switched to nominal when noise only is received in standard mode

PACKAGE OUTLINES

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V _p	10	12	13,2	V
Supply current (pin 22)	I _p	—	125	150	mA
Starting current (pin 23)	I ₂₃	5	5,5	10	mA
Video input voltage (positive video)					
pin 1 (peak-to-peak value)	V _{1-20(p-p)}	—	2,25	3	V
pin 5 (peak-to-peak value)	V _{5-20(p-p)}	—	1	1,4	V
Horizontal flyback input current (pin 18)	I ₁₈	0,3	1	4	mA
Vertical comparator input (pin 14)					
a.c. input voltage (peak-to-peak value)	V _{14-20(p-p)}	—	3	—	V
d.c. input voltage	V ₁₄₋₂₀	—	2,5	—	V
I ² C clock input/analogue input (pin 7)					
analogue video switching voltage level	V ₇₋₂₀	6,5	—	7,5	V
I ² C data input/analogue input (pin 8)					
for selecting peri-television connector input					
analogue switching voltage level for selecting					
non-standard mode (equal to V.T.R.)	V ₈₋₂₀	6,5	—	7,5	V
Max. horizontal output voltage (pin 17)	V ₁₇₋₂₀	14	—	16	V
Max. vertical drive output voltage (pin 13)	V ₁₃₋₂₀	—	—	10	V
Sandcastle 3-level output voltage (pin 9)					
burstkey	V ₉₋₂₀	—	10,8	—	V
horizontal blanking	V ₉₋₂₀	4,1	4,4	4,9	V
vertical blanking	V ₉₋₂₀	2,1	2,6	2,9	V
Scan composite sync output (pin 10)					
high output voltage at -I ₁₀ = 5 mA	V ₁₀₋₂₀	4,3	4,8	5,3	V
output current	-I ₁₀	—	1	—	mA
Video output (pin 3)					
a.c. output voltage (peak-to-peak value)	V _{3-20(p-p)}	2,6	3	3,4	V
d.c. level top sync	V ₃₋₂₀	2,8	3,2	3,7	V
50/60 Hz identification output voltage (pin 4)					
50 Hz at I ₄ = 0,1 mA	V ₄₋₂₀	—	1,3	1,7	V
60 Hz at -I ₄ = 5 mA	V ₄₋₂₀	8	10	—	V
output current	-I ₄	—	—	5	mA
Mute output voltage (pin 28)					
in-sync at I ₂₈ = 0,1 mA	V ₂₈₋₂₀	—	1,2	1,5	V
out-of-sync/no sync at -I ₂₈ = 0,5 mA	V ₂₈₋₂₀	—	10,5	—	V

DEVELOPMENT DATA

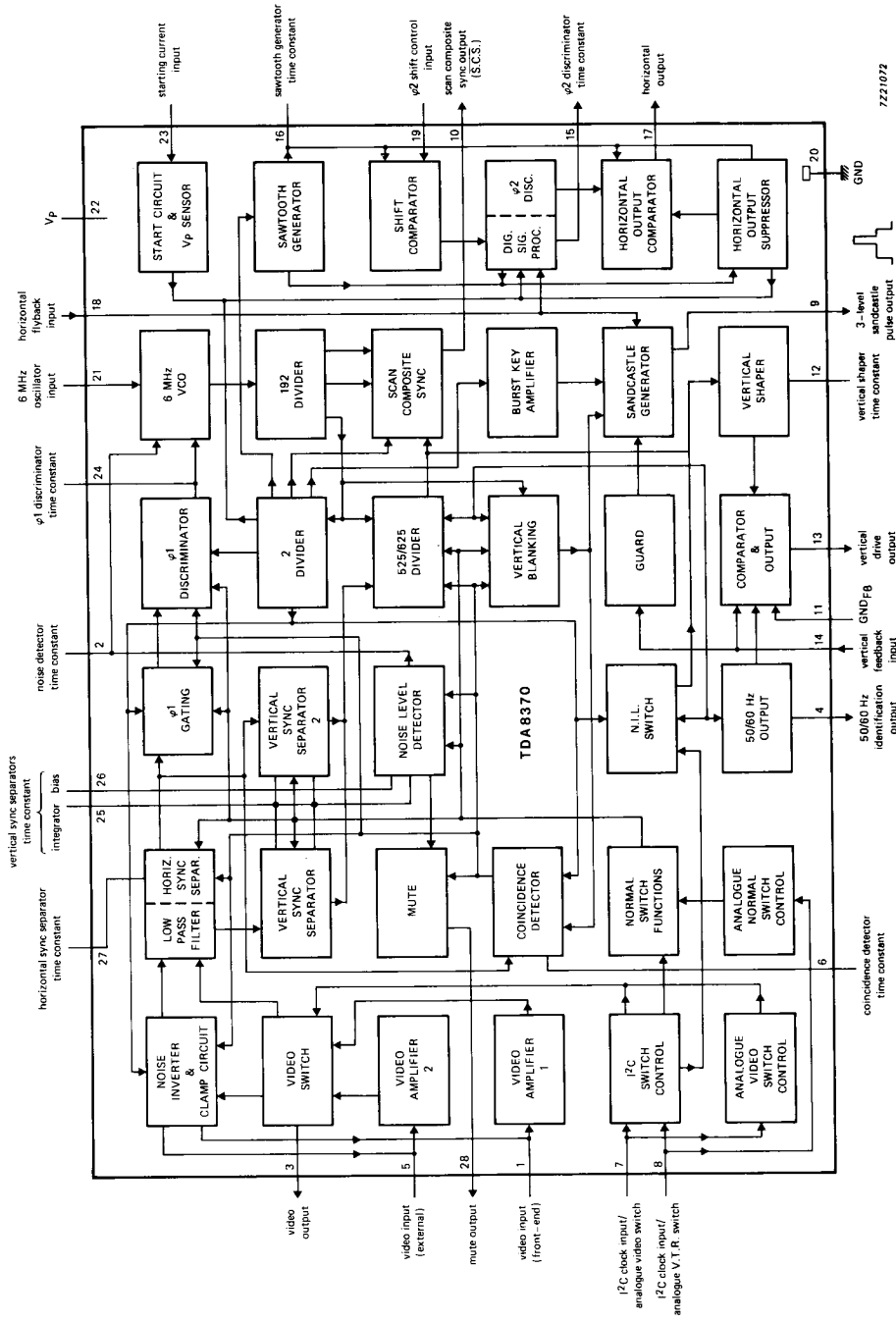


Fig. 1 Block diagram.

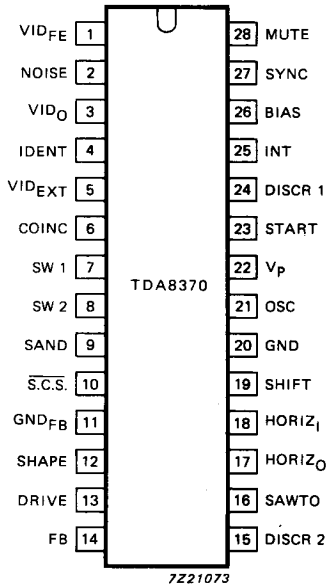


Fig. 2 Pinning diagram.

PINNING

- | | | |
|----|----------------------------|--|
| 1 | VID _{FE} | video input (front-end) |
| 2 | NOISE | noise detector time constant |
| 3 | VID _O | video output |
| 4 | IDENT | 50/60 Hz identification output |
| 5 | VID _{EXT} | video input (external) |
| 6 | COINC | coincidence detector time constant |
| 7 | SW 1 | I ² C clock input/analogue video switch |
| 8 | SW 2 | I ² C data input/analogue V.T.R. switch |
| 9 | SAND | 3-level sandcastle pulse output |
| 10 | $\overline{\text{S.C.S.}}$ | scan composite sync output |
| 11 | GND _{FB} | ground feedback input |
| 12 | SHAPE | vertical shaper time constant |
| 13 | DRIVE | vertical drive output |
| 14 | FB | vertical feedback input |
| 15 | DISCR 2 | φ 2 discriminator time constant |
| 16 | SAWTO | sawtooth generator time constant |
| 17 | HORIZ _O | horizontal output |
| 18 | HORIZ _I | horizontal flyback input |
| 19 | SHIFT | φ 2 shift control input |
| 20 | GND | ground |
| 21 | OSC | 6 MHz oscillator time constant |
| 22 | V _P | positive supply voltage |
| 23 | START | starting current input |
| 24 | DISCR 1 | φ 1 discriminator time constant |
| 25 | INT | integrator time constant
vertical sync separators |
| 26 | BIAS | time constant bias
vertical sync separators |
| 27 | SYNC | horizontal sync separator time constant |
| 28 | MUTE | mute output |

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 22)	V_p	max.	13,2 V
Starting current (pin 23)	I_{23}	max.	10 mA
Power dissipation	P_{tot}	max.	2 W
Storage temperature range	T_{stg}		-25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Thermal resistance			
From junction to ambient (in free)	$R_{th\ j\ a}$	=	40 K/W
Operating junction temperature	T_j	max.	150 °C

DEVELOPMENT DATA

CHARACTERISTICS

$V_p = 12 \text{ V}$; $I_{23} = 5,5 \text{ mA}$; 6 MHz clock oscillator operating at nominal frequency; synchronized;
 $T_{amb} = 25 \text{ }^\circ\text{C}$; measured in test set-up Fig. 6; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_p	10	12	13,2	V
Supply current (pin 22)	I_p	—	125	150	mA
Starting current (pin 23)	I_{23}	5,0	5,5	10	mA
Video input (pin 1)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{1-20(p-p)}$	—	2,25	3,0	V
D.C. level top sync	V_{1-20}	5,0	5,5	6,5	V
Input impedance	$ Z_{1-20} $	—	20	—	$k\Omega$
Generator resistance	R_G	—	75	150	Ω
Allowable sync compression *		20	—	—	dB
Video input (pin 5)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{5-20(p-p)}$	—	1,0	1,4	V
D.C. level top sync	V_{5-20}	3,5	4,2	4,9	V
Input impedance	$ Z_{5-20} $	—	20	—	$k\Omega$
Generator resistance	R_G	—	75	150	Ω
Allowable sync compression		20	—	—	dB
Video output (pin 3)					
Output voltage** positive video (peak-to-peak value)	$V_{3-20(p-p)}$	2,7	3,0	3,3	V
D.C. level top sync	V_{3-20}	2,8	3,2	3,7	V
Resistance npn emitter follower	R_{3-20}	—	—	50	Ω
Bandwidth at $-I_3 = 5 \text{ mA}$	B	10	15	—	MHz
Crosstalk between video signals pin 1 or pin 5 to pin 3		—	—	-54	dB
Noise inversion threshold level	V_{3-20}	1,9	2,1	2,3	V

* When not selected the negative-going input voltage is clamped at 0 V.

** Measured at $V_{1-20(p-p)} = 2,25 \text{ V}$ or $V_{5-20(p-p)} = 1 \text{ V}$.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Horizontal sync separator (pin 27)					
D.C. voltage level	V_{27-20}	—	6,2	—	V
Line ripple voltage (peak-to-peak value) during standard mode	V_{27-20}	—	2,8	—	mV
during non-standard mode	V_{27-20}	—	0,6	—	mV
φ 1 discriminator (pin 24)					
Catching range	$\pm \Delta f$	600	1000	1400	Hz
Holding range	$\pm \Delta f$	*	1000	1200	Hz
Phase shift		—	0,5	—	$\mu\text{s}/\text{kHz}$
Input resistance during sync pulse with slow time constant	R_{24-20}	—	12,6	—	$\text{k}\Omega$
with fast time constant	R_{24-20}	—	2,2	—	$\text{k}\Omega$
6 MHz VCO (pin 21)					
Output frequency free running at $V_{2-20} > 7 \text{ V}$	f_o	—	6	—	MHz
Frequency variation without tolerance of external components	Δf_o	—	—	± 4	%
Frequency variation as a function of supply voltage	$\Delta f_o / \Delta V_p$	—	—	0,01	
Temperature coefficient of oscillator frequency	TC_{osc}	—	1400	—	Hz/K
A.C. input voltage (peak-to-peak value)	$V_{21-20(p-p)}$	—	0,3	—	V
D.C. input voltage	V_{21-20}	—	1,6	—	V
Sawtooth generator (pin 16)					
Start of negative slope of sawtooth	V_{16-20}	—	7,2	—	V
Start flyback of sawtooth	V_{16-20}	—	3,7	—	V
φ 2 trigger pulse width (see Fig. 3)	t_W	—	6,8	—	μs
φ 2 loop not synchronized by φ 1 loop					
Start of negative slope of sawtooth	V_{16-20}	—	7,2	—	V
Start flyback of sawtooth	V_{16-20}	—	3,4	—	V
Flyback time (see Fig. 3)	t_{fb}	0,9	1,3	1,7	μs
Output frequency free running at $V_p = 8,5 \text{ V}$	f_o	—	15,4	—	kHz
Frequency variation without tolerance of external components	Δf_o	—	—	± 4	%

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal output (pin 17)					
Output current open collector npn; $V_{17-20} = 0,5 \text{ V}$	I_{17}	—	—	10	mA
Output voltage protection (2 internal zener diodes)	V_{17-20}	14	—	16	V
Maximum output current during voltage protection	I_{17}	—	0	1	mA
Delay between start of sawtooth output pulse at pin 16 and: negative-going edge of horizontal output voltage (see Fig. 3)	t_{d1}	14,5	16	17,5	μs
positive-going control edge of horizontal output voltage (see Fig. 3)	$t_{d2(\text{min.})}$	25	28	31	μs
	$t_{d2(\text{max.})}$	—	T_H	—	μs
	t_{d2^*}	—	T_H	—	μs
Condition: $I_{23} = 5 \text{ to } 10 \text{ mA}$					
Horizontal output pulse present if:	V_{23-20}	—	—	6	V
Horizontal output pulse not present if:	V_{23-20}	4	—	—	V
and	I_{23}	3	—	—	mA
δ Horizontal output is a function of the input voltage at pin 23					
$\delta = 0$	V_{23-20}	—	—	4	V
$\delta = \text{maximum}$	V_{23-20}	8,5	—	—	V
Horizontal output suppression time	t_s	20	22	24	μs
φ 2 discriminator (pin 15)					
Control current	$\pm I_{15}$	600	800	1000	μA
Control sensitivity	$\Delta\varphi_i/\Delta\varphi_o$	—	400	—	
Input current at $V_{15-20} = 4 \text{ V}$; $V_P = 0 \text{ V}$	I_{15}	—	—	0,6	μA
Condition: No flyback pulse and $V_{23-20} > 5 \text{ V}$					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V
Condition: $V_P < 8,9 \text{ V}$					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V

* Delay with no horizontal flyback pulse present at pin 18.

parameter	symbol	min.	typ.	max.	unit
φ 2 shift control input (pin 19)					
Shift control range		—	$1/16T_H + \Delta$	—	μs
Δ		0,2	—	1	μs
Delay between rising edge of horizontal flyback at the slicing level and rising edge of burst key pulse (see Fig. 2)	$t_{d3}(\text{min.})$	—	3	—	μs
	$t_{d3}(\text{max.})$	—	$7 + \Delta$	—	μs
t_{d3} = min. when:	V_{19-20}	—	—	4,5	V
t_{d3} = max. when:	V_{19-20}	0	—	—	V
Shift control is active when:	V_{22-20}	> 8,9	> 9,5	> 10	V
Starting control input (pin 23)					
Starting by current to pin 23:					
minimum	I_{23}	3	—	5	mA
maximum allowed	I_{23}	—	—	10	mA
Starting by a voltage on pin 22:					
required input current	I_{23}	0	—	10	mA
Stabilized voltage	V_{23-20}	8,2	8,7	9,2	V
Supply current is added to starting current if:					
$V_P > V_{23-20}$ and $V_{23-20} < 8,5$ V	V_{23-20}	—	$V_P - V_{BE}$	—	V
Horizontal flyback input (pin 18)					
Slicing level input voltage	V_{18-20}	0,7	0,9	1,1	V
Input current	I_{18}	0,3	1	4	mA
Maximum input current	$-I_{18}$	—	—	1	mA
Maximum input voltage	V_{18-20}	—	—	V_P	V
Vertical sync separator integrator time constant (pin 25)					
Condition: Standard mode					
D.C. voltage level of vertical sync top of integrated video	V_{25-20}	8,5	9,0	9,5	V
black level of integrated video during vertical blanking	V_{25-20}	4,0	4,5	5,0	V
Input resistance	R_{25-20}	—	5,1	—	kΩ
Condition: Non-standard mode					
Input voltage level of integrated vertical sync top level	V_{25-20}	9,5	10,7	11,0	V
integrated vertical sync amplitude (peak-to-peak value)	$V_{25-20}(p-p)$	—	8,9	—	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Vertical sync separator biasing (pin 26)					
Input voltage in standard mode	V ₂₆₋₂₀	—	5,9	—	V
Input voltage in non-standard mode	V ₂₆₋₂₀	—	8,4	—	V
Vertical shaper (pin 12)					
Condition: 50 Hz					
Ramp voltage starting level	V ₁₂₋₂₀	—	2	—	V
Flyback voltage starting level	V ₁₂₋₂₀	6,0	6,25	6,5	V
Condition: 60 Hz					
Ramp voltage starting level	V ₁₂₋₂₀	—	2	—	V
Flyback voltage starting level	V ₁₂₋₂₀	5,35	5,6	5,85	V
Flyback time (normal)	t _{fb}	170	220	270	μs
Flyback time controlled by second half of N.I.L. signal		—	t _{fb} -32	—	μs
Vertical drive output (pin 13)					
Open collector pnp					
Maximum output current at V ₁₃₋₂₀ = 8 V	-I ₁₃	3	—	—	mA
Output voltage LOW with 100 kΩ resistor to ground	V ₁₃₋₂₀	—	—	300	mV
Vertical feedback input (pin 14)					
A.C. input voltage not synchronized					
50 and 60 Hz condition:					
non-standard mode					
input voltage (peak-to-peak value)	V _{14-11(p-p)}	—	3	—	V
d.c. average input voltage	V ₁₄₋₁₁	—	2,8	—	V
Parabolic pre-correction convex (50 Hz)					
		—	4	—	%
Parabolic pre-correction convex (60 Hz)					
		—	3,3	—	%
Guard circuit input					
input voltage HIGH	V ₁₄₋₁₁	5,3	5,7	6,1	V
input voltage LOW	V ₁₄₋₁₁	—	—	0	V
input voltage at V ₁₄₋₂₀ = 2,5 V	-I ₁₄	—	1,5	6,1	μA
Ground feedback input (pin 11)					
A.C. feedback voltage	V ₁₁₋₂₀	—	0	—	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
50/60 Hz identification output (pin 4)					
50 Hz output voltage at $I_4 = 0,1 \text{ mA}$	V4-20	—	1,3	1,7	V
60 Hz output voltage at $-I_4 = 5 \text{ mA}$	V4-20	8	10	—	V
3-level sandcastle output (pin 9)					
Output voltage during burst key at $-I_9 = 0,5 \text{ mA}$	V9-20	—	10,8	—	V
at $-I_9 = 5 \text{ mA}$	V9-20	8,0	9,7	—	V
Output voltage during horizontal blanking at $-I_9 = 0,5 \text{ mA}$	V9-20	4,1	4,4	4,9	V
Output voltage during vertical blanking at $-I_9 = 0,5 \text{ mA}$	V9-20	2,1	2,6	2,9	V
Zero level output voltage at $I_9 = 0,5 \text{ mA}$	V9-20	—	0,25	0,5	V
Pulse width:					
burst key at $V_{9-20} = 7 \text{ V}$	t _W	3,7	4,0	4,3	μs
horizontal blanking at $V_{9-20} = 3,5 \text{ V}$	t _W	—	*	—	
Vertical blanking (see Fig. 4)					
Condition: 50 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t _{bk}	—	16	—	μs
Duration of vertical blanking	t _d	—	$22,5T_H - t_{bk}$	—	μs
Condition: 50 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t _{bk}	—	$-(2,5T_H + 20 \mu\text{s})$	—	
Duration of vertical blanking	t _d	—	$25T_H + 2 \mu\text{s}$	—	
Condition: 60 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t _{bk}	—	16	—	μs
Duration of vertical blanking	t _d	—	$18,5T_H - t_{bk}$	—	μs
Condition: 60 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t _{bk}	—	0	—	μs
Duration of vertical blanking	t _d	—	$18,5T_H$	—	μs
Phase position of burst key delay between the middle of the sync pulse on the video input and the rising edge of the burst key pulse at a slicing level of 7 V		2,5	2,9	3,3	μs

* Width of horizontal flyback on pin 18 pulse at the slicing level.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
S.C.S. output (pin 10)					
Output voltage HIGH at $-I_{10} = 5 \text{ mA}$	V ₁₀₋₂₀	4,3	4,8	5,3	V
Output voltage LOW at $I_{10} = 0,5 \text{ mA}$	V ₁₀₋₂₀	—	0,2	0,5	V
Conditions:*					
Noise only on video input pin 1 or 5 or indirect sync 50 Hz with a 4,7 μs horizontal sync pulse width on pin 1 or 5					
Delay between the starting edge of the horizontal sync pulse of the video input signal and the starting edge of the horizontal sync pulse in the S.C.S. signal					
		-0,25	0	0,25	μs
Noise detector time constant (pin 2)					
Condition: Standard mode					
Output voltage					
strong signal	V ₂₋₂₀	—	4,6	5,3	V
noise only**	V ₂₋₂₀	—	7,2	—	V
Switching voltage level					
strong signal \rightarrow noise only	V ₂₋₂₀	5,7	6,2	6,7	V
noise only \rightarrow strong signal	V ₂₋₂₀	—	5,6	—	V
Coincidence detector (pin 6)					
Average voltage level					
in-sync	V ₆₋₂₀	6,8	8	—	V
out-of-sync	V ₆₋₂₀	—	—	2,1	V
noise only	V ₆₋₂₀	—	—	2,4	V
Switching voltage level (see also Fig. 5)					
fast \rightarrow normal Δ	V ₆₋₂₀	—	4,4	—	V
normal \rightarrow fast Δ	V ₆₋₂₀	—	2,4	—	V

* All other conditions will cause distorted vertical sync pulses and/or equalizing pulses in the S.C.S. signal.

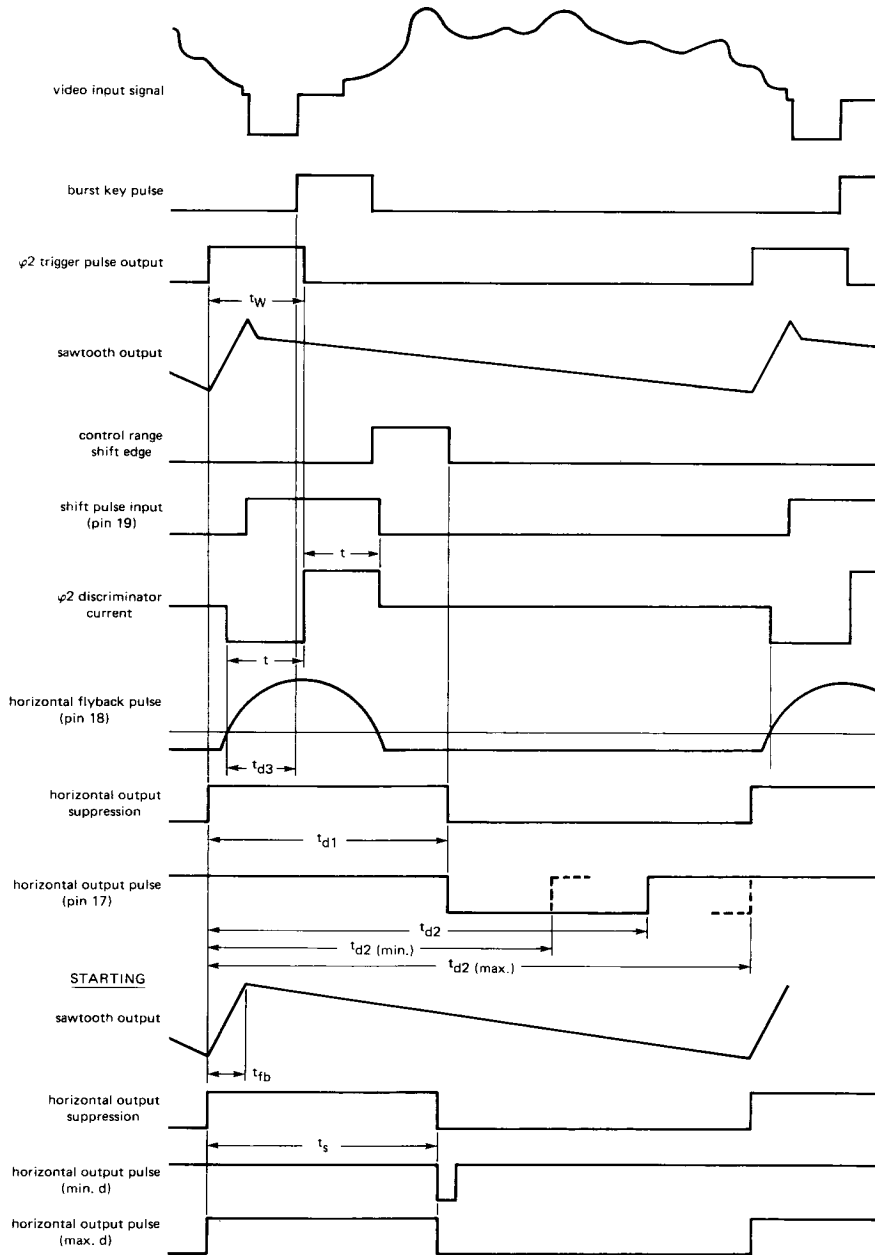
** When noise only is received the 6 MHz oscillator is switched to nominal frequency and the frame divider to the 625 standard.

Δ This switching level is also valid for clamp gating, φ 1 gating, muting, frame divider indirect/direct sync, horizontal sync separator gated/self-aligned and noise detector inhibit/inhibit off.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 28)					
Output voltage					
not synchronized					
at $-I_{28} = 0,5 \text{ mA}$	V_{28-20}	—	10,5	—	V
at $-I_{28} = 5 \text{ mA}$	V_{28-20}	7,0	8,5	—	V
synchronized					
at $I_{28} = 0,1 \text{ mA}$	V_{28-20}	—	1,2	1,5	V
I²C clock input/ analogue input video switch (pin 7)					
Input voltage					
analogue input inactive	V_{7-20}	5	—	—	V
analogue input switching level (external video selected)	V_{7-20}	6,5	—	7,5	V
Input current					
at $V_p = 0 \text{ V}$	$ I_7 $	—	—	10	μA
at $V_p = 12 \text{ V}$	$-I_7$	—	—	10	μA
I ² C clock input switching voltage level	V_{7-20}	1,5	2,6	3,0	V
I²C data input/ * analogue V.T.R. switch (pin 8)					
Input voltage					
analogue input inactive	V_{8-20}	5	—	—	V
analogue input switching level (non-standard mode)	V_{8-20}	6,5	—	7,5	V
Input current					
at $V_p = 0 \text{ V}$	$ I_8 $	—	—	10	μA
at $V_p = 12 \text{ V}$	$-I_8$	—	—	10	μA
I ² C data input switching voltage level	V_{8-20}	1,5	2,6	3,0	V
During acknowledge					
pull-down current	$-I_8$	—	—	5	mA
saturation voltage	V_{8-20}	—	—	1,5	V

* For address and data byte definition see Fig. 6 and Table 1 respectively.



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Fig. 3 Timing diagram; video input and starting time.

DEVELOPMENT DATA

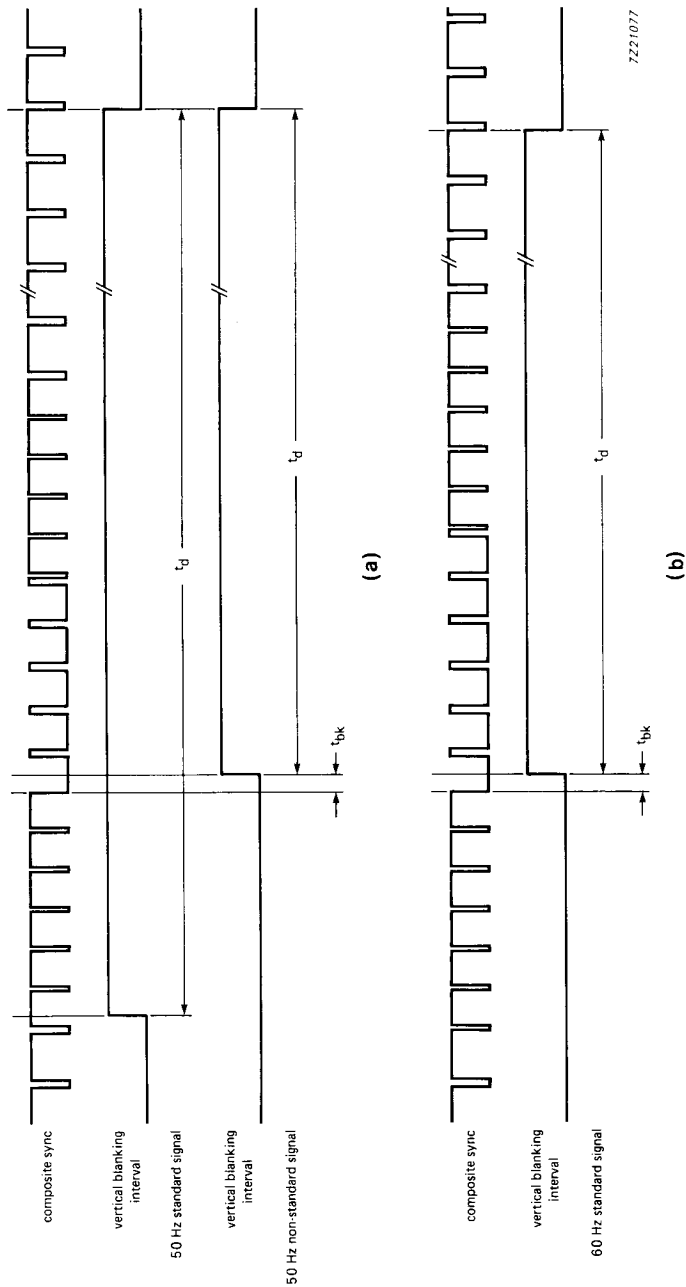
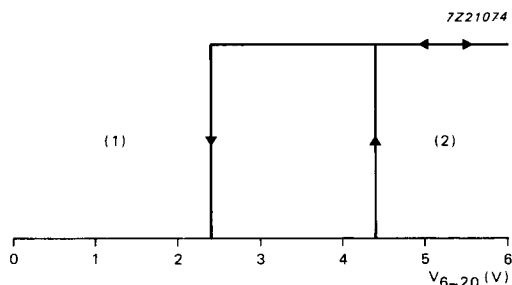


Fig. 4 Timing diagram; vertical blanking synchronization
 (a) 50 Hz standard (b) 60 Hz standard.



(1) ϕ 1 gating circuit off
 ϕ 1 discriminator to fast mode
 clamping gate off
 mute output HIGH
 frame divider direct sync
 horizontal sync separator self-aligned
 noise detector not inhibited

(2) ϕ 1 gating circuit on
 ϕ 1 discriminator to slow mode
 clamping gate on
 mute output LOW
 frame divider indirect sync
 horizontal sync separator gated
 noise detector inhibited

Fig. 5 Coincidence detector time constant switching levels.

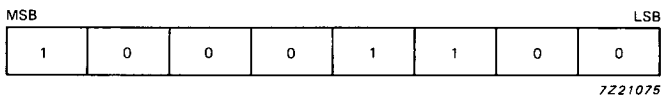


Fig. 6 Address byte.

Table 1 Data byte

	bit no.	logic level	description
MSB	D7	1	*
	D6	1	*
	D5	1	*
	D4	1	*
	D3	1	bit number D5 = don't care
	D3	0	bit numbers D6 and D7 = don't care
	D2	1	$\overline{\text{N.I.L.}}$ (inactive)
	D2	0	N.I.L. (active)
LSB	D1	1	$\overline{\text{VIDEXT}}$ (inactive)
	D1	0	VIDEXT (active)
	D0	1	standard mode
	D0	0	non-standard mode

* Bits D7 to D4 are used for measuring procedure in the IC factory. For application use they must be inactive (logic 1).

DEVELOPMENT DATA

APPLICATION INFORMATION

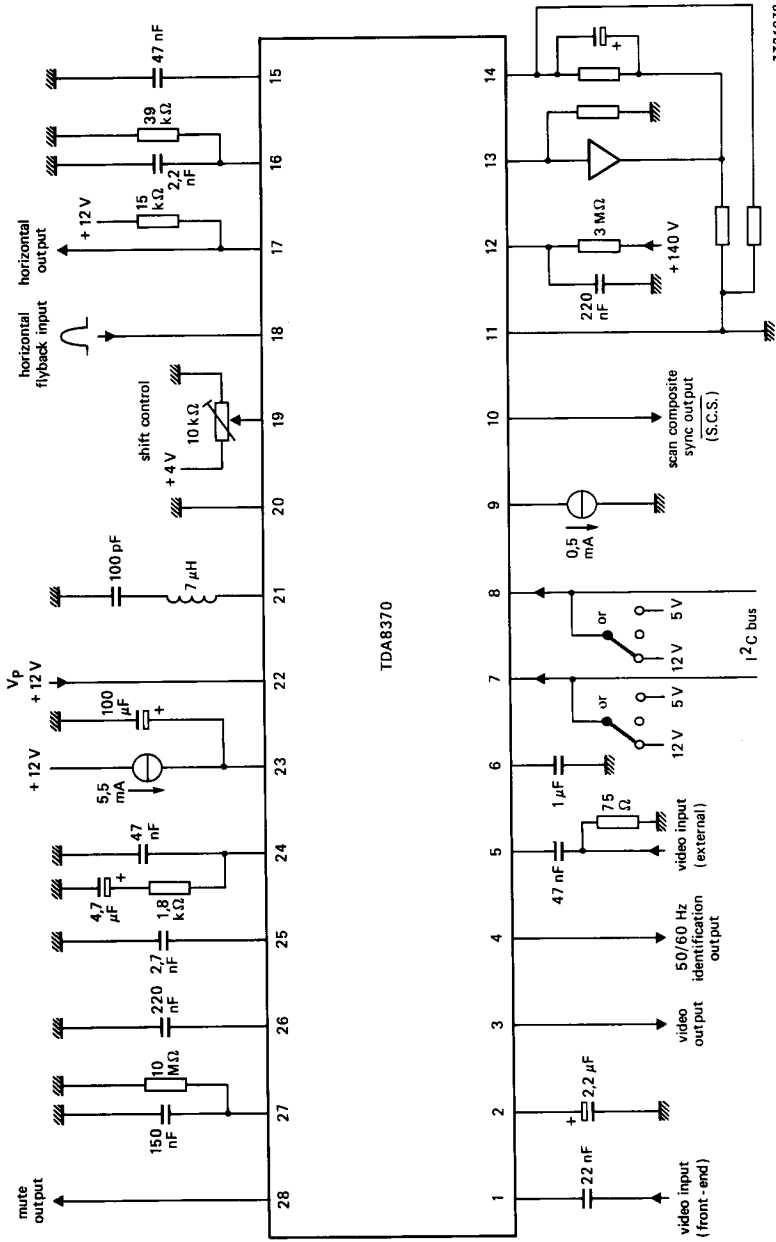


Fig. 7 Application diagram and test circuit.