

Document Title

64Kx36-Bit Synchronous Pipelined Burst SRAM, 3.3V Power Datasheets for 100TQFP

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
Rev. 0.0	Initial draft	Nov. 17. 1996	Preliminary
Rev. 1.0	Final spec release	May. 01. 1997	Final
Rev. 1.1	Change -10/-11 tps from 2.0ns to 2.5ns	Jun. 11. 1997	Final

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64Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V - 5\% / +10\%$ Power Supply
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

GENERAL DESCRIPTION

The KM736V689/L is a 2,359,296-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; \overline{GW} , \overline{BW} , \overline{LBO} , \overline{ZZ} . Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with \overline{CS}_1 high, \overline{ADSP} is blocked to control signals.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

\overline{LBO} pin is DC operated and determines burst sequence(linear or interleaved).

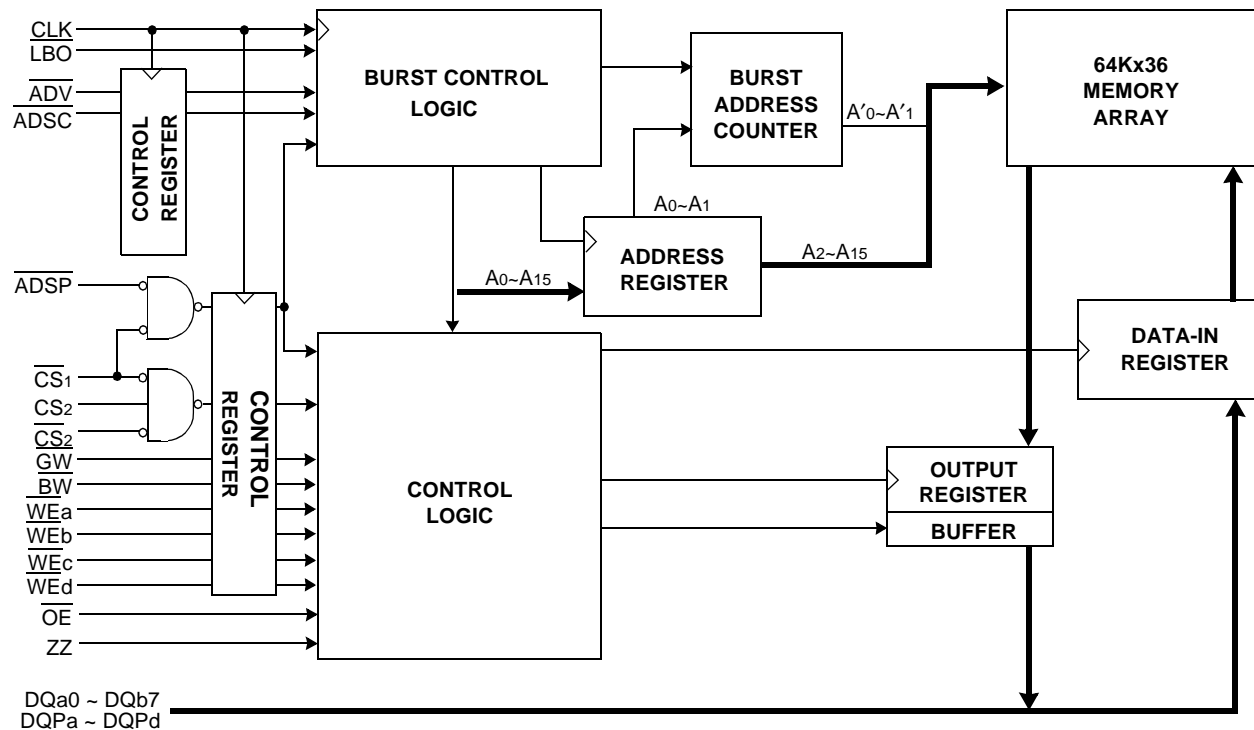
\overline{ZZ} pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM736V689/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

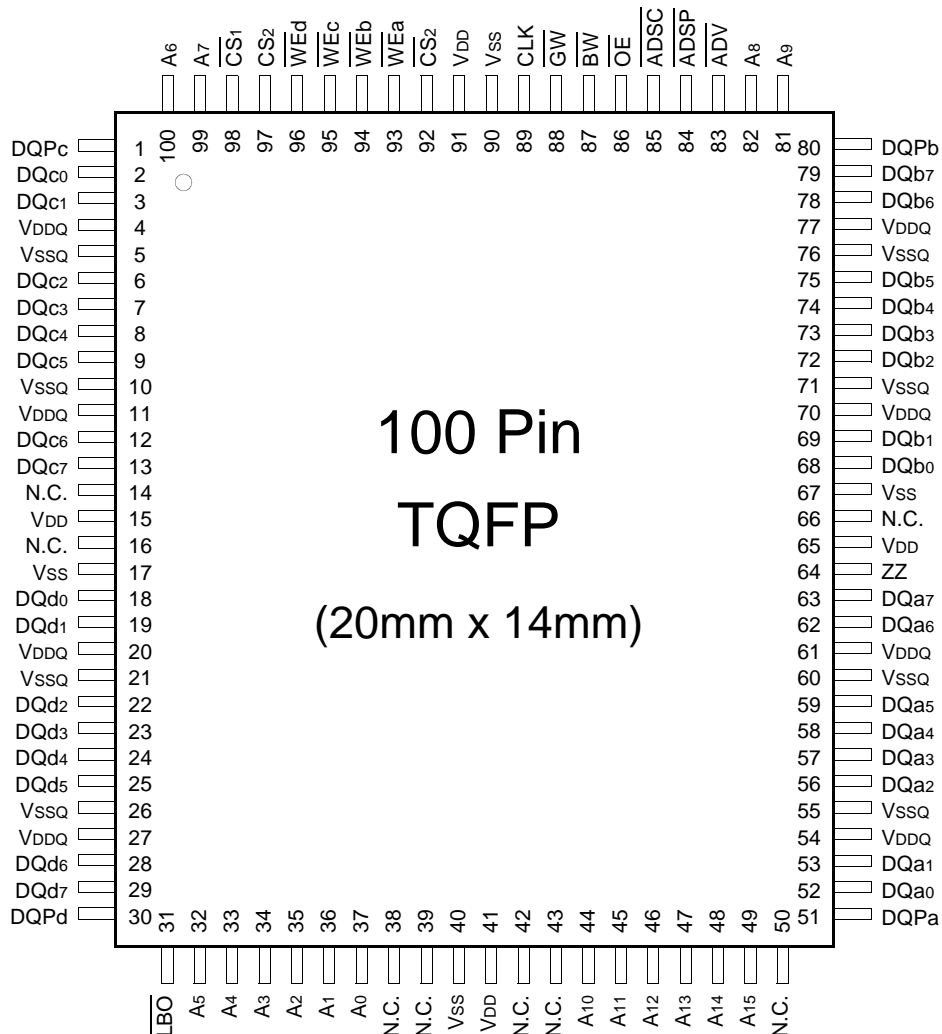
FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	-11	Unit
Cycle Time	t _{CYC}	7.5	8.6	10	11	ns
Clock Access Time	t _{CD}	4.5	5.0	5.0	6.0	ns
Output Enable Access Time	t _{OE}	4.5	5.0	5.0	6.0	ns

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0-A15	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,81,82,99,100	V _{DD}	Power Supply(+3.3V)	15,41,65,91
			V _{SS}	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,50,66
<u>ADV</u>	Burst Address Advance	83	DQ _{a0~a7}	Data Inputs/Outputs	52,53,56,57,58,59,62,63
<u>ADSP</u>	Address Status Processor	84	DQ _{b0~b7}		68,69,72,73,74,75,78,79
<u>ADSC</u>	Address Status Controller	85	DQ _{c0~c7}		2,3,6,7,8,9,12,13
<u>CLK</u>	Clock	89	DQ _{d0~d7}		18,19,22,23,24,25,28,29
<u>CS₁</u>	Chip Select	98	DQ _{Pa~Pd}		51,80,1,30
<u>CS₂</u>	Chip Select	97	V _{DDQ}	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
<u>CS₂</u>	Chip Select	92	V _{SSQ}	Output Ground	5,10,21,26,55,60,71,76
<u>WEx</u>	Byte Write Inputs	93,94,95,96			
<u>OE</u>	Output Enable	86			
<u>GW</u>	Global Write Enable	88			
<u>BW</u>	Byte Write Enable	87			
<u>ZZ</u>	Power Down Input	64			
<u>LBO</u>	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V689/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP (regardless of WEx and ADSC) using the new external address clocked into the on-chip address register whenever ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when WEx are sampled High and ADV is sampled low. And ADSP is blocked to control signals by disabling CS1.

All byte write is done by GW (regardless of BW and WEx), and each byte write is performed by the combination of BW and WEx when GW is high.

Write cycles are performed by disabling the output buffers with OE and asserting WEx. WEx are ignored on the clock edge that samples ADSP low, but are sampled on the subsequent clock edges. The output buffers are disabled when WEx are sampled Low (regardless of OE). Data is clocked into the data input register when WEx sampled Low. The address increases internally to the next address of burst, if both WEx and ADV are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals (WEa, WEb, WEc or WEd) sampled low. The WEa control DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb, WEc controls DQc0 ~ DQc7 and DQPc, and WEd control DQd0 ~ DQd7 and DQPd. Read or write cycle may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.
WEx are sampled on the same clock edge that sampled ADSC low (and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS ₁	CS ₂	CS ₂	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- NOTE : 1. X means "Don't Care".
 2. The rising edge of clock is symbolized by ↑.
 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- NOTE : 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	OE	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

- NOTE
 1. X means "Don't Care".
 2. ZZ pin is pulled down internally
 3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
 5. Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	WRITE	Operation	CS ₁	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	Pd	1.2	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	V
Ground	VSS	0	0	0	V

CAPACITANCE*(TA=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COU	VOUT=0V	-	7	pF

*NOTE : Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}\pm 5\%$)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	IIL	$V_{DD}=V_{SS}$ to V_{DD} ; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	ICC	Device Selected, $I_{OUT}=0\text{mA}$, $ZZ\leq V_{IL}$, All Inputs= V_{IL} or V_{IH} Cycle Time $\geq t_{CYC}$ min	-7	-	395	mA
			-8	-	360	
			-10	-	320	
			-11	-	320	
Standby Current	ISB	Device deselected, $I_{OUT} = 0\text{mA}$, $ZZ\leq V_{IL}$, $f = \text{Max}$, All Inputs $\leq 0.2\text{V}$ or $\geq V_{DD}-0.2\text{V}$	-7	-	100	mA
			-8	-	90	
			-10	-	80	
			-11	-	80	
	ISB1	Device deselected, $I_{OUT} = 0\text{mA}$, $ZZ\leq 0.2\text{V}$, $f = 0$, All Inputs=fixed ($V_{DD}-0.2\text{V}$ or 0.2V)	-	-	10	mA
			L-Ver	-	5.0	mA
ISB2	Device deselected, $I_{OUT}=0\text{mA}$, $ZZ\geq V_{DD}-0.2\text{V}$, $f = \text{Max}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	-	10	mA	
		L-Ver	-	1.0	mA	
Output Low Voltage	VOL	$I_{OL} = 8.0\text{mA}$	-	0.4	V	
Output High Voltage	VOH	$I_{OH} = -4.0\text{mA}$	2.4	-	V	
Input Low Voltage	VIL		-0.5*	0.8	V	
Input High Voltage	VIH		2.0	5.5**	V	

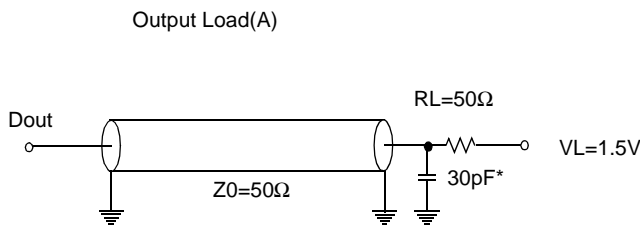
* $V_{IL}(\text{Min})=-3.0(\text{Pulse Width}\leq 20\text{ns})$

** In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.5\text{V}$

TEST CONDITIONS

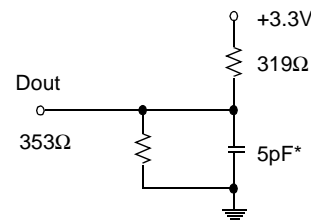
($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}-5\%/+10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1



* Capacitive Load consists of all components of the test environment.

Output Load(B),(3.3V I/O)
(for t_{LZC} , t_{LZOE} , t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

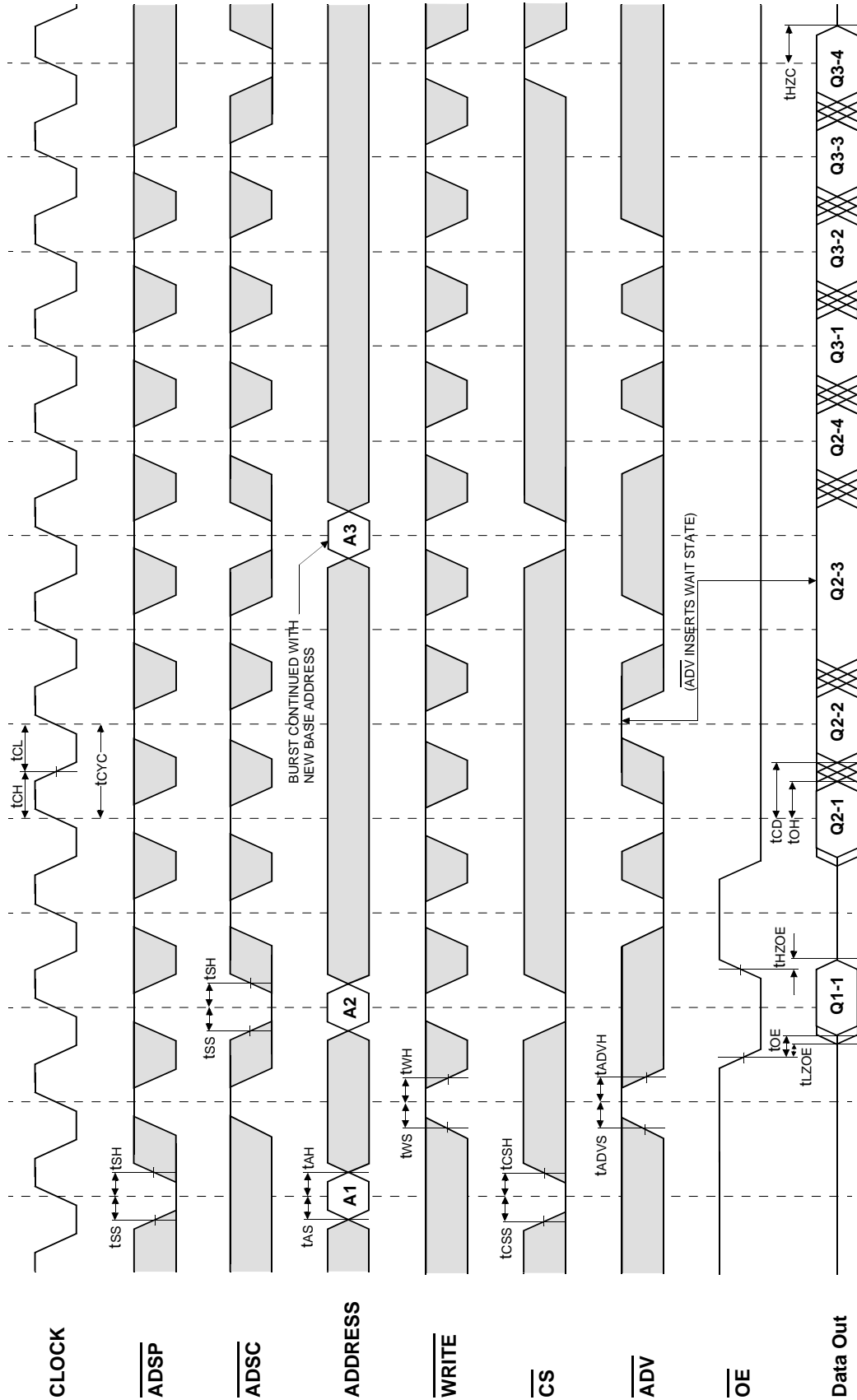
Fig. 1

AC TIMING CHARACTERISTICS(V_{DD}=3.3V-5%/+10%, T_A=0 to 70°C)

Parameter	Symbol	-7		-8		-10		-11		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t _{CYC}	7.5	-	8.6	-	10	-	11	-	ns
Clock Access Time	t _{CD}	-	4.5	-	5.0	-	5.0	-	6.0	ns
Output Enable to Data Valid	t _{OE}	-	4.5	-	5.0	-	5.0	-	6.0	ns
Clock High to Output Low-Z	t _{LZC}	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	t _{OH}	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	t _{HZC}	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	t _{CH}	3.0	-	3.5	-	4.0	-	4.0	-	ns
Clock Low Pulse Width	t _{CL}	3.0	-	3.5	-	4.0	-	4.0	-	ns
Address Setup to Clock High	t _{AS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t _{SS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t _{DS}	2.0	-	2.0	-	2.5	-	2.5	-	ns
Write Setup to Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	t _{WS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t _{ADVS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t _{CSS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t _{SH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	t _{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever \overline{ADSC} and/or \overline{ADSP} is sampled low and \overline{CS} is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 2. Both chip selects must be active whenever \overline{ADSC} or \overline{ADSP} is sampled low in order for the this device to remain enabled.
 3. \overline{ADSC} or \overline{ADSP} must not be asserted for at least 2 Clock after leaving ZZ state.

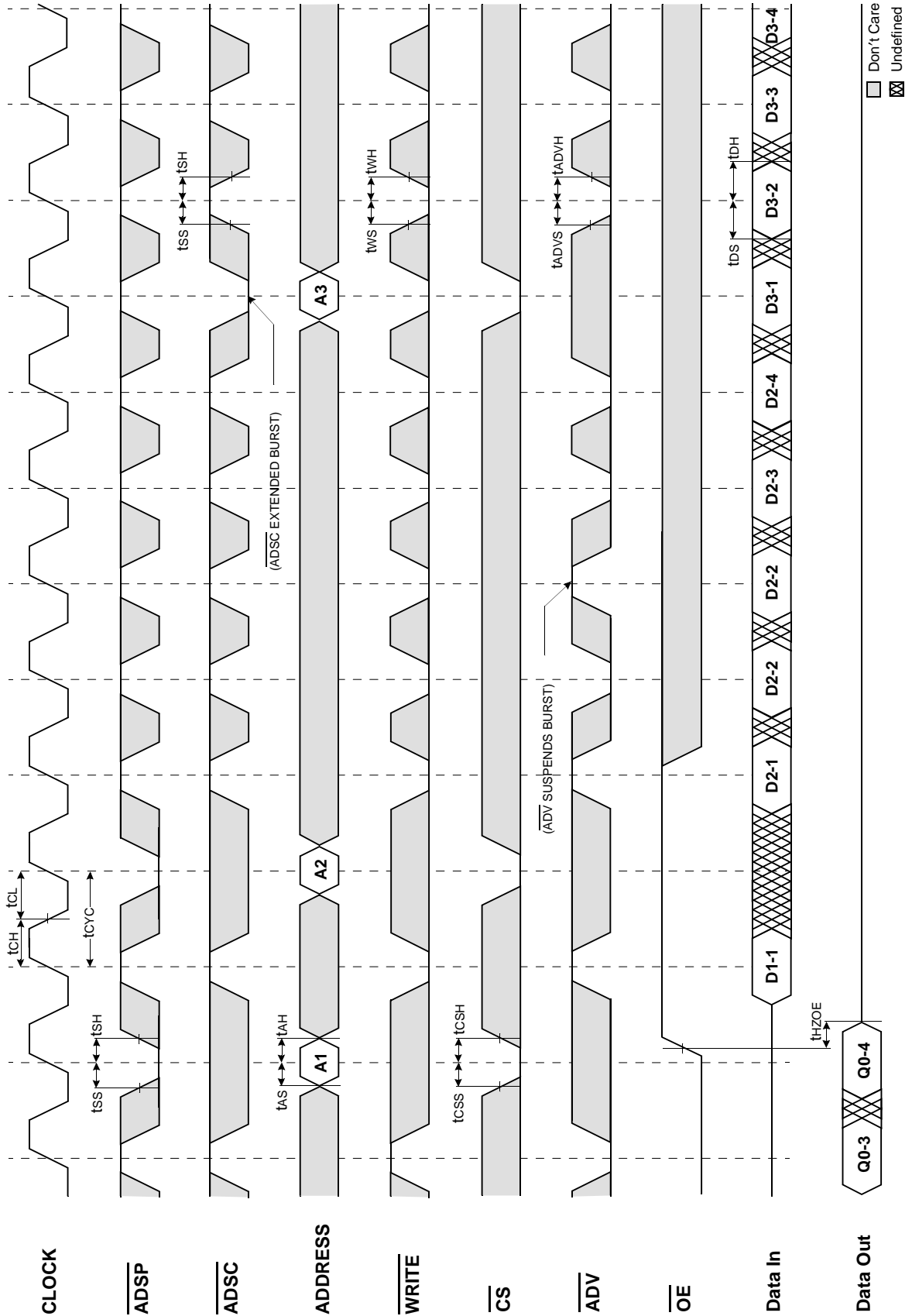
TIMING WAVEFORM OF READ CYCLE



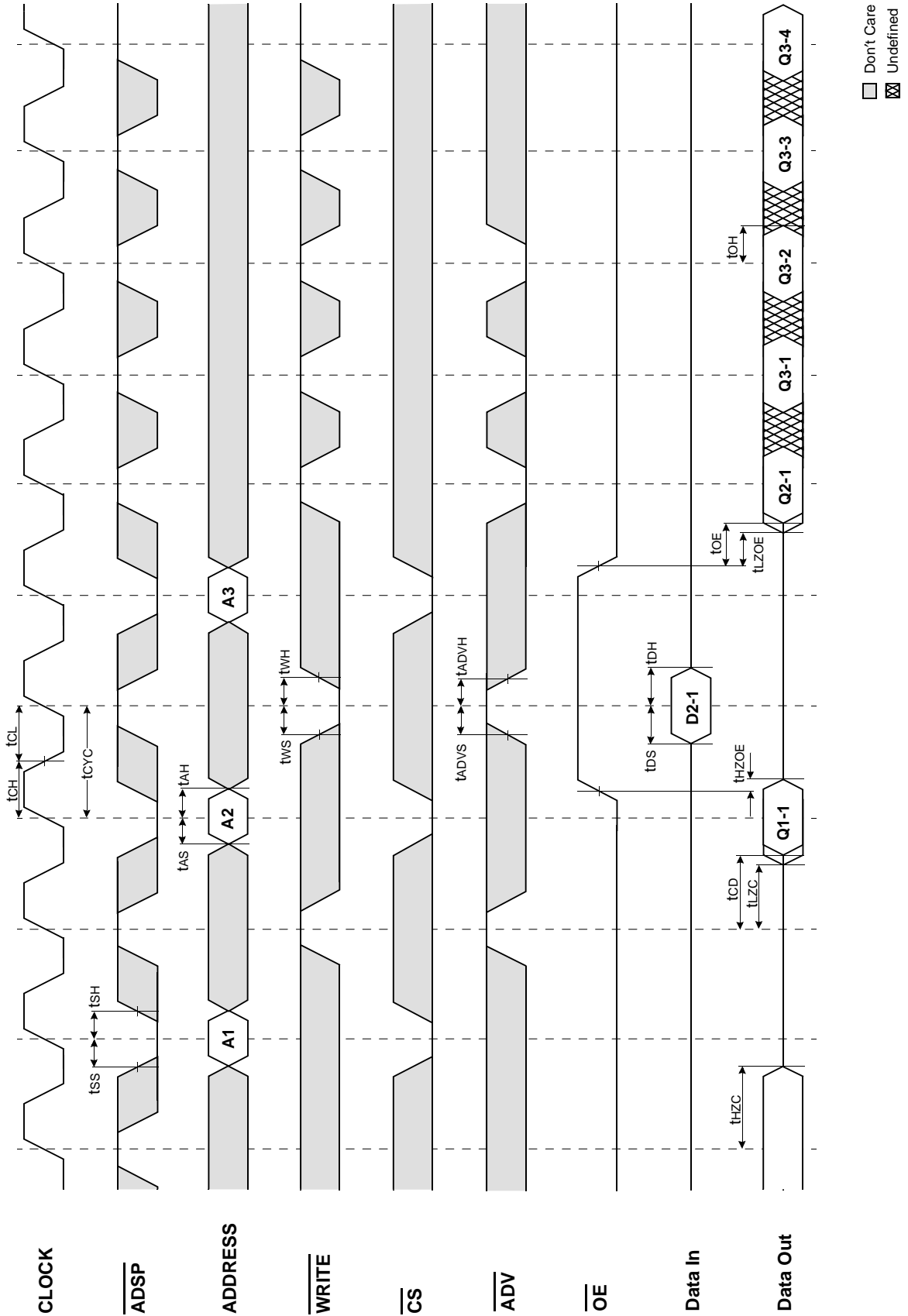
□ Don't Care
 ☒ Undefined

NOTES : $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H, \overline{BW} = L, \overline{WEX} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L, \overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$

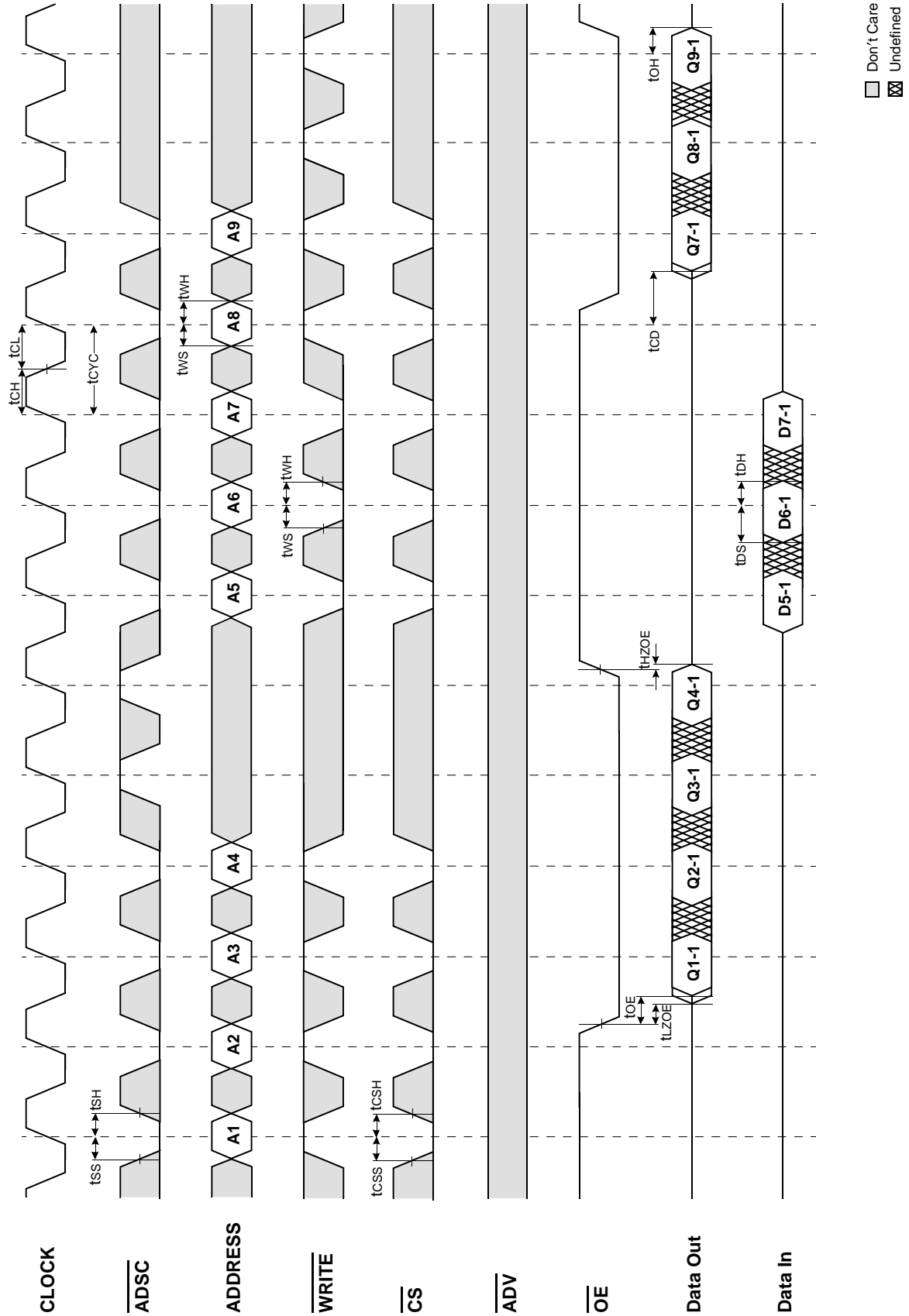
TIMING WAVEFORM OF WRTE CYCLE



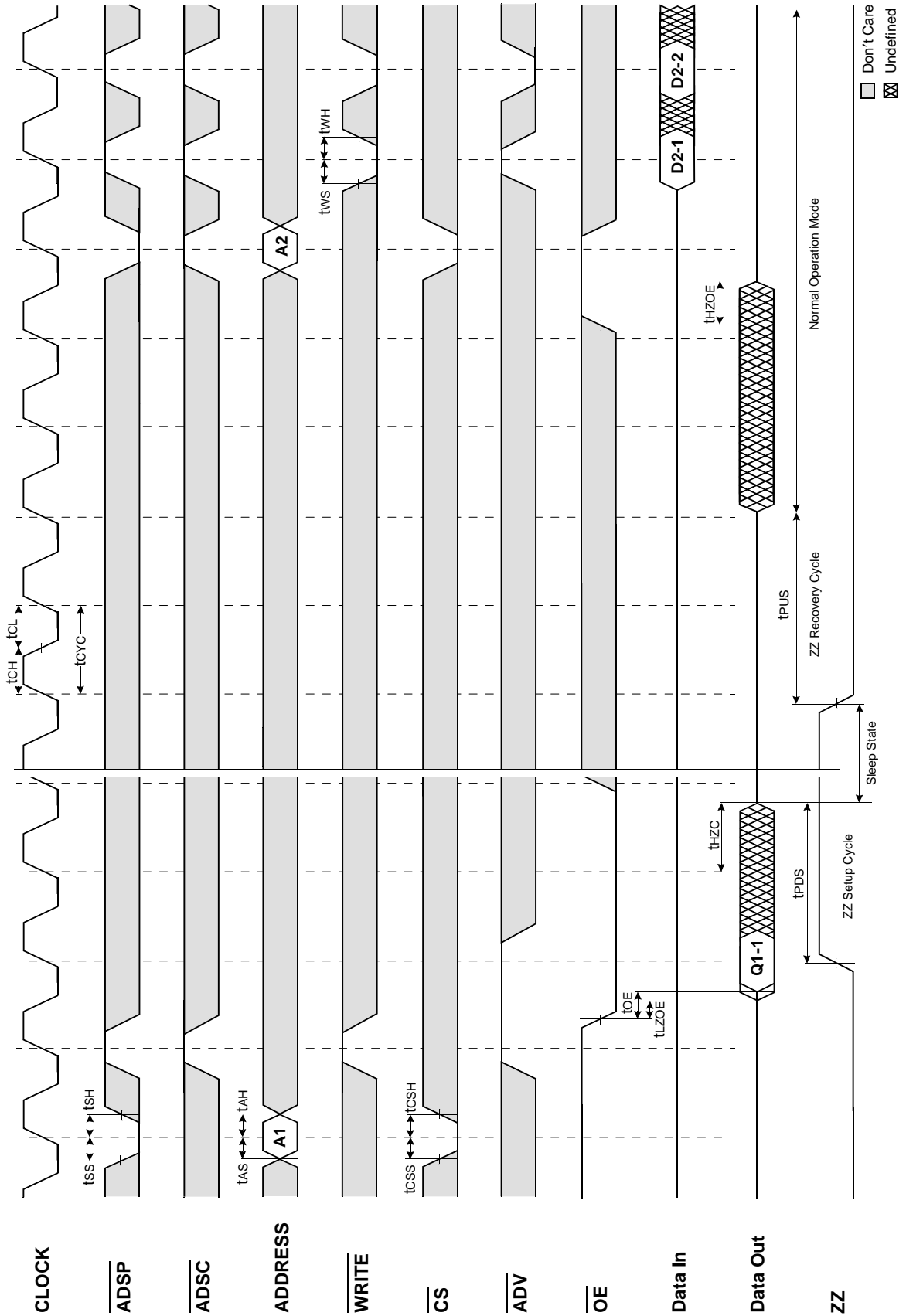
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



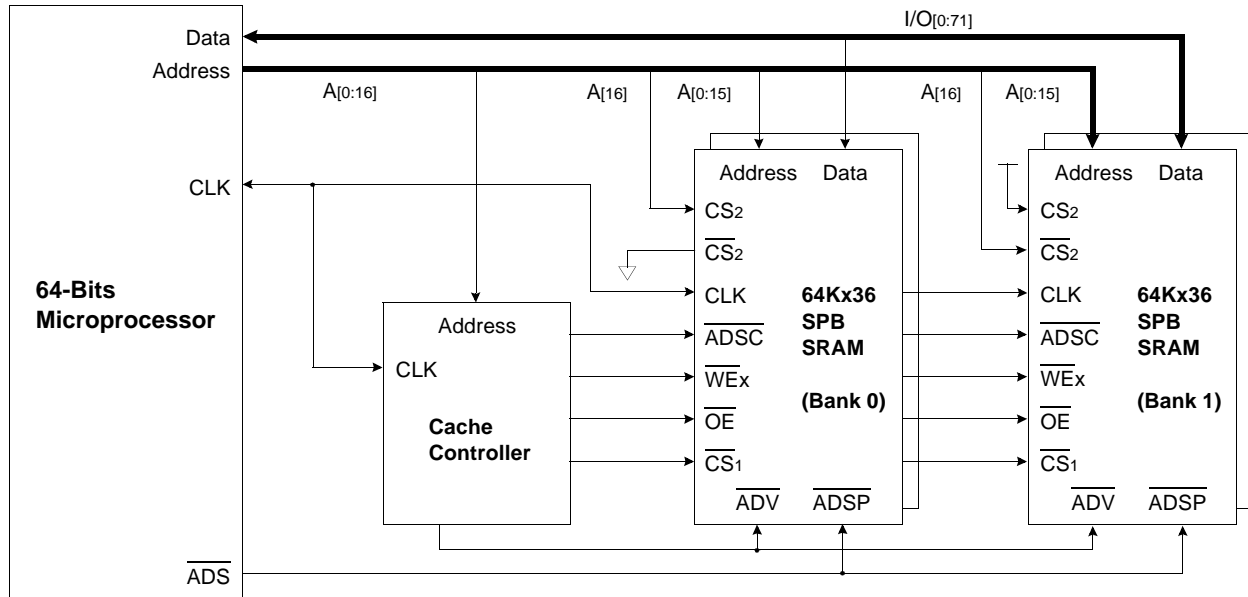
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

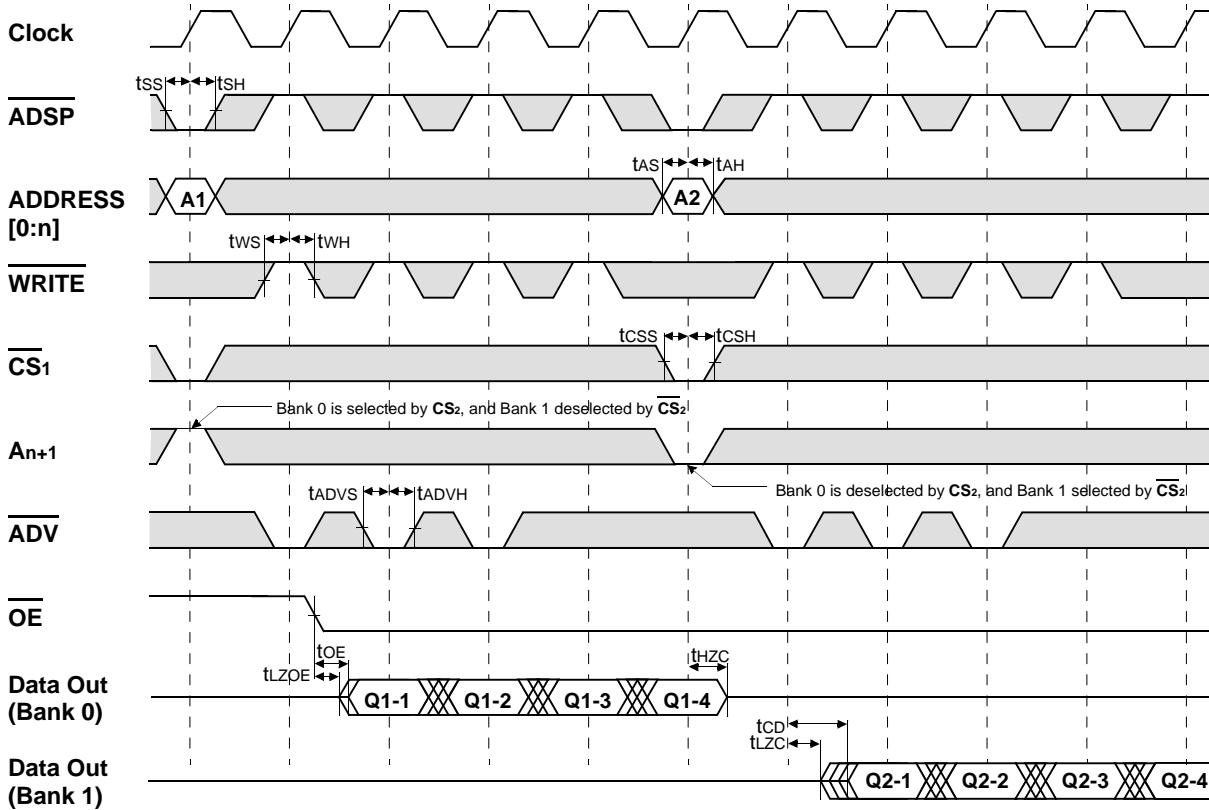
DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



* Please refer to attached timing diagram 2

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



*NOTES n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

□ Don't Care ⊗ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units: millimeters/inches

