Description

The μPD6307 can directly drive any multiplexed LCD organized with up to 32 rows. It is easily cascaded to 128 rows.

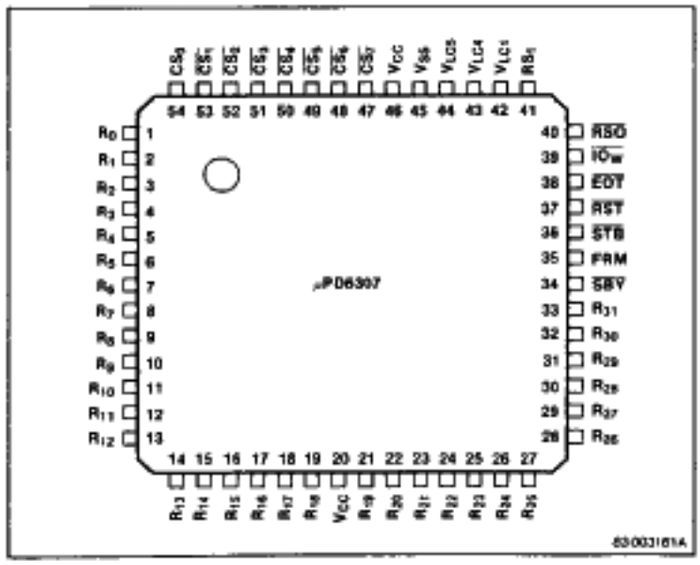
Features

- ☐ High voltage output 21 V maximum
- ☐ Directly controllable by the μPD72030
- ☐ CMOS technology
- ☐ Single 5 V ±10% power supply

Ordering Information

Part Number	Package Type
μPD6307G-F	54-pin plastic miniflat
μPD6307G-R	54-pin plastic miniflat (inverted leads)

Pin Configuration



Pin Identification

No.	Symbol	Function
1-19, 21-23	R_0-R_{31}	Row drive output
20	V_{CC}	Positive power supply
34	$\overline{SBY}$	Standby input
35	FRM	Frame input
36	STB	Strobe input
37	$\overline{RST}$	Reset input
38	$\overline{EOT}$	End of transfer input
39	$\overline{IOW}$	I/O write input
40, 41	RS_0, RS_1	Row select input
42-44	V_{LC1}, V_{LC4}, V_{LC5}	LCD drive supply
45	V_{SS}	Ground
46	V_{CC} (− V_{LC0})	Positive power supply and LCD drive supply
47-54	$\overline{CS_7}$-$\overline{CS_0}$	Chip select output

Pin Functions

R_0-R_{31} (Row Drive Output)

LCD row drive output.

$\overline{CS_0}$-$\overline{CS_7}$ (Chip Select)

Column driver chip select. These outputs are generated by the CS counter and RS_0-RS_1.

V_{LC1}, V_{LC4}, V_{LC5} (LCD Drive Supply)

Reference voltages used to drive R_0-R_{31}.

RS_0, RS_1 (Row Select)

This input selects the row driver cascade connection. It enables expansion to 128 row drive outputs and 32 $\overline{CS}$ outputs, as shown in table 1.

FRM (Frame)

A high level input to this pin displays a positive frame and a low level input displays a negative frame. At the falling or rising edge of the signal, the row counter is cleared and the row driver is started from R_0.

STB (Strobe)

Row drive strobe input. One STB pulse input at the timing interval causes the display of the next row.

$\overline{IOW}$ (I/O Write)

This input increments the CS counter signal following 10 low level $\overline{IOW}$ pulses.

$\overline{EOT}$ (End of Transfer)

This input clears the CS counter when it goes active low.

$\overline{RST}$ (Reset)

This is the row driver reset input. A low input clears the internal counter and row outputs R_0-R_{31}, and sets the CS_0-CS_7 outputs to a high level.

$\overline{SBY}$ (Standby)

This is the standby input. A low level input to this pin sets the row outputs R_0-R_{31} to V_{LC0}. Before entering standby mode, set all column driver display data to high level.

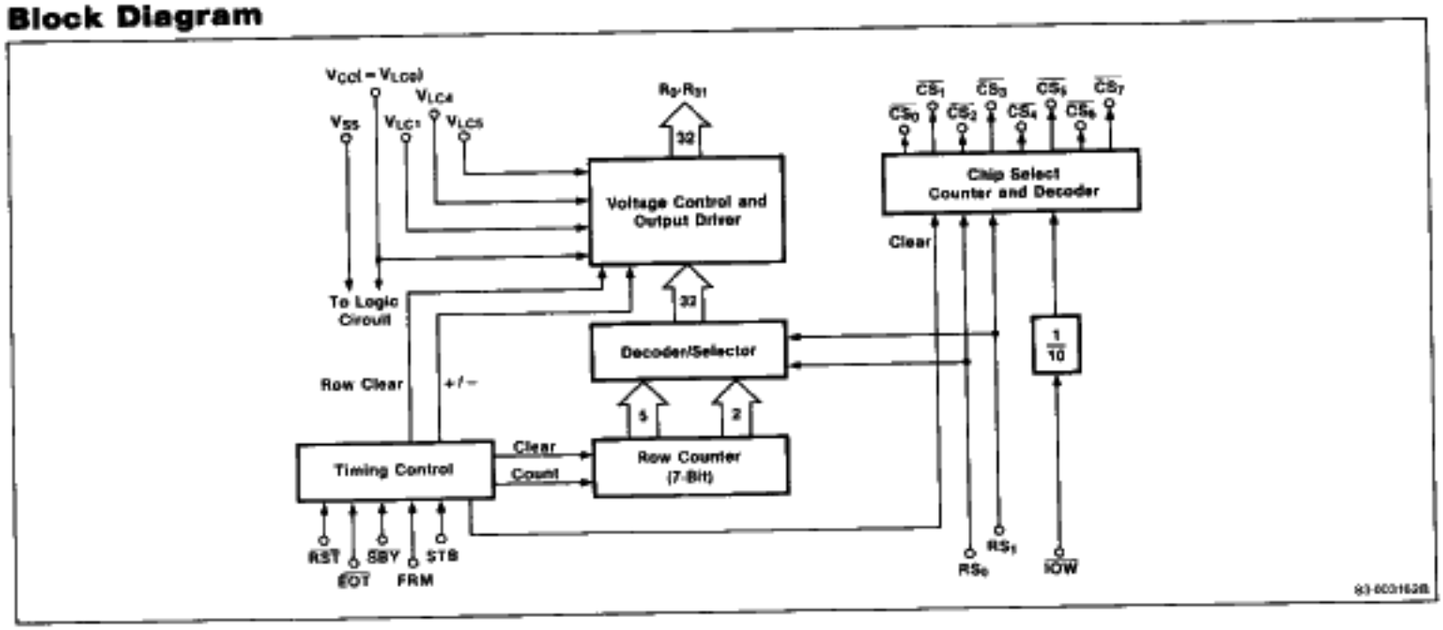
V_{CC} (= V_{LC0}) (Power Supply and LCD Drive Supply)

Connect the 5 V power supply between V_{CC} and V_{SS} for logic circuit operation. This pin is also used for the row drive voltage output.

V_{SS} (Ground)

Ground.

Block Diagram



Functional Description

Timing Control Circuit

This circuit controls the timing for each internal block. FRM, RS_0, RS_1, $\overline{RST}$, and $\overline{SBY}$ are sampled at the leading edge of STB, and then supplied to other internal circuits.

Row Counter Decoder/Select Circuit

As shown in figure 1, this circuit consists of a 7-bit counter, a comparator, and a 5 to 32 decoder. The 7-bit counter can accommodate 128 rows. The comparator acts to clear R_0-R_{31} if the upper two bits of the counter do not match RS_0 and RS_1. If they match, one of R_0-R_{31}, indicated by the lower five bits of the row counter, is selected and the rest are cleared. RS_0 and RS_1 allow for cascading as shown in table 1. Table 2 shows the row select logic.

Figure 1. Row Counter Decoder/Select Circuit

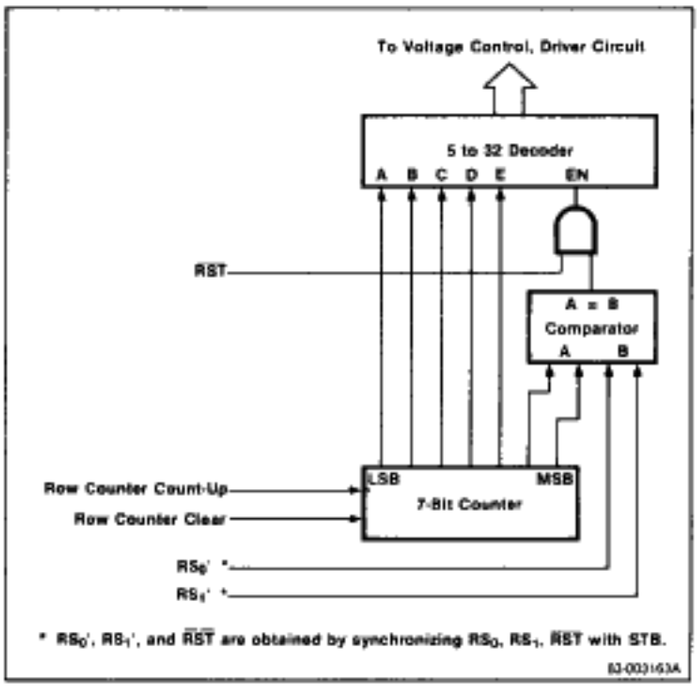


Table 1. RS_0 and RS_1 Row Cascading

RS_0	RS_1	Row Signal	Chip Select
0	0	R_0-R_{31}	$\overline{CS}_0$-$\overline{CS}_7$
0	1	R_{32}-R_{63}	$\overline{CS}_8$-$\overline{CS}_{15}$
1	0	R_{64}-R_{95}	$\overline{CS}_{16}$-$\overline{CS}_{23}$
1	1	R_{96}-R_{127}	$\overline{CS}_{24}$-$\overline{CS}_{31}$

Table 2. Row Select Logic

EN	E	D	C	B	A	Selected Row Signal
1	0	0	0	0	0	R_0
1	0	0	0	0	1	R_1
1	↓	↓	↓	↓	↓	R_n
1	1	1	1	1	0	R_{30}
1	1	1	1	1	1	R_{31}
0	X	X	X	X	X	None

Voltage Control Driver Circuit

This circuit generates the row signals for AC drive of the LCD panel. A low level $\overline{RST}$ clears the output. A low level $\overline{SBY}$ sets the output V_{LC0}. Table 2 shows the R_0-R_{31} output levels.

Table 2. R_0-R_{31} Outputs Levels

Function	+ (FRM = 1)	− (FRM = 0)
Select	V_{LC5}	V_{LC0}
Clear	V_{LC4}	V_{LC1}

Chip Select Counter/Decoder Circuit

This circuit, shown in figure 2, generates the column driver $\overline{CS}$ signal. This circuit has a 5-bit counter to generate up to 32 $\overline{CS}$ signals. The 5-bit counter is incremented once for every 10 $\overline{IOW}$ (active low) pulses. If the upper two bits of the chip select counter do not match RS_0 and RS_1, all the $\overline{CS}_0$-$\overline{CS}_7$ outputs are set to high level. If they match, one of $\overline{CS}_0$-$\overline{CS}_7$ (indicated by the lower three bits of the chip select counter) goes low. If $\overline{RST}$ is low, $\overline{CS}_0$-$\overline{CS}_7$ become high level. Table 3 shows the chip select logic.

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Figure 2. Chip Select Counter/Decoder Circuit

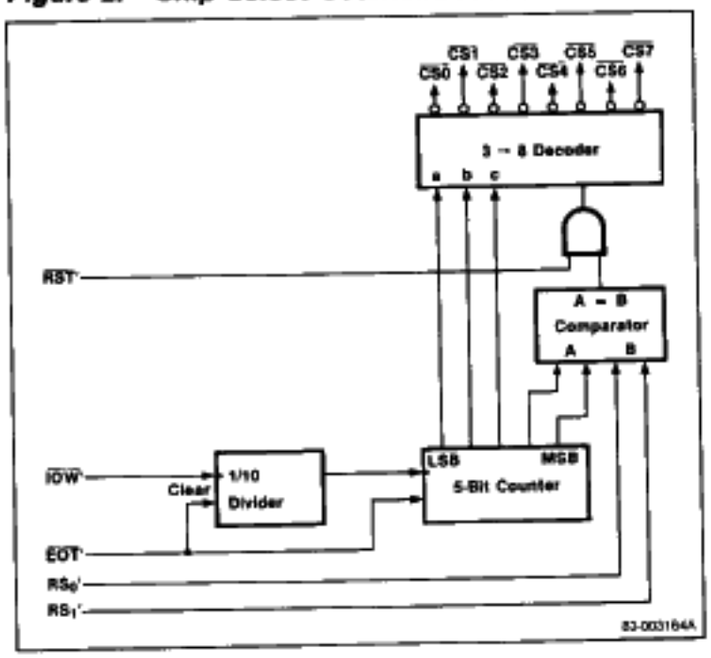

Table 3. Chip Select Logic

EN	c	b	a	Chip Select
1	0	0	0	$\overline{CS}_0$
1	0	0	1	$\overline{CS}_1$
1	0	1	0	$\overline{CS}_2$
1	0	1	1	$\overline{CS}_3$
1	1	0	0	$\overline{CS}_4$
1	1	0	1	$\overline{CS}_5$
1	1	1	0	$\overline{CS}_6$
1	1	1	1	$\overline{CS}_7$
0	X	X	X	Disabled