DATA SHEET

O K I A S I C P R O D U C T S

MSM13Q/14Q000
0.35 µm Sea of Gates Arrays

November 1999

Oki Semiconductor

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MSM13Q0000/14Q0000

0.35 µm Sea of Gates Arrays

DESCRIPTION

Oki's 0.3 5 µm ASIC products deliver ultra-high performance and high density at low power dissipation. The MSM13Q0000/14Q0000 series devices (referred to as "MSM13Q/14Q") are implemented with the industry-standard Cell-Based Array (CBA) architecture in a Sea-of-Gates (SOG) structure. Built in a 0.35 µm drawn CMOS technology (with an L-Effective of 0.27 µm), these SOG devices are available in three layers (MSM13Q) and four layers (MSM14Q) of metal. The semiconductor process is adapted from Oki's production-proven 64-Mbit DRAM manufacturing process.

The MSM13Q/14Q Series contains 6 arrays each, offering over 1 million raw gates and 352 I/O pads. Up to 66% and 90% of the raw gates can be used for the 3-layer and 4-layer arrays, respectively. Oki's 0.35 µm family is optimized for 3-V core operation with optimized 3-V I/O buffers and 5-V tolerant 3-V buffers. These SOG products are designed to fit the most popular plastic quad flat packs (QFPs), thin QFPs (TQFPs) , and plastic ball grid array (PBGA) packages.

The MSM13Q/14Q Series uses the popular CBA architecture from Silicon Architects of Synopsys which mixes two types of cells (8-transistor compute cells and 4-transistor drive cells) on the same die to deliver high gate density and high drives. The CBA is supported by a rich macro library, optimized for synthesis. Memory blocks are efficiently created by Oki's memory compilers to generate single- and dual-port RAM's in high-density and low-power configurations with synchronous RAM options.

As such, the MSM13Q/14Q series is well suited to memory-intensive designs with high production volumes approaching the real estate and cost savings of standard cells. At the same time, its SOG architecture allows rapid prototyping turnaround times. Thus, Oki's MSM13Q/14Q family offers the best of two worlds: quick prototyping of a gate array and low production cost of a standard cell.

Oki's 0.35 µm ASIC products are supported by leading-edge CAD tools including a synthesis-linked floorplanner, motive static timing analyzer, and H-clock tree methodology. They are further supported by specialized macrocells including phase-locked loop (PLL), pseudo-emitter coupled logic (PECL), peripheral component interconnect (PCI), universal synchronous receiver/transmitter (UART) cells, and ARM7TDMI RISC cores.

FEATURES

- 0.35 µm drawn 3- and 4-layer metal CMOS
- Optimized 3.3-V core
- Optimized 3-V I/O and 3-V I/O that is 5-V tolerant
- CBA SOG architecture
- Over 1.0M raw gates and 352 pads
- User-configurable I/O with V_{SS}, V_{DD}, TTL, 3-state, and 1- to 24-mA options
- Slew-rate-controlled outputs for low-radiated noise
- H-clock tree cells which reduce the maximum skew for clock signals
- User-configurable single and dual-port; synchronous or asynchronous memories
- Specialized macrocells including PLL, PECL, PCI, UART, and ARM7TDMI
- Floorplanning for front-end simulation, back-end layout controls, and link to synthesis
- Joint Test Action Group (JTAG) boundary scan and scan-path ATPG
- Support for popular CAE systems, including Cadence, IKOS, Mentor Graphics, Synopsys, Viewlogic, and Zycad

MSM13Q/14Q FAMILY LISTING

MSM13Q/14Q Series	PAD No.	Raw Gate (Gates)	Usable Gate M13Q(3LM)	Usable Gate M14Q(4LM)	Raw Gate	
					Row	Column
0150	144	157,192	105,319	143,045	196	802
0230	176	242,400	152,712	208,464	240	1,010
0340	208	346,176	204,244	276,941	288	1,202
0530	256	536,400	289,656	391,572	360	1,490
0840	320	847,048	415,054	567,522	452	1,874
1020	352	1,033,000	475,180	650,790	500	2,066

ARRAY ARCHITECTURE

The primary components of a 0.35 µm MSM13Q/14Q circuit include:

- I/O base cells
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (optimized 3-V I/O and 3-V I/O that is 5-V tolerant)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base modules containing three compute cells for each drive cell
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 24 dedicated corner pads for power and ground use during wafer probing, with 4 pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} and V_{SSO}).

The array architecture uses optimally sized transistors to efficiently implement logic and memory in a metal programmable technology. CBA uses two types of cells: compute cells and drive cells. The compute cell employs four PMOS and four NMOS trasnsistors whose sizes are optimized for logic and memory implementations as shown in *Figure 1*. The quantity and size of the transistors in a compute cell are carefully selected to maximize the efficiency of most commonly used functions in VLSI design. The drive cell consists of two large PMOS pull-up transistors and two large pull-down transistors. The compute and drive cells are tiled to create a channelless core array, with three comput cells for each drive cell as shown in *Figure 2*. The 3:1 ratio of compute to drive cells was selected for optimal implementation of emerging applications. Macrocells are created using either compute cells, drive cells, or combinations of compute and drive cells.

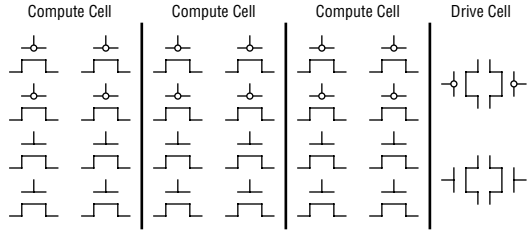


Figure 1. Base Cell Consisting of Three Compute Cells and One Drive Cell

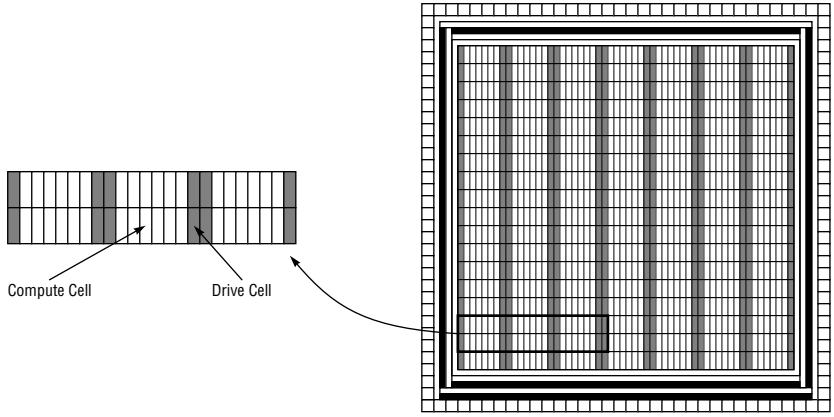


Figure 2. Core Array with Base Cell Mirrored Horizontally and Vertically

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0 V, T_j = 25°C) [1]

Parameter		Symbol	Conditions	Rated Value	Unit
Power supply voltage		V_{DD}		-0.3 to +4.6	V
Input voltage	Normal buffers	V_I		-0.3 to V_{DD}+0.3	V
	5-V tolerant	V_I		-0.3 to 6.0	
Output voltage	Normal buffers	V_O		-0.3 to V_{DD}+0.3	V
	5-V tolerant	V_O		-0.3 to 6.0	
Input current	Normal buffers	I_I		-10 to +10	mA
	5-V tolerant	I_I		-6 to +6	
Output current per I/O	Normal buffers	I_O	I_O = 1, 2, 4, 6, 8, 12, 24 mA	-24 to +24	mA
	5-V tolerant	I_O	I_O = 2, 4, 6, 8, 12 mA	-8 to +8	
Storage temperature		T_{stg}	–	-65 to +150	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions in the other specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rated Value	Unit
Power supply voltage	V_{DD} (3 V)	+3.0 to +3.6	V
Junction temperature	T_j	-40 to +85	°C

DC Characteristics (V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, T_j = -40°C to +85°C)

Parameter		Symbol	Conditions	Rated Value [1] Min.	Typ [2]	Max.	Unit
High-level input voltage	Normal buffer	V_{IH}		2.0	–	V_{DD} + 0.3	V
	5-V tolerant	V_{IH}		2.0	–	5.5	
Low-level input voltage	Normal buffer	V_{IL}	TTL input	-0.3	–	0.8	
	5-V tolerant	V_{IL}	TTL input	-0.3	–	0.8	
TTL- level Schmitt trigger input threshold voltage	Normal buffer	V_{t+}	TTL input	–	1.5	2.0	
		V_{t-}		0.7	1.0	–	
		ΔV_t	V_{t+} - V_{t-}	0.4	0.5	–	
	5-V tolerant	V_{t+}	TTL 5-V tolerant input	–	1.5	2.0	
		V_{t-}		0.7	1.0	–	
		ΔV_t	V_{t+} - V_{t-}	0.4	0.5	–	
High-level output voltage	Normal buffer	V_{OH}	I_{OH} = -100 µA	V_{DD} - 0.2	–	–	
			I_{OH} = -1, -2, -4, -6, -8, -12, -24 mA	2.4	–	–	
	5-V tolerant	V_{OH}	I_{OH} = -100 µA	V_{DD} - 0.2	–	–	
			I_{OH} = -1, -2, -4, -6, -8, -12 mA	2.4	–	–	
Low-level output voltage	Normal buffer	V_{OL}	I_{OL} = 100 µA	–	–	0.2	
			I_{OL} = 1, 2, 4, 6, 8, 12, 24mA	–	–	0.4	
	5-V tolerant	V_{OL}	I_{OL} = 100 µA	–	–	0.2	
			I_{OL} = 1, 2, 4, 6, 8, 12 mA	–	–	0.4	
High-level input current	Normal buffer	**I_{IH}**	V_{IH} = V_{DD}	–	0.1	10	µA
			V_{IH} = V_{DD} (50-kΩ pull-down)	10	66	200	
	5-V tolerant	I_{IH}	V_{IH} = V_{DD}	–	0.1	10	
			V_{IH} = V_{DD} (50-kΩ pull-down)	10	66	200	
Low-level input current	Normal buffer	I_{IL}	V_{IL} = V_{SS}	-10	-0.1	-	
			V_{IL} = V_{SS} (50-kΩ pull-up)	-200	-66	-10	
			V_{IL} = V_{SS} (3-kΩ pull-up)	-3.3	-1.1	-0.3	mA
	5-V tolerant	I_{IL}	V_{IL} = V_{SS}	-10	-0.1	–	µA
3-state output leakage current	Normal buffer	I_{OZH}	V_{OH} = V_{DD}	–	0.1	10	µA
			V_{OH} = V_{DD} (50-kΩ pull-down)	10	-66	200	
		I_{OZL}	V_{OL} = V_{SS}	-10	-0.1	–	
			V_{OL} = V_{SS} (50-kΩ pull-up)	-200	-66	-10	
			V_{OL} = V_{SS} (3-kΩ pull-up)	-3.3	-1.1	-0.3	mA
	5-V tolerant	I_{OZH}	V_{OH} = V_{DD}	–	0.1	10	µA
			V_{OH} = V_{DD} (50-kΩ pull-down)	10	66	200	
		I_{OZL}	V_{OL} = V_{SS}	-10	-0.1	–	
Stand-by current [3]		I_{DDQ}	Output open, V_{IH} = V_{DD}, V_{IL} = V_{SS}	Design Dependent			µA

1. JEDEC Compatible; JESD8-1A LVTTL.
2. Typical condition is V_{DD} = 3.3 V and T_j = 25°C on a typical process.
3. RAM/ROM should be in powerdown mode.

AC Characteristics (V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25°C)

Parameter		Driving Type	Conditions [1] [2]	Rated Value [3]	Unit
Internal gate propagation delay	Inverter	1X	F/O = 2, L = 0 mm V_{DD} = 3.3 V	0.082	ns
		2X		0.068	
		4X		0.062	
	2-input NAND	1X		0.14	
		2X		0.13	
	2-input NOR	1X		0.16	
		2X		0.14	
	Inverter	1X	F/O = 2, L = 1 mm V_{DD} = 3.3 V	0.19	
		2X		0.13	
		4X		0.097	
	2-input NAND	1X		0.28	
		2X		0.20	
	2-input NOR	1X		0.34	
		2X		0.24	
Toggle frequency			F/O= 1, L = 0 mm	1040	MHz
Input buffer propagation delay	TTL level normal input buffer		F/O = 2,L = 1 mm	0.35	ns
	TTL level 5-V tolerant buffer			0.64	
Output buffer propagation delay	Push-pull Normal output buffer	4 mA	CL = 20pF	2.15	
		8 mA	CL= 50 pF	2.25	
		12 mA	CL = 100 pF	2.82	
	3-state 5-V tolerant buffer	4 mA	CL = 20 pF	2.41	
Output buffer transition times [4]	Push-pull Normal output buffer	12 mA	CL = 100 pF	4.68 (r) 3.48 (f)	
	3-state 5-V tolerant buffer	4 mA	CL = 20 pF	3.53 (r) 3.24 (f)	

1. Input transition time in 0.2 ns / 3.3 V.
2. Typical condition is V_{DD} = 3.3 V and T_j = 25°C.
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.
4. Output rising and falling times are both specified over a 10 to 90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells and macrofunctions, ranging from simple hard macrocells for basic Boolean operations to large, user-parameterizable macrofunctions. The following figure illustrates the main classes of macrocells and macrofunctions available.

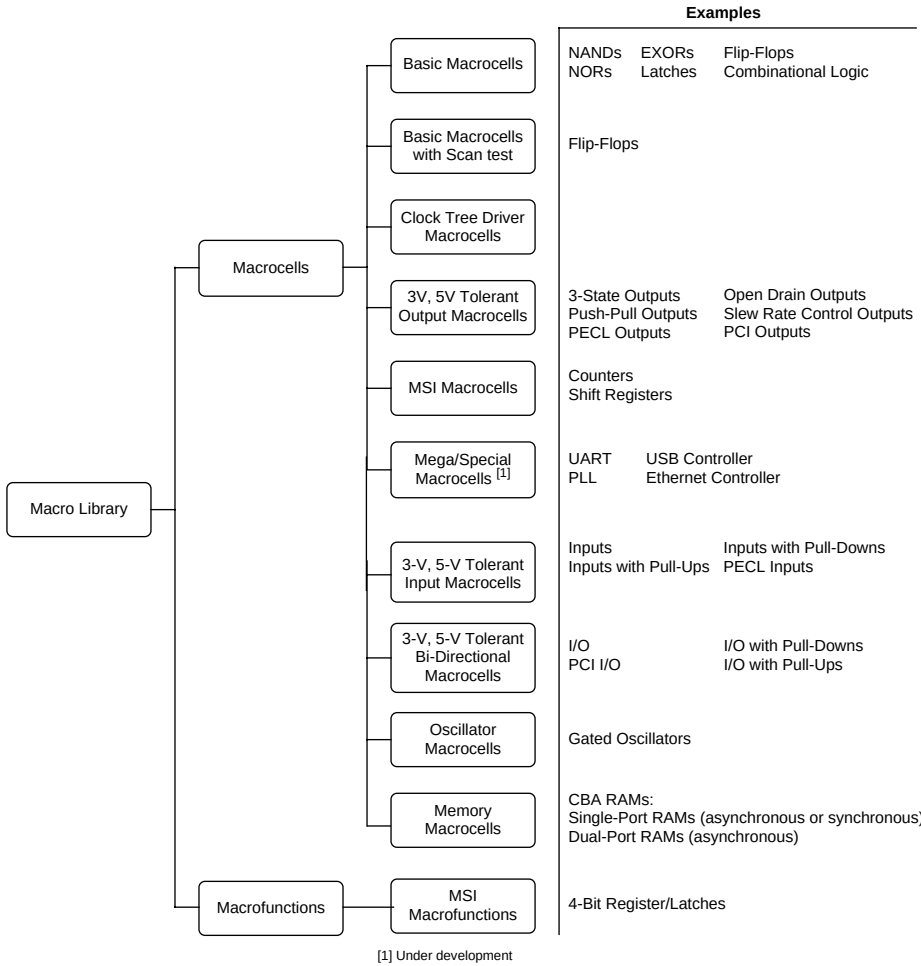


Figure 3. Oki Macrocell and Macrofunction Library

Macrocells for Driving Clock Trees

Oki offers H-clock-tree drivers that minimize clock skew. The advanced layout software uses dynamic driver placement and sub-trunk allocation to optimize the clock-tree implementation for a particular circuit. Features of the H-clock-tree driver-macrocells include:

- True RC back annotation of the clock network
- Automatic fan-out balancing
- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Automatic branch length minimization
- Dynamic driver placement
- Allows multiple clock trees

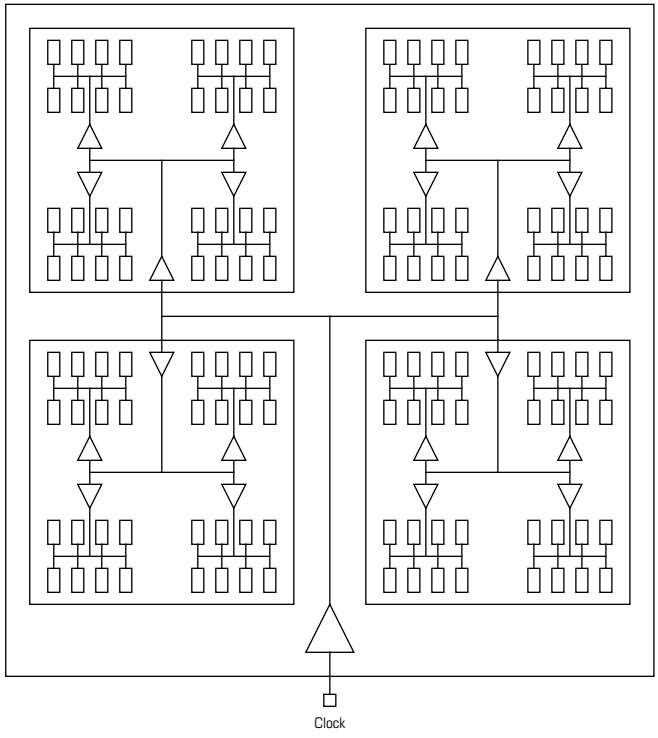


Figure 4. H-Clock-Tree Structure

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation, back-end layout control, and link to synthesis
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements (in development)

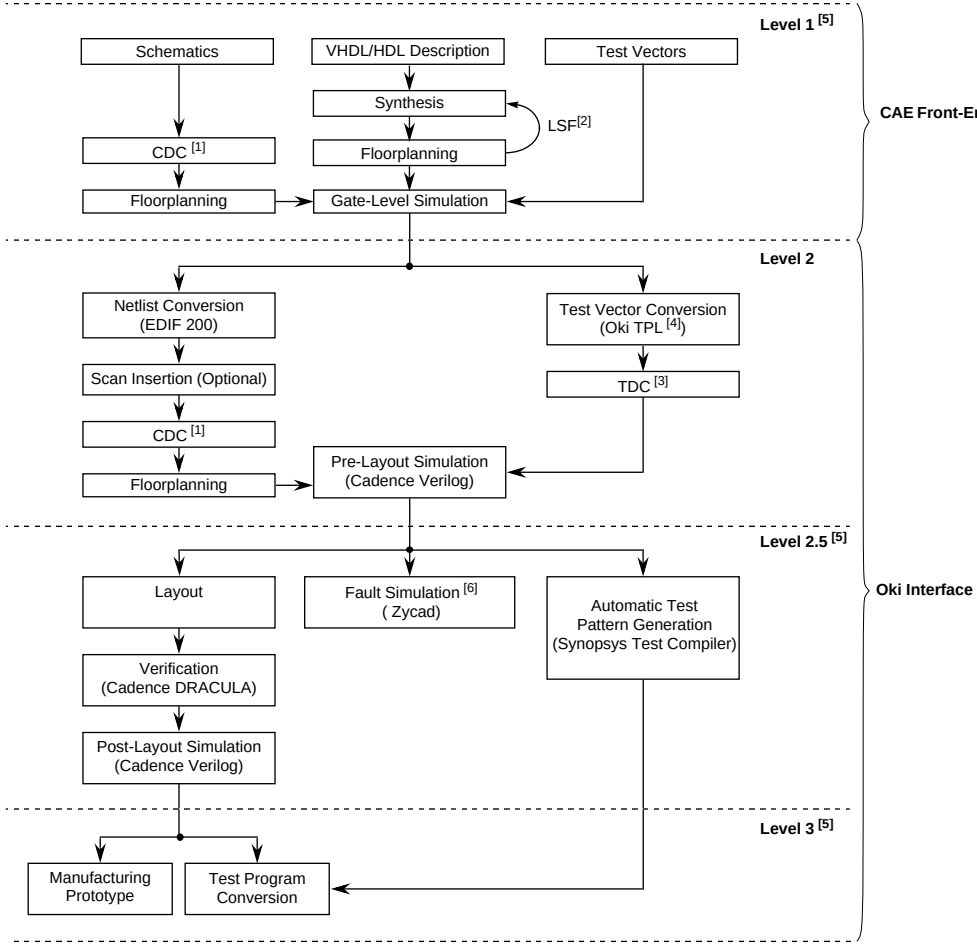
Table 1: CAD Design Tools

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	HP9000, 7xx IBM RS6000 Sun® [2]	HP-UX AIX SunOS, Solaris	Composer™ Verilog™ Veritime™ Verifault™ Synergy™ Concept™ [3] Leapfrog™	Design capture Simulation Timing analysis Fault grading Design synthesis Design capture VHDL simulation
IKOS	HP9000, 7xx, Sun [2]	HP-UX, SunOS, Solaris	NSIM Gemini/Voyager	Simulation
Mentor Graphics™	HP9000, 7xx Sun [2]	HP-UX SunOS, Solaris	IDEA™ QuickVHDL QuickSim II™ QuickPath™ QuickFault™ QuickGrade™ AutoLogic™ DFT Advisor	Design capture VHDL simulation Logic simulation Timing analysis Fault grading Fault grading Design synthesis Test synthesis
Synopsys (Interface to Mentor Graphics, VIEWLogic)	IBM RS6000 HP9000, 7xx Sun [2]	AIX HP-UX SunOS, Solaris	Design Compiler™ HDL/VHDL Compiler™ Test Compiler™ VSS™	Compilation Design synthesis Test synthesis VHDL simulation
Model Technology, Inc. (MTI)	HP9000, 7xx Sun [2] PC	HP-UX SunOS, Solaris. Win95/NT™	V-System	VHDL Simulation
VIEWLogic	PC Sun [2]	Windows™, Windows NT™ SunOS, Solaris	Workview Office™ Powerview™ Vantage Optium Motive ViewSim™ with VSO	Design capture Simulation VHDL simulation Timing analysis Design synthesis Simulation

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.
3. Sun and HP platform only.

Design Process

The following figure illustrates the overall IC design process and shows the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check (CDC) program verifies logic design rules.
[2] Oki's Link to Synthesis Floorplanning (LSF) toolset transfers post-floorplanning timing for resynthesis.
[3] Oki's Test Data Check (TDC) program verifies test vector rules.
[4] Oki's Test Pattern Language (TPL).
[5] Alternate Customer-Oki design interfaces available in addition to standard level 2.
[6] Standard design process includes fault simulation.

Figure 5. Oki's Design Process

Automatic Test Pattern Generation

Oki's 0.35 µm ASIC technologies support Automatic Test Pattern Generation (ATPG) using full scan-path design techniques, including the following:

- Increases fault coverage ≥95%
- Uses Synopsys Test Compiler
- Inserts scan structures automatically
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

ATPG methodology is described in detail in Oki's *0.35 µm Scan Path Application Note*.

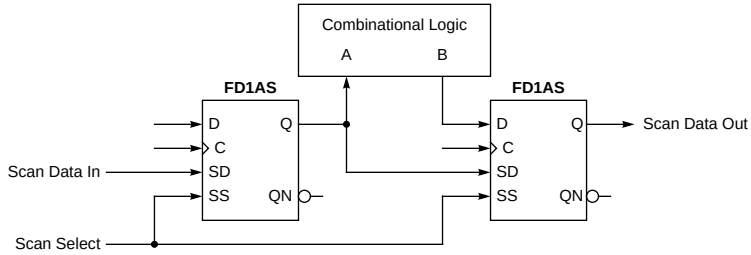


Figure 6. Full Scan Path Configuration

Floorplanning Design Flow

Oki offers three floorplanning tools for high-density ASIC design. The two main purposes for Oki's floorplanning tool are to:

- Ensure conformance of critical circuit performance specifications
- Shorten overall design turnaround time (TAT)

The supported floorplanners are: Cadence DP3, Gambit GFP, and Oki's internal floorplanner.

In a traditional design approach with synthesis tools, timing violations after prelayout simulation are fixed by manual editing of the netlist. This process is difficult and time consuming. Also, there is no physical cluster information provided in the synthesis tool, and so it is difficult to synthesize logic using predicted interconnection delay due to wire length. Therefore, synthesis tools may create over-optimized results.

To minimize these problems, Synopsys proposed a methodology called Links to Layout (LTL). Based on this methodology, Oki developed an interface between Oki's floorplanners and the Synopsys environment, called Link Synopsys to Floorplanner (LSF). Because not all Synopsys users have access to the Synopsys Floorplan Management tool, Oki developed the LSF system to support both users who can access

Synopsys Floorplan Management and users who do not have access to Synopsys Floorplan Management.

More information on OKI's floorplanning capabilities is available in Oki's Application Note, *Using Oki's Floorplanner: Standalone Operation and Links to Synopsys*.

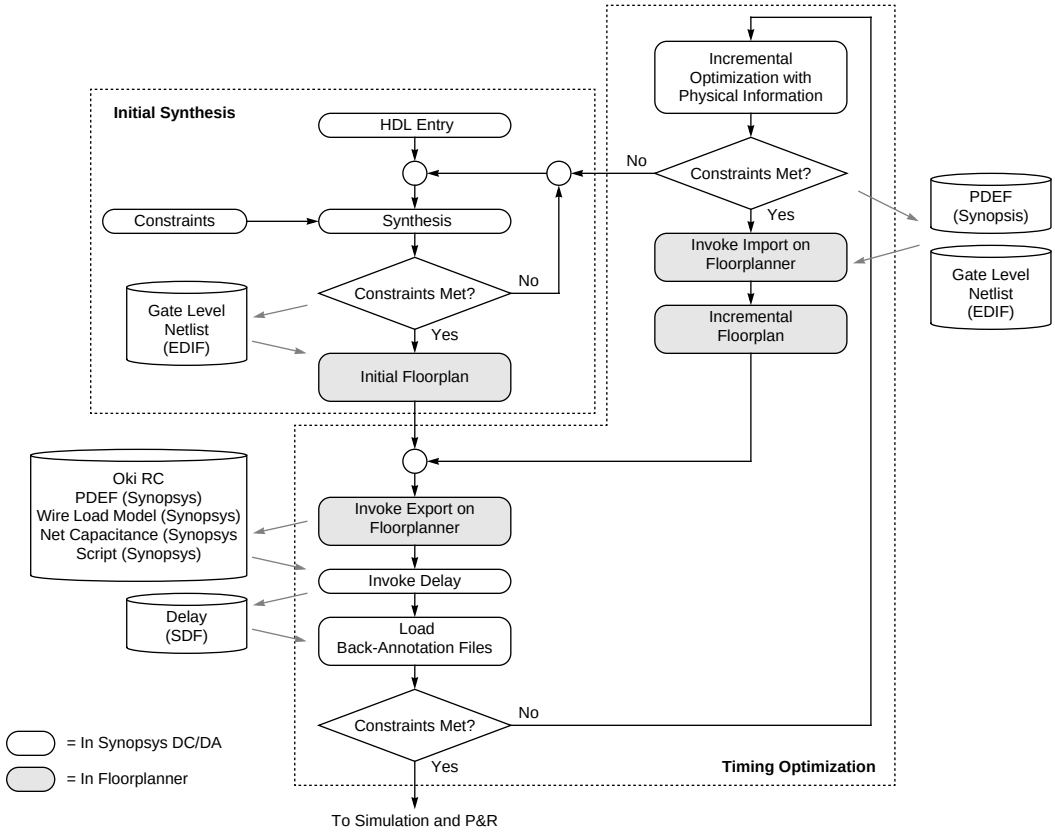


Figure 7. LSF System Design Flow

IEEE JTAG Boundary Scan Support

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note.* (Contact the Oki Application Engineering Department for interface options.)

PACKAGE OPTIONS

TQFP & LQFP Package Menu

Base Array MSM…	I/O Pads [1]	TQFP			LQFP		
		64	80	100	144	176	208
13Q/14Q0150	144	●	●	●	●		
13Q/14Q0230	176	●	●	●	●	●	
13Q/14Q0340	208	●	●	●	●	●	●
13Q/14Q0530	256		●	●	●	❍	●
13Q/14Q0840	320			●	❍	●	●
13Q/14Q1020	352				❍	●	●
Body Size (mm)		10 x 10	12 x 12	14 x 14	20 x 20	24 x 24	28 x 28
Lead Pitch (mm)		0.5	0.5	0.5	0.5	0.5	0.5

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

PQFP Package Menu

Base Array MSM…	I/O Pads [1]	PQFP (42 Alloy)		PQFP (Cu-Alloy)	
		128	160	208	240
13Q/14Q0150	144	❍			
13Q/14Q0230	176	❍	❍		
13Q/14Q0340	208	●	●		
13Q/14Q0530	256	●	●	●	
13Q/14Q0840	320	●	●	●	❍
13Q/14Q1020	352	❍	●	●	❍
Body Size (mm)		28 x 28	28 x 28	28 x 28	32 x 32
Lead Pitch (mm)		0.80	0.65	0.50	0.50

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

BGA Package Menu

Base Array MSM…	I/O Pads [1]	256	352
13Q/14Q0150	144		
13Q/14Q0230	176	●	
13Q/14Q0340	208	●	
13Q/14Q0530	256	●	
13Q/14Q0840	320	●	●
13Q/14Q1020	352	●	●
Body Size (mm)		27 x 27	35 x 35
Ball Pitch (mm)		1.27	1.27

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

Notes:

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

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