Ordering number : ENN7498

Monolithic Digital IC

LB11923V

Three-Phase Brushless Motor Driver

Overview

The LB11923V is a pre-driver IC designed for variable-speed control of 3-phase brushless motors. It can be used to implement a motor drive circuit with the desired output capacity (voltage, current) by using discrete transistors for the output stage. It implements direct PWM drive for minimal power loss. Since the LB11923V includes a built-in VCO circuit, applications can control the motor speed arbitrarily by varying the external clock frequency.

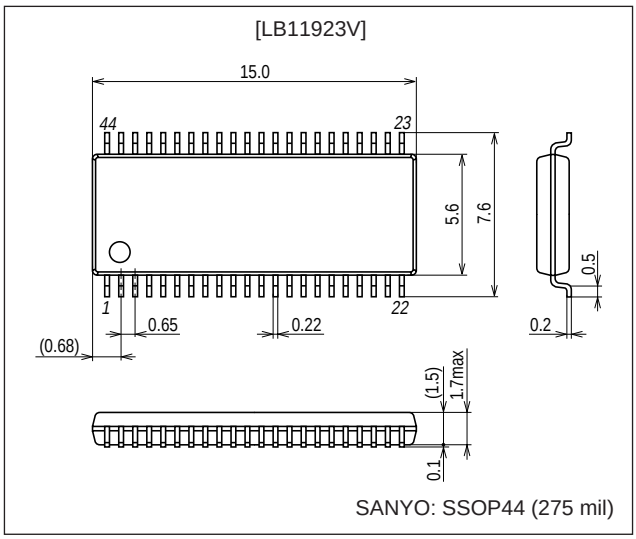
Features

- Direct PWM drive output
- Speed discriminator + PLL speed control circuit
- Speed lock detection output
- Built-in crystal oscillator circuit
- Forward/reverse switching circuit
- Braking circuit (short braking)
- Full complement of on-chip protection circuits, including lock protection, current limiter, and thermal shutdown protection circuits.

Package Dimensions

unit: mm

3277-SSOP44



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		8	V
Maximum input current	I_{REG} max	V_{REG} pin	2	mA
Output current	I_O max	UH, VH, WH, UL, VL, and WL outputs	30	mA
Allowable power dissipation 1	Pd max1	Independent IC	0.62	W
Allowable power dissipation 2	Pd max2	When mounted on the specified PCB (114.3 × 76.1 × 1.6 mm glass epoxy PCB)	1.79	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		4.4 to 7.0	V
Input current range	I_{REG}	V_{REG} pin (7 V)	0.2 to 1.5	mA
FG Schmitt output applied voltage	V_{FGS}		0 to 7	V
FG Schmitt output current	I_{FGS}		0 to 5	mA
Lock detection applied voltage	V_{LD}		0 to 7	V
Lock detection output current	I_{LD}		0 to 20	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 6.3 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	$I_{CC}1$			21	29.5	mA
	$I_{CC}2$	In stop mode		2.3	3.3	mA
	$I_{CC}3$	V_{CC} = 5 V		20	28	mA
	$I_{CC}4$	V_{CC} = 5 V, In stop mode		2.1	2.9	mA
Output saturation voltage 1-1	V_O sat1-1	At low level: I_O = 400 µA		0.1	0.3	V
Output saturation voltage 1-2	V_O sat1-2	At low level: I_O = 10 mA		0.8	1.2	V
Output saturation voltage 2	V_O sat2	At high level: I_O = –20 mA	V_{CC} – 1.2	V_{CC} – 0.9		V
[Hall Amplifier]						
Input bias current	$I_{HB(HA)}$		–2	–0.1		µA
Common-mode input voltage range 1	$V_{ICM}1$	When Hall-effect sensors are used	0.5		V_{CC} – 2.0	V
Common-mode input voltage range 2	$V_{ICM}2$	When one-side biased inputs are used (Hall-effect IC applications)	0		V_{CC}	V
Hall input sensitivity		Sine wave	100			mVp-p
Hysteresis	$\Delta V_{IN(HA)}$		25	35	52	mV
Input voltage low → high	V_{SLH}		9	17	29	mV
Input voltage high → low	V_{SHL}		–29	–18	–9	mV
[PWM Oscillator]						
Output high-level voltage 1	$V_{OH(PWM)}1$		3.5	3.8	4.1	V
Output high-level voltage 2	$V_{OH(PWM)}2$	V_{CC} = 5 V	2.75	3.0	3.25	V
Output low-level voltage 1	$V_{OL(PWM)}1$		1.8	2.1	2.4	V
Output low-level voltage 2	$V_{OL(PWM)}2$	V_{CC} = 5 V	1.45	1.65	1.9	V
Oscillator frequency	$f_{(PWM)}$	C = 560 pF		22		kHz
Amplitude 1	$V_{(PWM)}1$		1.4	1.7	2.0	Vp-p
Amplitude 2	$V_{(PWM)}2$	V_{CC} = 5 V	1.1	1.35	1.6	Vp-p
[CSD Oscillator]						
Output high-level voltage 1	$V_{OH(CSD)}1$		3.95	4.4	4.85	V
Output high-level voltage 2	$V_{OH(CSD)}2$	V_{CC} = 5 V	3.15	3.5	3.85	V
Output low-level voltage 1	$V_{OL(CSD)}1$		1.1	1.4	1.7	V
Output low-level voltage 2	$V_{OL(CSD)}2$	V_{CC} = 5 V	0.9	1.1	1.3	V
External capacitor charge current	$I_{CHG}1$		–13	–9	–6	µA
External capacitor discharge current	$I_{CHG}2$		8	12	16	µA
Oscillator frequency	$f_{(RK)}$	C = 0.068 µF		22		Hz
Amplitude 1	$V_{(RK)}1$		2.65	3.0	3.35	Vp-p
Amplitude 2	$V_{(RK)}2$	V_{CC} = 5 V	2.1	2.4	2.65	Vp-p
[VCO Oscillator C pin]						
Output high-level voltage 1	$V_{OH(C)}1$		2.10	2.40	2.65	V
Output high-level voltage 2	$V_{OH(C)}2$	V_{CC} = 5 V	2.00	2.30	2.55	V
Output low-level voltage 1	$V_{OL(C)}1$		1.60	1.90	2.10	V
Output low-level voltage 2	$V_{OL(C)}2$	V_{CC} = 5 V	1.55	1.80	2.05	V
Oscillator frequency	$f_{(C)}$				1.0	MHz
Amplitude 1	$V_{(C)}1$		0.3	0.5	0.7	Vp-p
Amplitude 2	$V_{(C)}2$	V_{CC} = 5 V	0.3	0.5	0.7	Vp-p

*Note: Not tested

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current Limiter Operation]						
Limiter	V_{RF}		0.235	0.260	0.285	V
[Thermal Shutdown Operation]						
Thermal shutdown operating temperature	TTSD	Design target value *	150	180		°C
Hysteresis	ΔTSD	Design target value *		30		°C
[V_{REG} Pin]						
V_{REG} pin voltage	V_{REG}	I = 500 μA	6.6	7.0	7.4	V
[Low-voltage Protection Circuit]						
Operating voltage	V_{SDL}		3.55	3.75	4.00	V
Release voltage	V_{SDH}		3.85	4.03	4.25	V
Hysteresis	ΔVSD		0.18	0.28	0.38	V
[FG Amplifier]						
Input offset voltage	$V_{IO(FG)}$		–10		+10	mV
Input bias current	$I_{B(FG)}$		–1		+1	μA
Output high-level voltage 1	$V_{OH(FG)}1$	IFGI = –0.1 mA, No load	4.2	4.6	5.0	V
Output high-level voltage 2	$V_{OH(FG)}2$	IFGI = –0.1 mA, No load, V_{CC} = 5 V	3.6	3.95	4.3	V
Output low-level voltage 1	$V_{OL(FG)}1$	IFGI = 0.1 mA, No load	1.3	1.7	2.1	V
Output low-level voltage 2	$V_{OL(FG)}2$	IFGI = 0.1 mA, No load, V_{CC} = 5 V	0.7	1.05	1.4	V
FG input sensitivity		Gain: 100×	3			mV
Schmitt amplitude for the next stage			100	180	250	mV
Operating frequency range					2	kHz
Open-loop gain		$f_{(FG)}$ = 2 kHz	45	51		dB
Reference voltage	$V_{B(FG)}$		–5%	V_{CC}/2	5%	V
[FGS Output]						
Output saturation voltage	$V_{O(FGS)}$	$I_{O(FGS)}$ = 2 mA		0.2	0.4	V
Output leakage current	$I_{L(FGS)}$	V_O = V_{CC}			10	μA
[Speed Discriminator Output]						
Output high-level voltage	$V_{OH(D)}$		V_{CC} – 1.0	V_{CC} – 0.7		V
Output low-level voltage	$V_{OL(D)}$			0.8	1.1	V
[Speed Control PLL Output]						
Output high-level voltage	$V_{OH(P)}1$		4.05	4.30	4.65	V
	$V_{OH(P)}2$	V_{CC} = 5 V	3.25	3.50	3.85	V
Output low-level voltage	$V_{OL(P)}1$		1.85	2.15	2.45	V
	$V_{OL(P)}2$	V_{CC} = 5 V	1.25	1.60	1.85	V
[Lock Detection]						
Output saturation voltage	$V_{OL(LD)}$	I_{LD} = 10 mA		0.25	0.4	V
Output leakage current	$I_{L(LD)}$	V_O = V_{CC}			10	μA
Lock range			–6.25		+6.25	%
[Integrator]						
Input offset voltage	$V_{IO(INT)}$		–10		+10	mV
Input bias current	$I_{B(INT)}$		–0.4		+0.4	μA
Output high-level voltage 1	$V_{OH(INT)}1$	IINTI = –0.1 mA, No load	4.1	4.4	4.7	V
Output high-level voltage 2	$V_{OH(INT)}2$	IINTI = –0.1 mA, No load, V_{CC} = 5 V	3.45	3.7	3.95	V
Output low-level voltage 1	$V_{OL(INT)}1$	IINTI = 0.1 mA, No load	1.2	1.4	1.65	V
Output low-level voltage 2	$V_{OL(INT)}2$	IINTI = 0.1 mA, No load, V_{CC} = 5 V	1.1	1.3	1.5	V
Open-loop gain			45	51		dB
Gain-bandwidth product		Design target value *		1.0		MHz
Reference voltage	$V_{B(INT)}$		–5%	V_{CC}/2	5%	V
[FIL Output]						
Output source current	$I_{OH(FIL)}$		–17	–13	–7	μA
Output sink current	$I_{OL(FIL)}$		7	12	17	μA

*Note: Not tested

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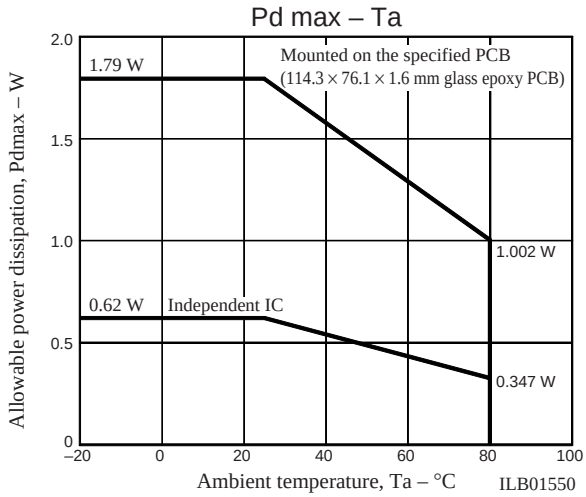
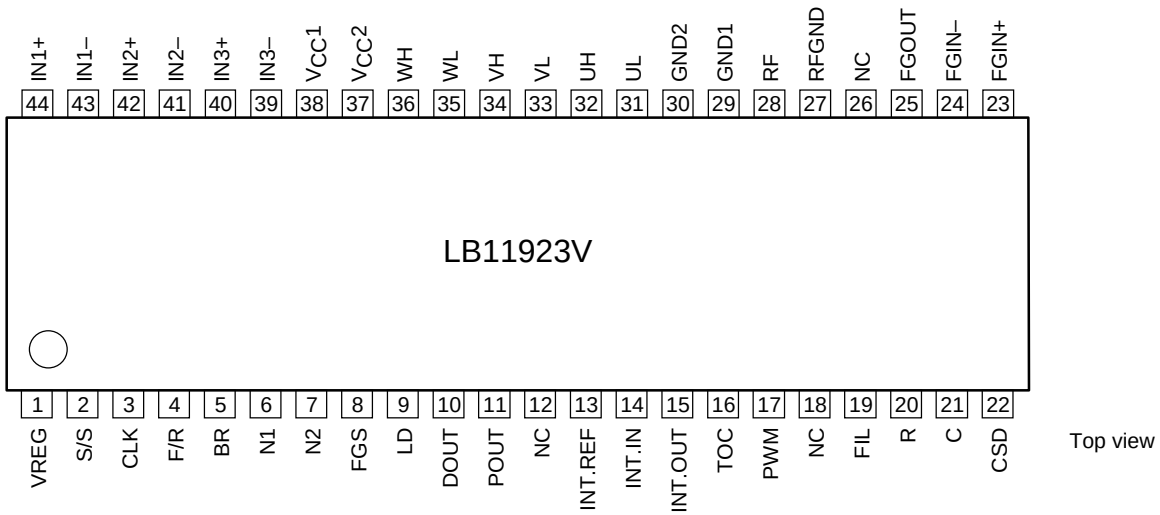
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[S/S Pin]						
Input high-level voltage	$V_{IH(S/S)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(S/S)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(S/S)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(S/S)}$	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
Input high-level current	$I_{IH(S/S)}$	$V_{S/S} = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(S/S)}$	$V_{S/S}$ = 0 V	–170	–118		µA
Pull-up resistance	$R_{U(S/S)}$		37	53.5	70	kΩ
[F/R Pin]						
Input high-level voltage	$V_{IH(F/R)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(F/R)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(F/R)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(F/R)}$	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
Input high-level current	$I_{IH(F/R)}$	$V_{F/R} = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(F/R)}$	$V_{F/R}$ = 0 V	–170	–118		µA
Pull-up resistance	$R_{U(F/R)}$		37	53.5	70	kΩ
[BR Pin]						
Input high-level voltage	$V_{IH(BR)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(BR)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(BR)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(BR)}$	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
Input high-level current	$I_{IH(BR)}$	$V_{BR} = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(BR)}$	V_{BR} = 0 V	–170	–118		µA
Pull-up resistance	$R_{U(BR)}$		37	53.5	70	kΩ
[CLK Pin]						
Input high-level voltage	$V_{IH(CLK)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(CLK)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(CLK)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(CLK)}$	V_{CC} = 6.3 V, 5 V, design target value *	0.13	0.22	0.31	V
Input high-level current	$I_{IH(CLK)}$	$V_{CLK} = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(CLK)}$	V_{CLK} = 0 V	–170	–118		µA
Input frequency	$f_{(CLK)}$				3.9	kHz
Pull-up resistance	$R_{U(CLK)}$		37	53.5	70	kΩ
[N1 Pin]						
Input high-level voltage	$V_{IH(N1)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(N1)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(N1)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(N1)}$	V_{CC} = 6.3 V, 5 V, design target value *	0.13	0.22	0.31	V
Input high-level current	$I_{IH(N1)}$	$V_{N}1 = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(N1)}$	$V_{N}1$ = 0 V	–170	–118		µA
Pull-up resistance	$R_{U(N1)}$		37	53.5	70	kΩ
[N2 Pin]						
Input high-level voltage	$V_{IH(N2)}$	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
Input low-level voltage	$V_{IL(N2)}$	V_{CC} = 6.3 V, 5 V	0		1.0	V
Input open voltage	$V_{IO(N2)}$		V_{CC} – 0.5		V_{CC}	V
Hysteresis	$\Delta V_{IN(N2)}$	V_{CC} = 6.3 V, 5 V, design target value *	0.13	0.22	0.31	V
Input high-level current	$I_{IH(N2)}$	$V_{N}2 = V_{CC}$	–10	0	+10	µA
Input low-level current	$I_{IL(N2)}$	$V_{N}2$ = 0 V	–170	–118		µA
Pull-up resistance	$R_{U(N2)}$		37	53.5	70	kΩ

*Note: Not tested



Pin Assignment



Speed Discriminator Count and VCO Divisor

N1	N2	Count	Divisor
High or open	High or open	1024	1024
High or open	Low	1024	512
Low	High or open	256	256
Low	Low	512	512

$f_{FG} = (\text{divisor} \div \text{count}) \times f_{CLK}$

Three-Phase Logic Truth Table (A high (H) input is the state where $IN^+ > IN^-$.)

Item	F / R = L			F / R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	—
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

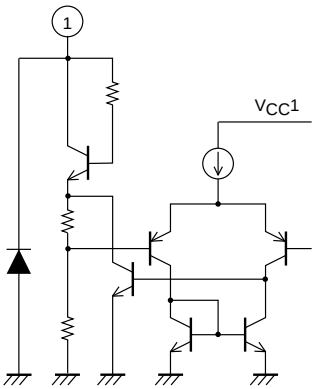
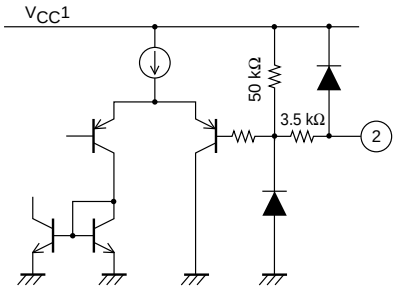
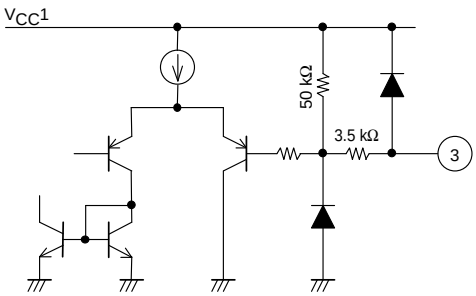
S/S Pin

High or open	Stop
Low	Start

BRK Pin

High or open	Brake
Low	Released

Pin Functions

Pin No.	Pin	Functions	Equivalent circuit
1	VREG	7-V shunt regulator output	
2	S/S	Start/stop control Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. Low for start. High or open for stop. The hysteresis is about 0.22 V.	
3	CLK	External clock signal input Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. The hysteresis is about 0.22 V. f = 16 kHz, maximum	

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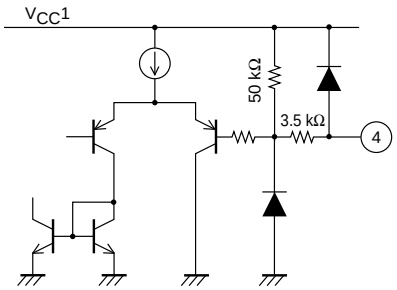
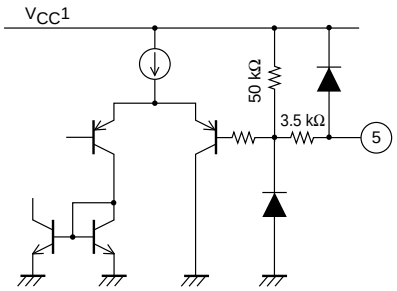
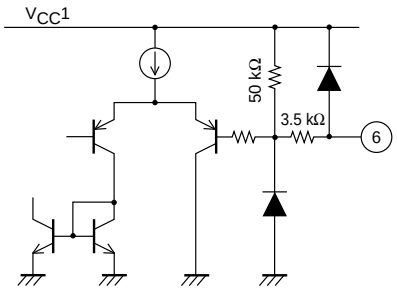
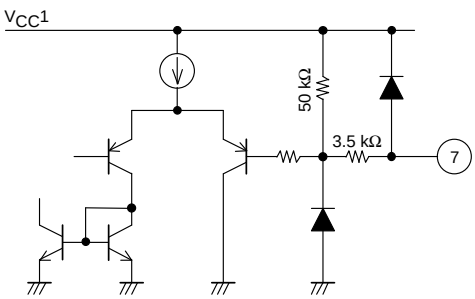
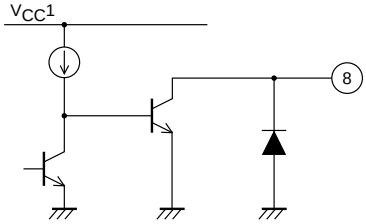
Pin No.	Pin	Functions	Equivalent circuit
4	F/R	Forward/reverse control Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. Low for forward. High or open for reverse. The hysteresis is about 0.22 V.	
5	BR	Brake control (short braking operation) Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. High or open for brake mode operation. The hysteresis is about 0.22 V.	
6	N1	Switches the speed discriminator VCO divisor count. Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. The hysteresis is about 0.22 V.	
7	N2	The speed discriminator count switching. Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. The hysteresis is about 0.22 V.	
8	FGS	FG amplifier output (after the Schmitt circuit) This is an open collector output.	

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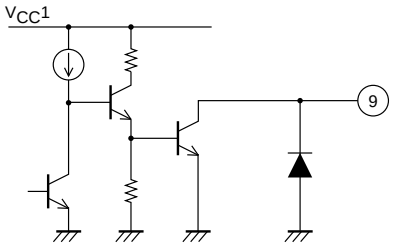
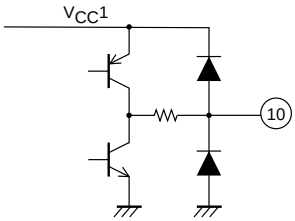
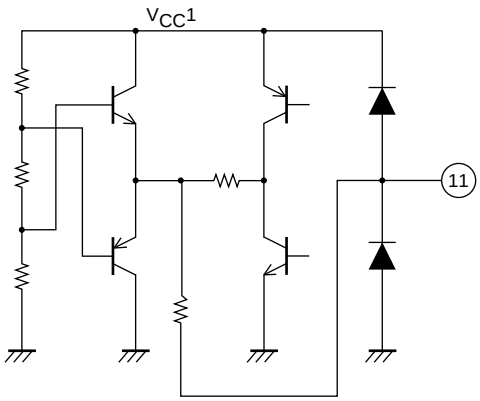
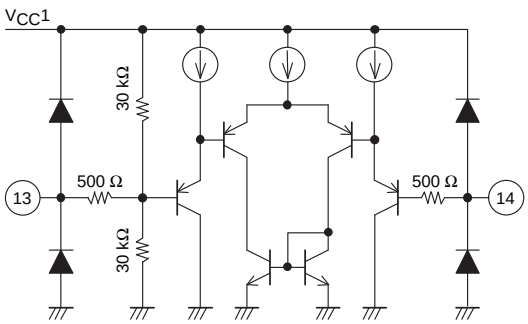
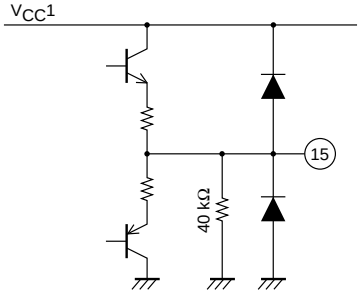
Pin No.	Pin	Functions	Equivalent circuit
9	LD	Speed lock detection output This is an open collector output. Goes low when the motor speed is within the speed lock range (±6.25%).	
10	DOUT	Speed discriminator output Acceleration → high, deceleration → low	
11	POUT	Speed control system PLL output Outputs the phase comparison result for CLK and FG.	
13	INT REF	Integrating amplifier non-inverting input (1/2 V_{CC} potential)	
14	INT IN	Integrating amplifier inverting input	
15	INT OUT	Integrating amplifier output (speed control)	

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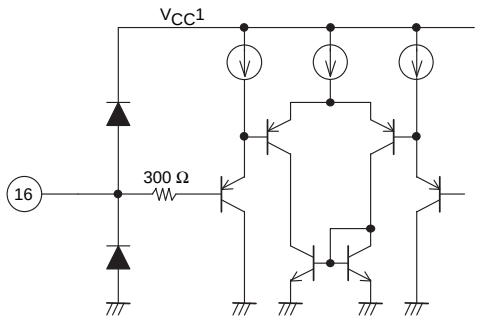
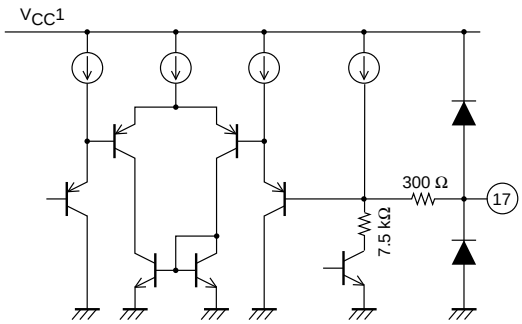
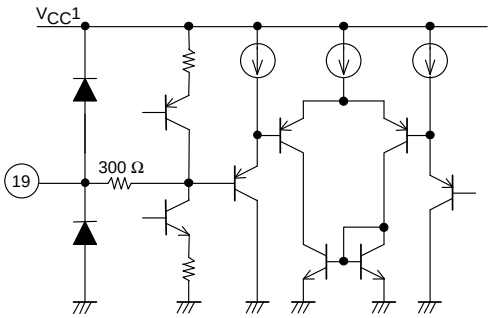
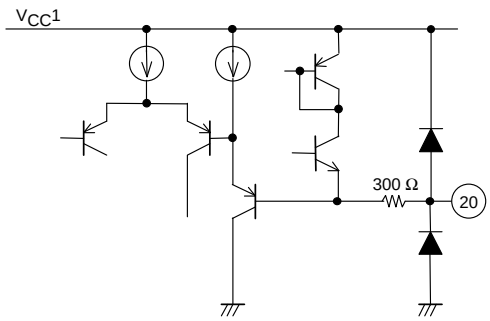
Pin No.	Pin	Functions	Equivalent circuit
16	TOC	Torque command input Normally, this pin is connected to the INT.OUT pin. The PWM duty is increased when the TOC pin voltage falls. Do not apply a voltage that exceeds V_{CC} – 0.5 V to this pin. (An input from a normal operational amplifier is desirable.)	
17	PWM	PWM oscillator frequency setting. Connect a capacitor between this pin and ground.	
19	FIL	VCO PLL filter connection	
20	R	Sets the value of the charge current from the VCO circuit C pin. Insert a resistor between this pin and ground.	

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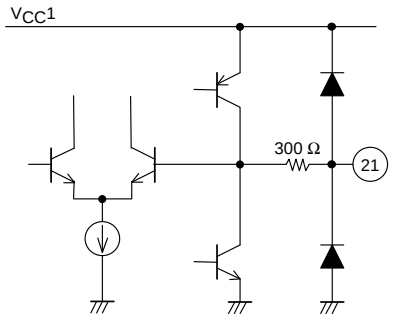
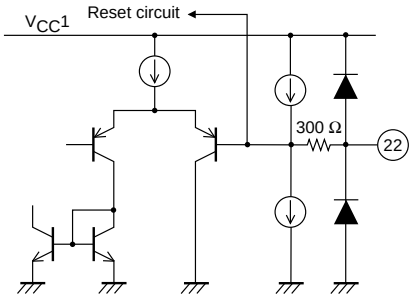
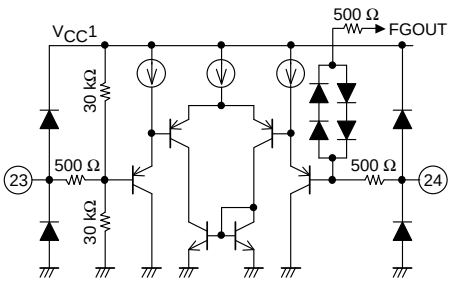
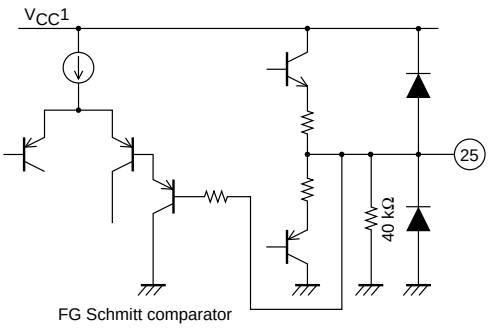
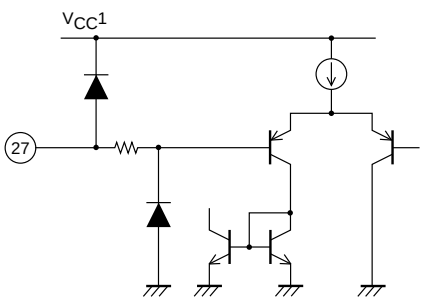
Pin No.	Pin	Functions	Equivalent circuit
21	C	VCO oscillator connection This pin sets the VCO frequency. Insert a capacitor between this pin and ground. Set the value of the capacitor so that the oscillator frequency does not exceed 1 MHz.	
22	CSD	Sets the operating time of the constrained-rotor protection circuit. Reference signal oscillator used when the clock signal is cut off and to prevent malfunctions. The protection function operating time can be set by connecting a capacitor between this pin and ground. This pin also functions as the logic circuit block power-on reset pin.	
23 24	FGIN+ FGIN−	FG amplifier input	
25	FGOUT	FG amplifier output This pin is connected to the FG Schmitt comparator circuit internally in the IC.	
27	RF GND	Output current detection Connect a resistor between this pin and ground.	

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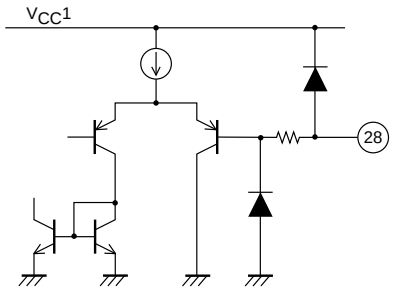
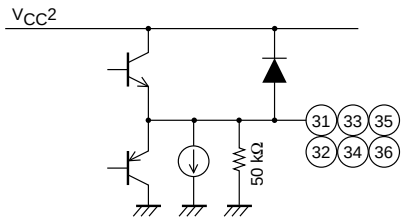
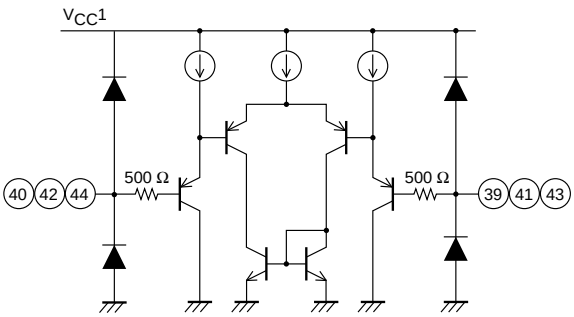
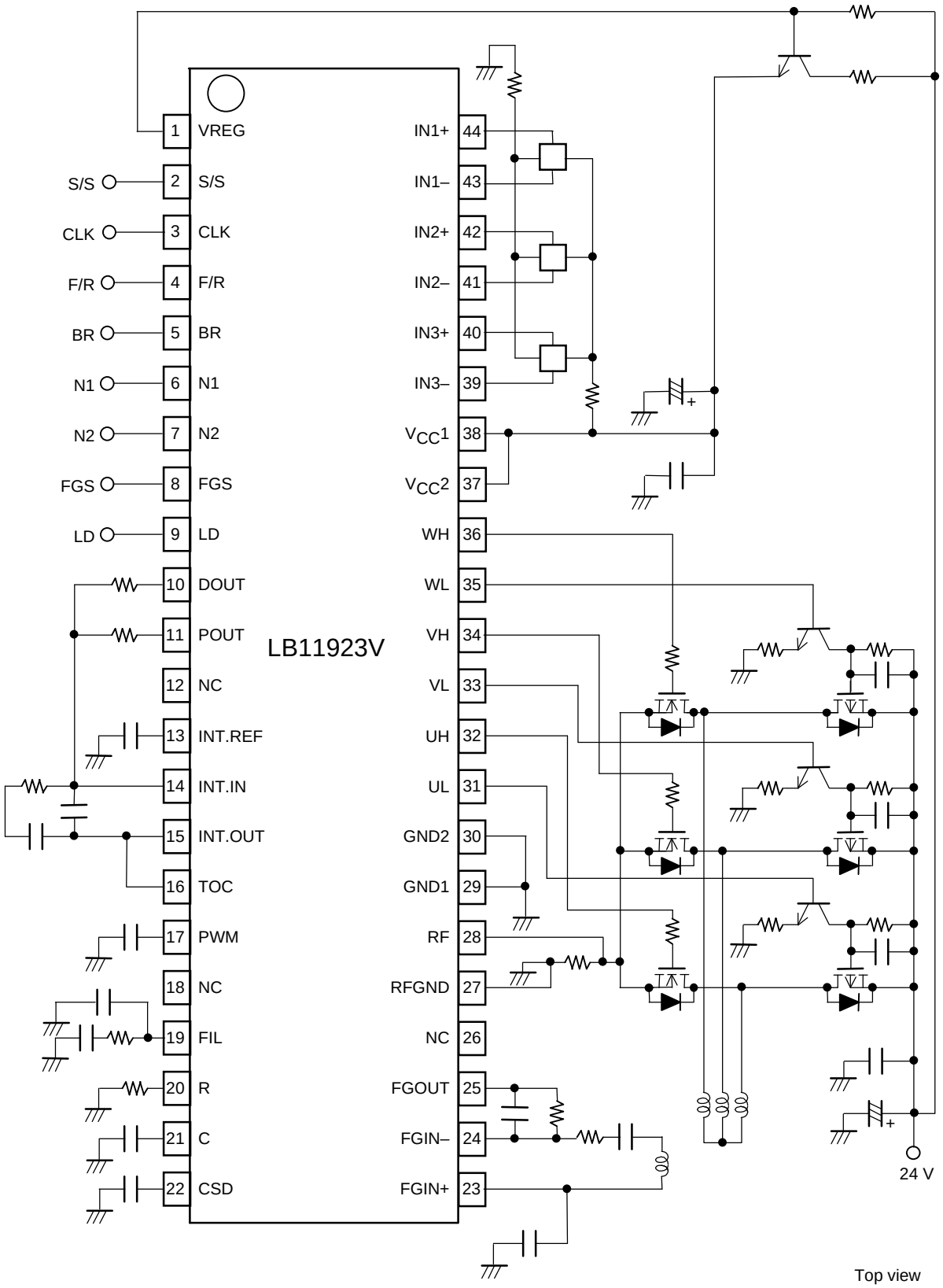
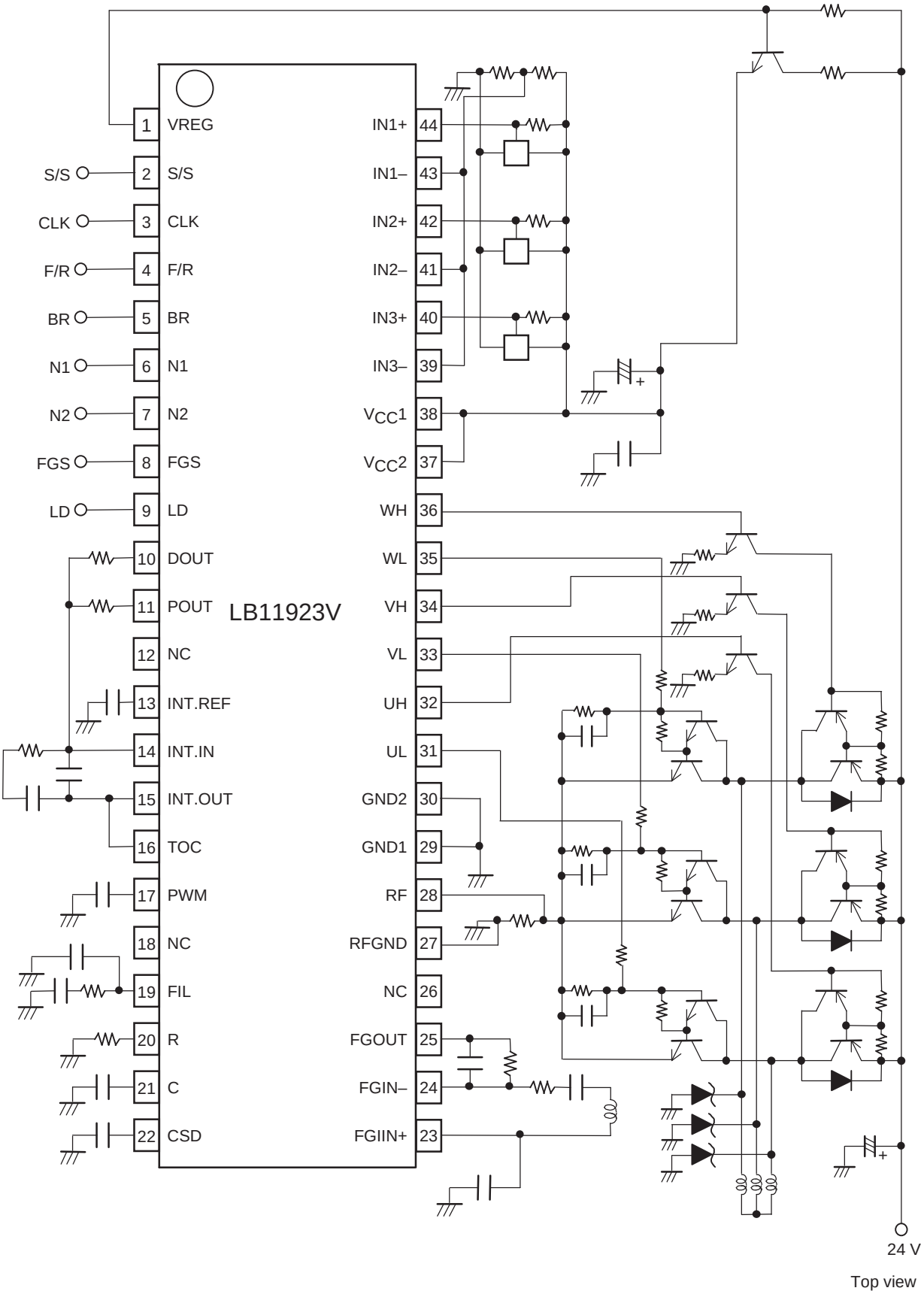
Pin No.	Pin	Functions	Equivalent circuit
28	RF	Output current detection Connect a resistor between this pin and ground. The output limitation maximum current, I_{OUT}, is set to be $0.26/R_f$ by this resistor.	
29	GND1	Control block ground	
30	GND2	Output block ground	
31 32 33 34 35 36	UL UH VL VH WL WH	Outputs (that are used to drive external transistors). The PWM duty is controlled on the UH, VH, and WH side of these outputs.	
37 38	$V_{CC}2$ $V_{CC}1$	Output block power supply Control block power supply Short $V_{CC}1$ to $V_{CC}2$ and, for stability, insert a capacitor between these pins and ground.	
39 40 41 42 43 44	IN3− IN3+ IN2− IN2+ IN1− IN1+	Hall-effect device inputs. The input is seen as a high-level input when IN+ > IN−, and as a low-level input for the opposite state. If noise on the Hall-effect device signals is a problem, insert capacitors between the corresponding IN+ and IN− inputs. The logic high state indicates that $V_{IN}^+ > V_{IN}^-$	
12 18 26	NC	These are unconnected pins, and can be used for wiring.	

Sample Application Circuit 1 (P-channel + n-channel, Hall-effect sensor application)

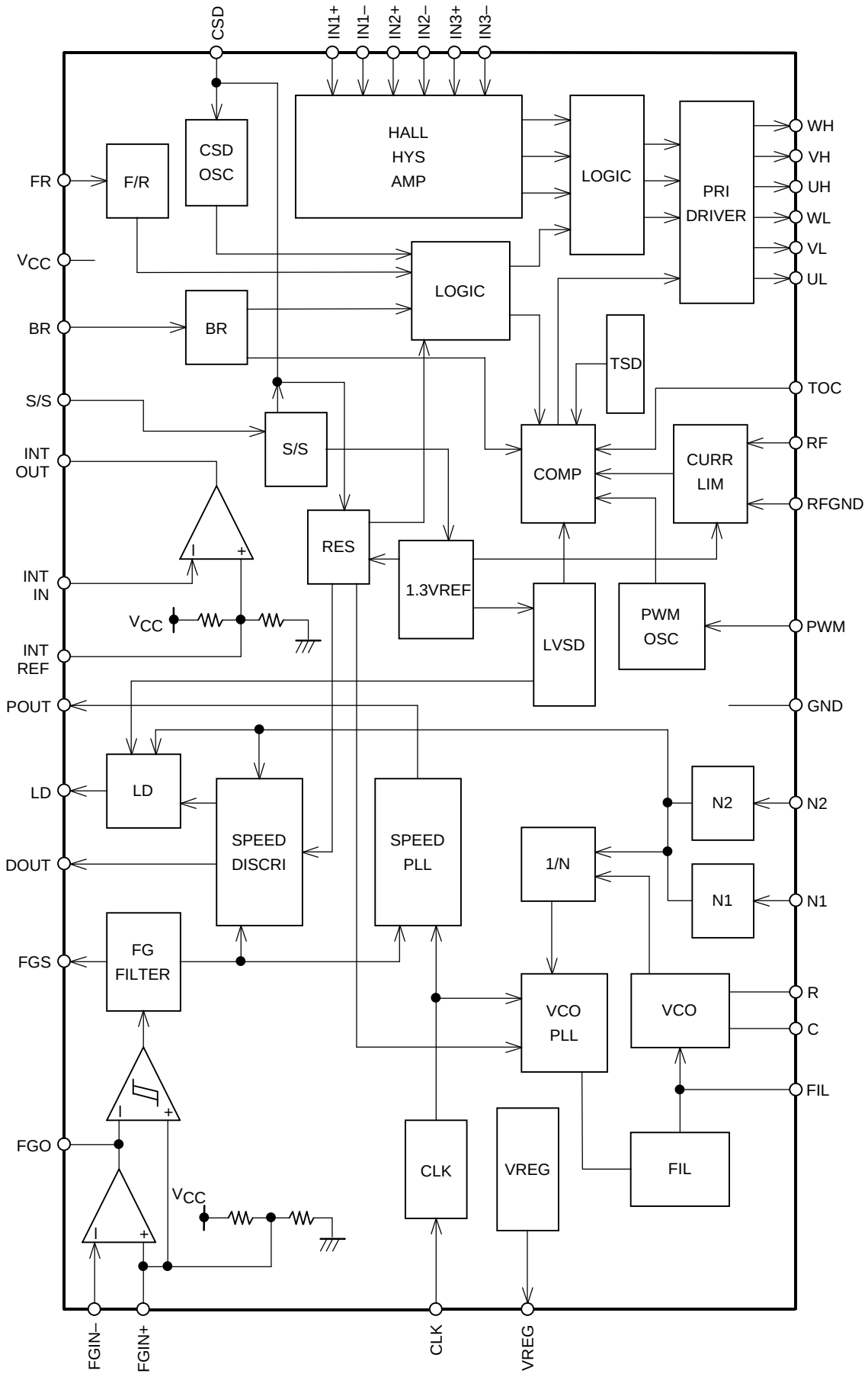


Sample Application Circuit 2 (PNP + NPN, Hall-effect sensor application)



Top view

Equivalent Circuit Block Diagram



IC Operation Description

1. Speed Control Circuit

   This IC implements speed control using the combination of a speed discriminator circuit and a PLL circuit. The speed discriminator circuit outputs (This counts a single FG period.) an error signal once every two FG periods. The PLL circuit outputs an error signal once every one FG Period. As compared to the earlier technique in which only a speed discriminator circuit was used, the combination of a speed discriminator and a PLL circuit allows variations in motor speed to be better suppressed when a motor that has large load variations is used. The FG servo frequency (fFG) is determined by the frequency relationship shown below and by the clock signal (fCLK) input to the CCLK pin.

   f_{FG} = (VCO divisor ÷ speed discriminator count) × f_{CLK}

N1	N2	Count	Divisor
High or open	High or open	1024	1024
High or open	Low	1024	512
Low	High or open	256	256
Low	Low	512	512

   Therefore it is possible to implement half-speed control without switching the clock frequency by using combinations of the N1 = high, N2 = low state and other setting states.

2. VCO Circuit

   The LB11923V includes a built-in VCO circuit to generate the speed discriminator circuit reference signal. The reference signal frequency is given by the following formula.

   $f_{VCO} = f_{CLK} \times$ divisor f_{VCO}: Reference signal frequency

   f_{CLK}: Externally input clock frequency

   The range over which the reference signal frequency can be varied is determined by the resistor and capacitor components connected to the R and C pins (pins 20 and 21) and by the VCO loop filter constant (the values of the external components connected to pin 19).

Supply voltage	R (kΩ)	C (pF)
When V_{CC} is 5 V	7.5	200
When V_{CC} is 6.3 V	11	200

   To acquire the widest possible range, it is better to use 6.3 V than 5 V as the supply voltage. It is also possible to handle an even wider range than is possible with fixed counts by making the speed discriminator count and the VCO divisor switchable.

   The components connected to the R, C, and FIL pins must be connected with lines to their ground pins (pins 29 and 30) that are as short as possible.

3. Output Drive Circuit

   To reduce power loss in the output, this IC adopts the direct PWM drive technique. The output transistors (which are external to the IC) are always saturated when on, and the motor drive output is adjusted by changing the duty with which the output is on. The PWM switching is performed on the high side for each phase (UH, VH, and WH). The PWM switching side in the output can be selected to be either the high or low side depending on how the external transistors are connected.

4. Current Limiter Circuit

   The current limiter circuit limits the (peak) current at the value I = V_{RF}/R_f (V_{RF} = 0.26 V (typical), R_f: current detection resistor). The current limitation operation consists of reducing the output duty to suppress the current.

   High accuracy detection can be achieved by connecting the RF and RFGND pin lines near the ends of the current detection resistor (Rf).

5. Speed Lock Range

   The speed lock range is ±6.25% of the fixed speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the motor on duty is adjusted according to the speed error to control the motor speed to be within the lock range.

6. Notes on the PWM Frequency

   The PWM frequency is determined by the capacitor (F) connected to the PWM pin.

   When V_{CC} = 6.3 V: $f_{PWM} \approx 1/(82000 \times C)$

   When V_{CC} = 5.0 V: $f_{PWM} \approx 1/(66000 \times C)$

   A PWM frequency of between 15 and 25 kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency during motor control, and if that frequency is in the audible range, that resonation may result in audible noise. If the PWM frequency is too high, the output transistor switching loss will increase. To make the circuit less susceptible to noise, the connected capacitors must be connected to the GND pin (pin 29 and pin 30) with lines that are as short as possible.

7. Hall effect sensor input signals

   An input amplitude of over 100 mV p-p is desirable in the Hall effect sensor inputs. The closer the input waveform is to a square wave, the lower the required input amplitude. Inversely, a higher input amplitude is required the closer the input waveform is to a triangular wave. Also note that the input DC voltage must be set to be within the common-mode input voltage range.

   If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs. Those capacitors must be located as close as possible to the input pins.

   When the Hall inputs for all three phases are in the same state, all the outputs will be in the off state.

   If a Hall sensor IC is used to provide the Hall inputs, those signals can be input to one side (either the + or - side) of the Hall effect sensor signal inputs as 0 to VCC level signals if the other side is held fixed at a voltage within the common-mode input voltage range that applies when a Hall effect sensors are used.

8. Forward/Reverse Switching

   The motor rotation direction can be switched using the F/R pin. However, the following notes must be observed if the motor direction is switched while the motor is turning.

   - This IC is designed to avoid through currents when switching directions. However, increases in the motor supply voltage (due to instantaneous return of motor current to the power supply) during direction switching may cause problems. The values of the capacitors inserted between power and ground must be increased if this increase is excessive.
   - If the motor current after direction switching exceeds the current limit value, the PWM drive side outputs will be turned off, but the opposite side output will be in the short-circuit braking state, and a current determined by the motor back EMF voltage and the coil resistance will flow. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which the direction is switched, the more severe this problem becomes.)

9. Brake Switching

   The LB11923V provides short-circuit braking implemented by turning the output transistors for the high side for all phases (UH, VH, and WH) on. (The opposite side transistors are turned off for all phases.) Note that the current limiter does not operate during braking. During braking, the duty is set to 100%, regardless of the motor speed. The current that flows in the output transistors during braking is determined by the motor back EMF voltage and the coil resistance. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which braking is applied, the more severe this problem becomes.)

   The braking function can be applied and released with the IC in the start state. This means that motor startup and stop control can be performed using the brake pin with the S/S pin held at the low level (the start state). If the startup time becomes excessive, it can be reduced by controlling motor startup and stop with the brake pin rather than with the S/S pin. (Since the IC goes to the power saving state when stopped, enough time for the VCO circuit to stabilize will be required at the beginning of the motor start operation.)

10. Constraint Protection Circuit

    The LB11923V includes an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. If the LD output remains high (indicating the locked state) for a fixed period in the start state, the upper side (external) transistors are turned off. This time is set by the capacitance of the capacitor attached to the CROCK pin. A time of a few seconds can be set with a capacitance of under 0.1 μF.

When V_{CC} = 6.3 V: The set time (in seconds) is 37 × C (μF)

When V_{CC} = 5.0 V: The set time (in seconds) is 30 × C (μF)

To clear the rotor constrained protection state, the application must either switch to the stop state for a fixed period (about 1 ms or longer) or turn off and reapply power.

If the rotor constrained protection circuit is not used, a 220 kΩ resistor and a 1500 pF capacitor must be connected in parallel between the CSD pin and ground. However, in that case, the clock disconnect protection circuit described below will no longer function. Since the CSD pin also functions as the power-on reset pin, if the CSD pin were connected directly to ground, the IC would go to the power-on reset state and motor drive operation would remain off. The power-on reset state is cleared when the CSD pin voltage rises above a level of about 0.64 V.

11. Clock Disconnect Protection Circuit

If the clock input goes to the no input state when the IC is in the start state, this protection circuit will operate and turn off the PWM output. If the clock is resupplied before the motor constraint protection circuit operates, the IC will return to the drive state, but if the motor constraint protection circuit does operate, the IC must either be set temporarily (approximately 1 ms or over) to the stop or brake state, or the power must be turned off and reapplied.

12. Low-Voltage Protection Circuit

The LB11923V includes a low-voltage protection circuit to protect against incorrect operation when power is first applied or if the power-supply voltage (V_{CC}) falls. The (external) upper side output transistors are turned off if V_{CC} falls under about 3.75 volts, and this function is cleared at about 4.0 volts.

13. Power Supply Stabilization

Since this IC is used in applications that draw large output currents, the power-supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the V_{CC} pin and ground. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.

14. Ground Lines

The signal system ground and the output system ground must be separated and a single ground point must be taken at the connector. Since the output system ground carries large currents, this ground line must be made as short as possible.

Output system ground ... Ground for R_f and the output diodes

Signal system ground ... Ground for the IC and the IC external components

15. V_{REG} Pin

If a motor drive system is formed from a single power supply, the V_{REG} pin (pin 1) can be used to create the power-supply voltage (about 6.3 V) for this IC. The V_{REG} pin is a shunt regulator and generates a voltage of about 7 volts by passing a current through an external resistor. A stable voltage can be generated by setting the current to value in the range 0.2 to 1.5 mA. The external transistors must have current capacities of at least 80 mA (to cover the I_{CC} + Hall bias current + output current <source> requirements) and they must have voltage handling capacities in excess of the motor power-supply voltage. Since the heat generated by these transistor may be a problem, heat sinks may be required depending on the packages used. If the IC power-supply voltage (4.4 to 7.0 V) is provided from an external circuit, apply that voltage directly to the V_{CC} pin(pin 37 and pin 38). In that case, the V_{REG} pin must either be left open or connected to ground.

16. FG Amplifier

The FG amplifier is normally implemented as a filter amplifier such as that shown in the application circuits to reject noise. Since a clamp circuit has been added at the FG amplifier output, the output amplitude is clamped at about 3 V p-p, even if the gain is increased.

Since a Schmitt comparator is inserted after the FG amplifier, applications must set the gain so that the amplifier output amplitude is at least 250 mV p-p. (It is desirable that the gain be set so that the amplitude is over 0.5 V p-p at the lowest controlled speed to be used.)

The capacitor inserted between the $FGIN^+$ pin (pin 23) and ground is required for bias voltage stabilization. To make the connected capacitor as immune from noise as possible, connect this capacitor to the GND pin (pin 29 and pin 30) with a line that is as short as possible.

17. Integrating Amplifier

The integrating amplifier integrates the speed error pulses and the phase error pulses and converts them to a speed command voltage. At the same time it also sets the control loop gain and frequency characteristics using external components.

The integrating amplifier output (pin 15) is normally connected to the TOC pin (pin 16) using external wiring. In cases where it is necessary to switch the integration constant in an application that uses a wide speed range by isolating the integrating amplifier output and the PWM control circuit, this type of constant switching application can be implemented by adding external operational amplifier, analog switch, and other components.

In either case, the basic idea is that the operational amplifier output is connected to the TOC pin. (Note that voltages in excess of V_{CC} – 0.5 V must not be applied to the TOC pin.)

18. FIL Pin External Components

The capacitor inserted between the FIL pin and ground is used to suppress ripple on the FIL pin voltage. Therefore, application designers must select a capacitance value that provides fully adequate smoothing of the FIL pin voltage even at the lowest external clock input frequency used. Also, the FIL pin voltage convergence time (the time until the reference signal stabilizes) when the input clock frequency is switched is shortened by connecting a resistor and a capacitor in series between the FIL pin and ground. Therefore, designers must select values for the resistor and capacitor that give the required convergence time.

19. R and C Pin External Components

The maximum range over which the reference signal frequency f_{VCO} can be varied when 5 V is used as the V_{CC} supply voltage is about a factor of three.

When it is desirable to make this range as wide as possible, since the values of the R pin external resistor (R) and the C pin external capacitor (C) are determined by the maximum value of the reference signal frequency ($f_{VCO}1$) and the minimum value ($V_{CC}L$) of the V_{CC} power supply due to unit-to-unit variations, R and C can be determined using the following procedure as a reference.

(1) Calculate R1 and C1 using the following formulas and determine values for R and C such that the conditions R ≤ R1 and C ≤ C1 will hold taking the sample-to-sample variations (including other issues such as temperature characteristics) into account.

$R1 = (V_{CC}L - 2.2\ V) / 280\ \mu A$

$C1 = (280\ \mu A / 0.9\ V) \times (1/f_{VCO}1) \times 0.7$

(2) The minimum value ($f_{VCO}2$) for the reference signal frequency that can be set for the R and C values determined in step (1) can be calculated from the following formula if we let R2 and C2 be the smallest values for R and C due to the sample-to-sample variations (including other issues such as temperature characteristics). Therefore, the range over which the reference signal frequency can be set is $f_{VCO}1$ to $f_{VCO}2$.

$f_{VCO}2 = 0.38 / (R2 \times C2)$

(3) The following are the conditions that must be met and the points that require care when determining the values of the external components connected to the R and C pins.

1. The maximum value of the set reference signal frequency must not exceed 1 MHz.
2. The R pin voltage and the FIL pin voltage must be in the range 0.3 V to ($V_{CC}L$ – 2.2 V). ($V_{CC}L$ is the lowest value of the V_{CC} supply voltage given the unit-to-unit variations. $V_{CC}L$ is always greater than or equal to 4.4 V.) However, the lower the R pin voltage, the more susceptible the system will be to ground line noise, and the reference signal frequency may become unstable as a result. Therefore the lower end of the R pin voltage range must not be used if there is much ground line noise in the system.
3. Set the value of the R pin external resistor to a value in the range 6.8 kΩ to 15 kΩ. Also, assure that the R pin current remains under 280 μA.
4. Set the value of the C pin external capacitor to a value in the range 150 pF to 1000 pF.
5. When it is desirable to make the range of the reference signal frequency as wide as possible, set the values of R and C to the largest possible values. (However, those values must be lower than the calculated values R1 and C1.) Use components with the smallest sample-to-sample variations possible. The V_{CC} voltage must be made as much higher than 5 V as possible by, for example, using this IC's VREG pin (7 V shunt regulator), to acquire the widest possible range for the reference signal frequency.

20. NC pin

Since the NC pins are electrically open with respect to the IC itself, they can be used as intermediate connection points for lines in the PCB pattern.