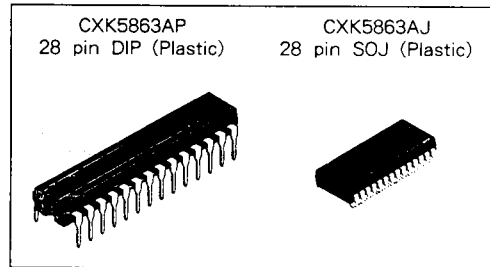


SONY**CXK5863AP/AJ** -20/25/30**8192 word × 8-bit High Speed CMOS Static RAM****Description**

CXK5863AP/AJ are 65,536 bits high speed CMOS static RAMS organized as 8,192 words by 8-bits and operate from a single 5V supply. These devices are suitable for use in high speed applications such as cash memory.

Features

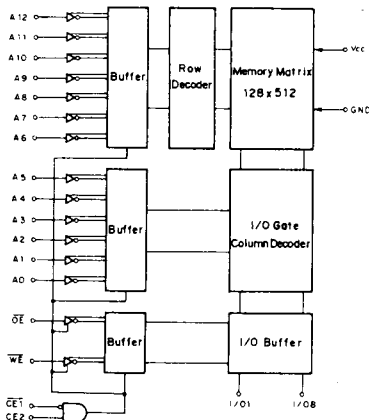
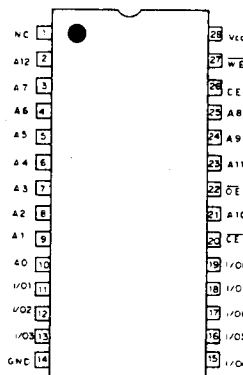
- Fast access time 20ns/25ns/30ns (Max.)
- Low power operation 250mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Full CMOS.
- Compatible with various types of packages
CXK5863AP 300mil 28pin DIP package
CXK5863AJ 300mil 28pin SOJ package

**Structure**

Silicon gate CMOS IC

Function

8192 word × 8-bit static RAM

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$)

Item	Symbol	Test condition	- 20			- 25 / - 30			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	-1	—	1	-1	—	-1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$	-1	—	1	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0mA$	—	50	80	—	50	80	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, $I_{OUT} = 0mA$	—	95	130	—	70	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	—	1	—	—	1	mA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

($T_a = 25^\circ C$, $f = 1MHz$)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

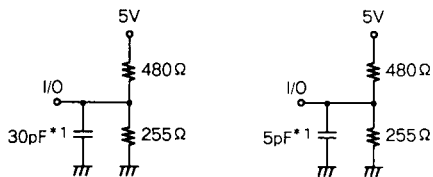
● AC test conditions

($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

Item	Conditions
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2) *2



*1 including scope and jig capacitance

*2 for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	trc	20	—	25	—	30	—	ns
Address access time	tAA	—	20	—	25	—	30	ns
Chip enable access time ($\overline{CE1}$)	tc01	—	20	—	25	—	30	ns
Chip enable access time (CE2)	tc02	—	20	—	25	—	30	ns
Output enable to output valid	toE	—	10	—	12	—	12	ns
Output hold from address change	tOH	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	tLZ1*, tLZ2*	5	—	5	—	5	—	ns
Output enable to output in low Z (\overline{OE})	tOLZ*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	tHZ1*, tHZ2*	0	10	0	12	0	12	ns
Chip disable to output in high Z (\overline{OE})	tOHZ*	0	8	0	10	0	10	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	tPU	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	tPD	—	20	—	20	—	20	ns

2) Write cycle

Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	tWC	20	—	25	—	30	—	ns
Address valid to end of write	tAW	15	—	20	—	20	—	ns
Chip enable to end of write	tcW	15	—	20	—	20	—	ns
Data to write time overlap	tDW	10	—	12	—	12	—	ns
Data hold from write time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	15	—	20	—	20	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	tWR	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	tWR1	0	—	0	—	0	—	ns
Output active from end of write	tOW*	5	—	5	—	5	—	ns
Write to output in high Z	tWHZ*	0	10	0	12	0	12	ns

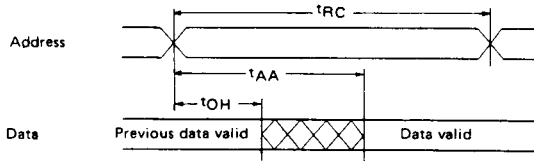
* Transition is measured ± 500 mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

5

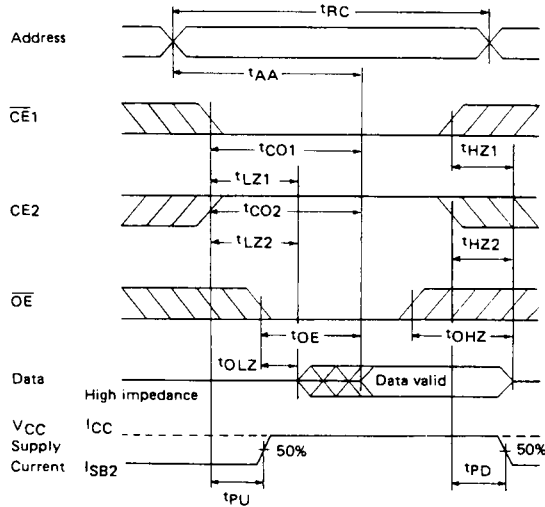
Timing Waveform

1) Read cycle

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

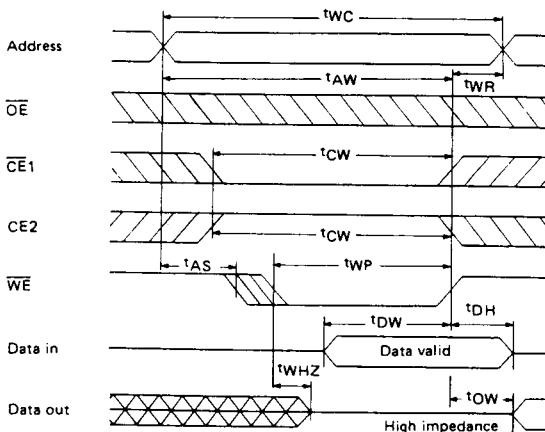


- Read cycle (2) : $\overline{WE} = V_{IH}$

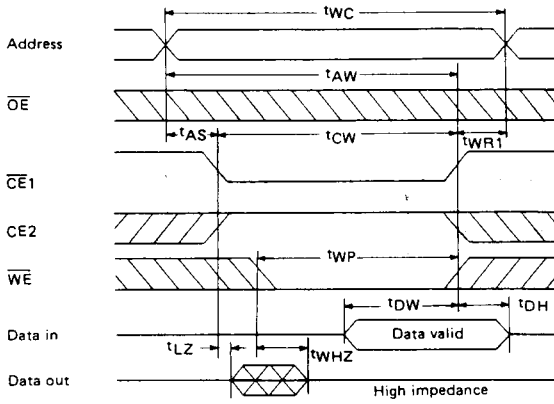


2) Write cycle

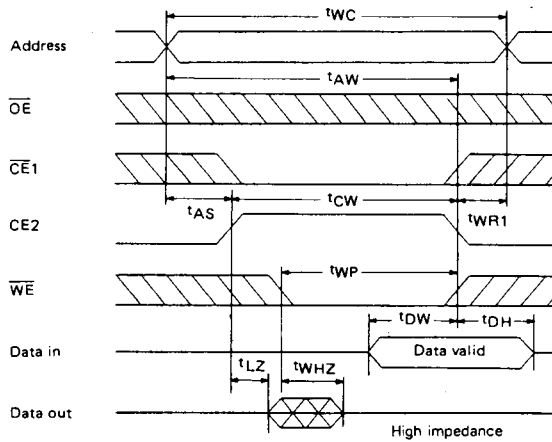
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



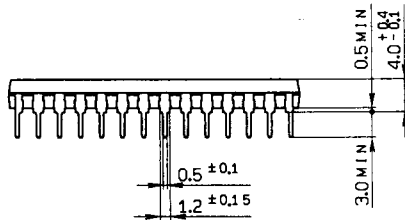
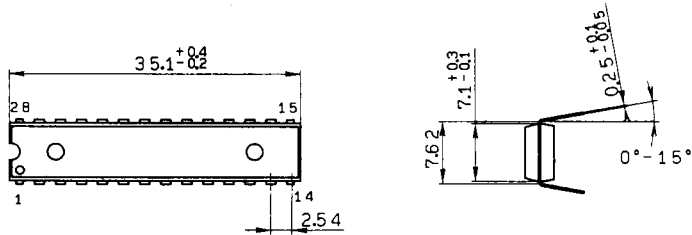
• Write cycle (3) : $\overline{CE2}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

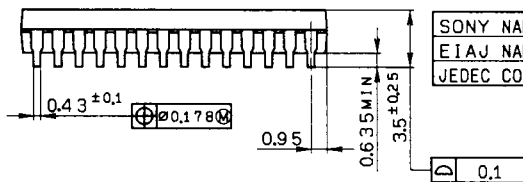
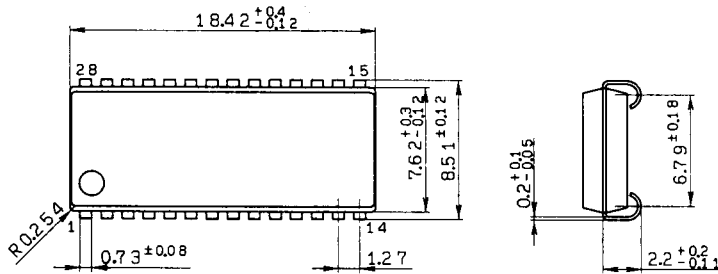
CXK5863AP 28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB*

*(Similar)

CXK5863AJ 28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB