NEC

MOS FIELD EFFECT TRANSISTOR

μPA503T

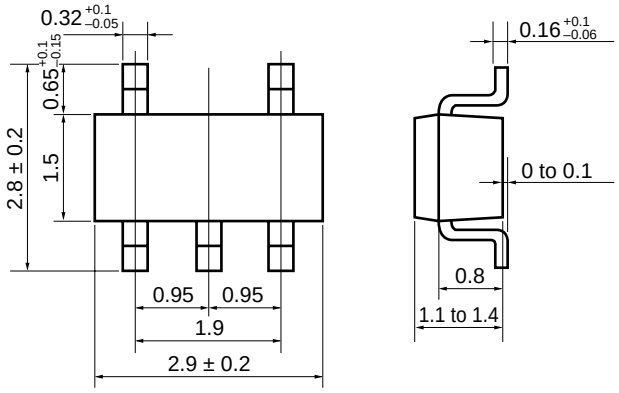
P-CHANNEL MOS FET (5-PIN 2 CIRCUITS)

The μPA503T is a mini-mold device provided with two MOS FET circuits. It achieves high-density mounting and saves mounting costs.

FEATURES

- Two source common MOS FET circuits in package the same size as SC-59
- Complement to μPA502T
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)

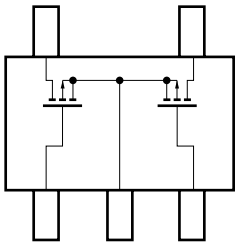


ABSOLUTE MAXIMUM RATINGS (T_A = 25 ˚C)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	–50	V
Gate to Source Voltage	V_{GSS}	∓16	V
Drain Current (DC)	$I_{D(DC)}$	–100	mA
Drain Current (pulse)	$I_{D(pulse)}$*	–200	mA
Total Power Dissipation	P_T	300 (TOTAL)	mW
Channel Temperature	T_{ch}	150	˚C
Storage Temperature	T_{stg}	–55 to +150	˚C

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

PIN CONNECTION (Top view)



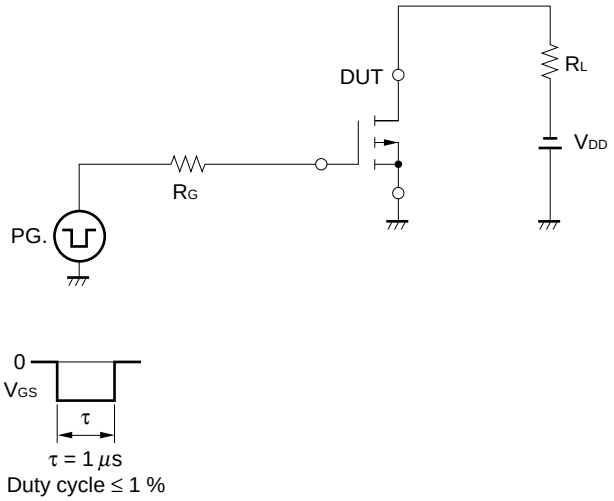
Document No. G11239EJ1V0DS00 (1st edition)
Date Published June 1996 P
Printed in Japan

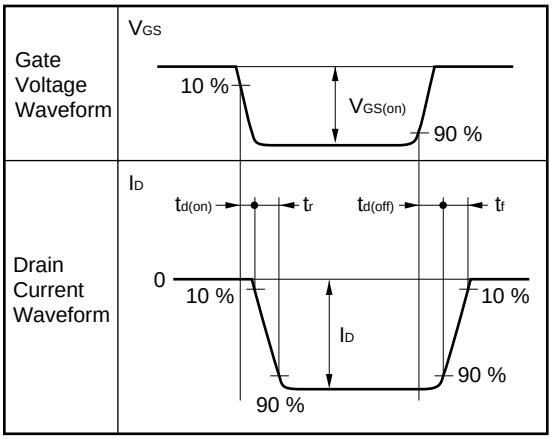
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DSS}	V_{DS} = –50 V, V_{GS} = 0			–1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –5.0 V, I_D = –1.0 μA	–1.5	–1.9	–2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –5.0 V, I_D = –10 mA	15			mS
Drain to Source On-State Resistance	$R_{DS(on)1}$	V_{GS} = –4.0 V, I_D = –10 mA		60	100	Ω
Drain to Source On-State Resistance	$R_{DS(on)2}$	V_{GS} = –10 V, I_D = –10 mA		40	60	Ω
Input Capacitance	C_{iss}	V_{DS} = –5.0 V, V_{GS} = 0, f = 1.0 MHz		17		pF
Output Capacitance	C_{oss}			9		pF
Reverse Transfer Capacitance	C_{rss}			1		pF
Turn-On Delay Time	$t_{d(on)}$	$V_{GS(on)}$ = –4.0 V, R_G = 10 Ω		45		ns
Rise Time	t_r	V_{DD} = –5.0 V, I_D = –10 mA		75		ns
Turn-Off Delay Time	$t_{d(off)}$	R_L = 500 Ω		25		ns
Fall Time	t_f			80		ns

Marking: CA

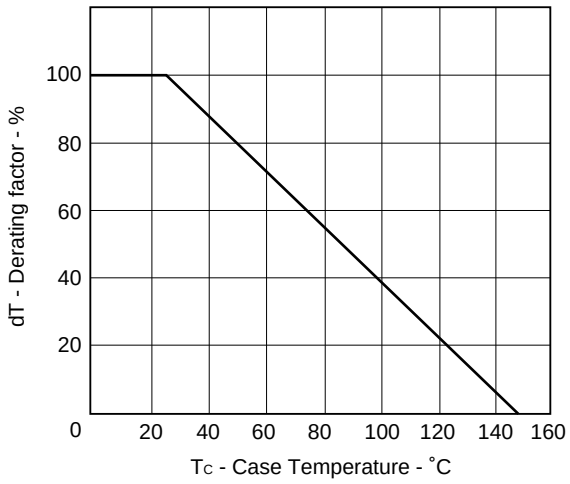
SWITCHING TIME MEASUREMENT CIRCUIT AND MEASUREMENT CONDITIONS (RESISTANCE LOADED)



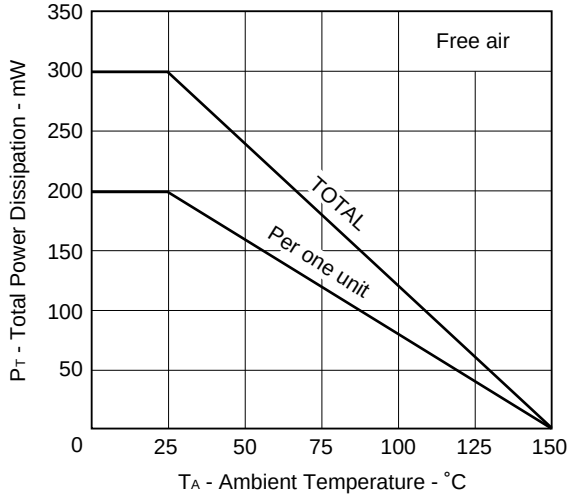


TYPICAL CHARACTERISTICS (T_A = 25 ˚C)

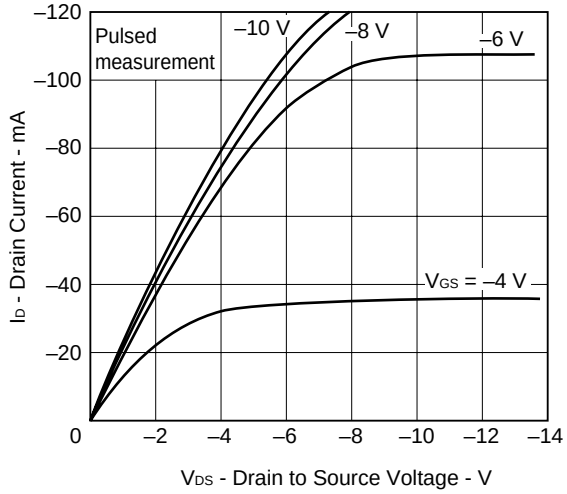
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



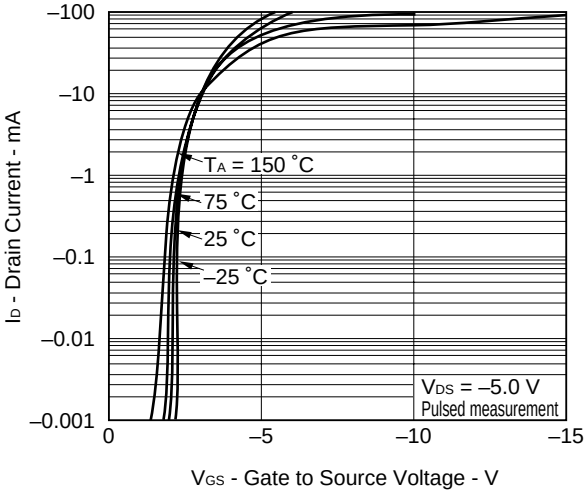
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



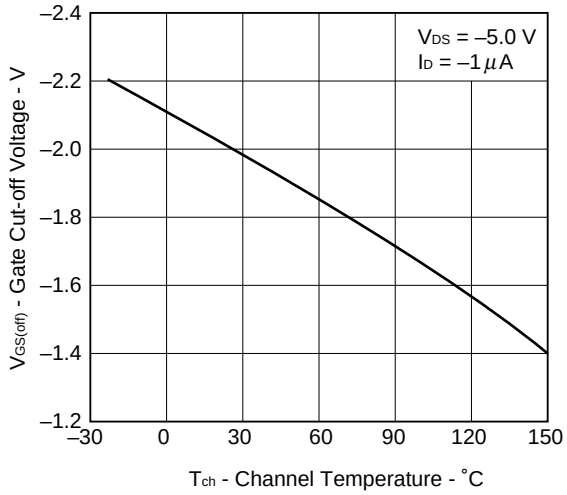
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



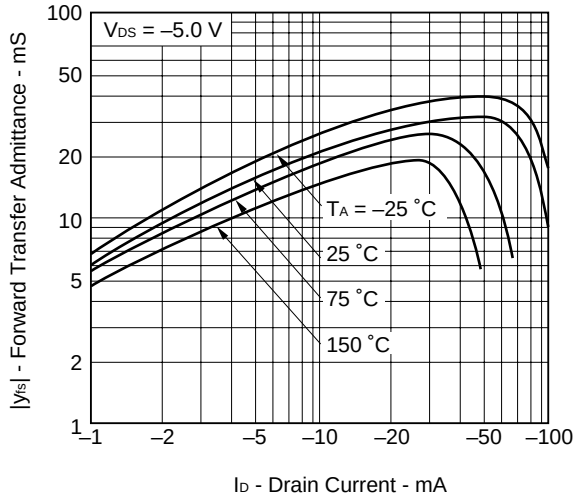
TRANSFER CHARACTERISTICS



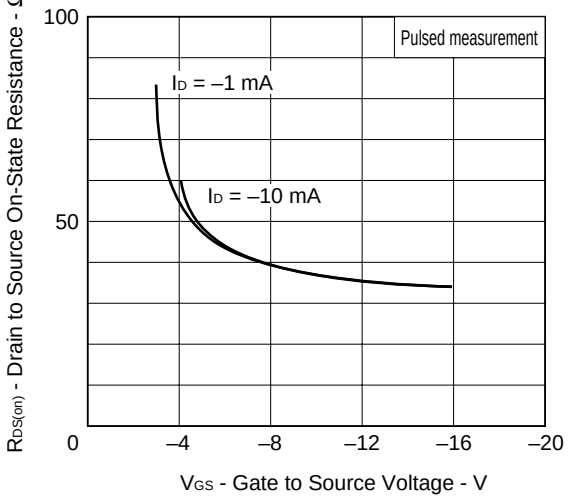
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



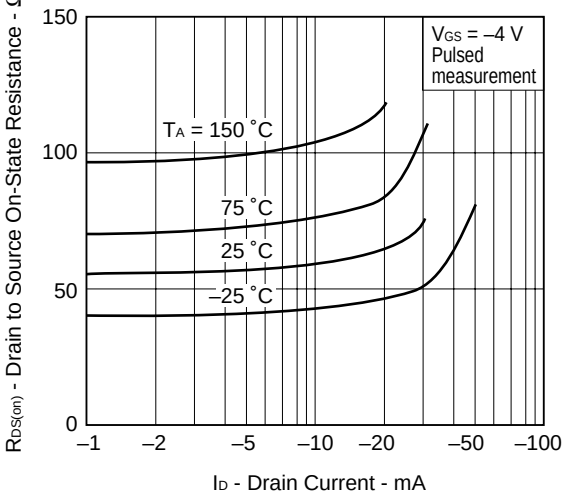
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



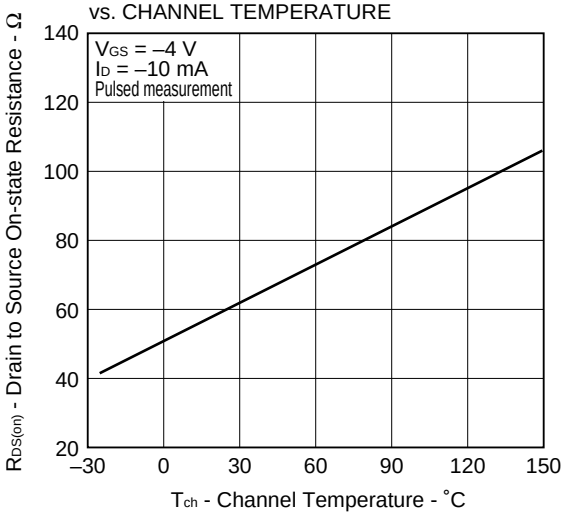
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



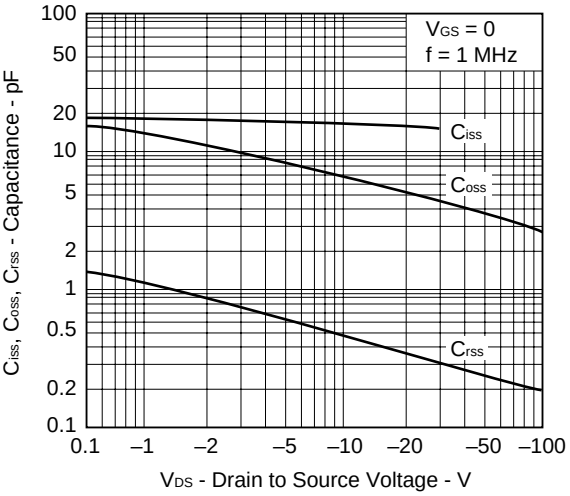
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



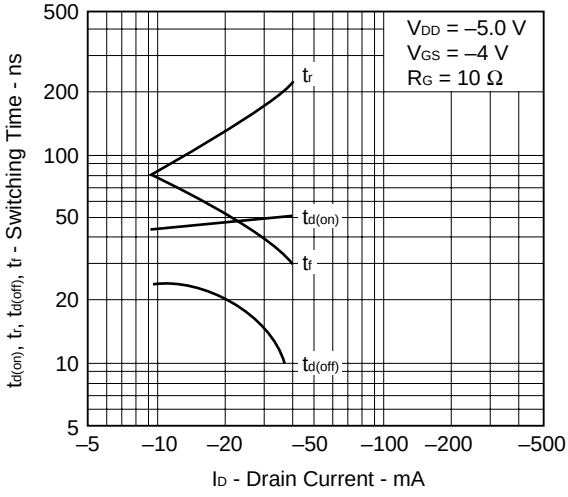
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



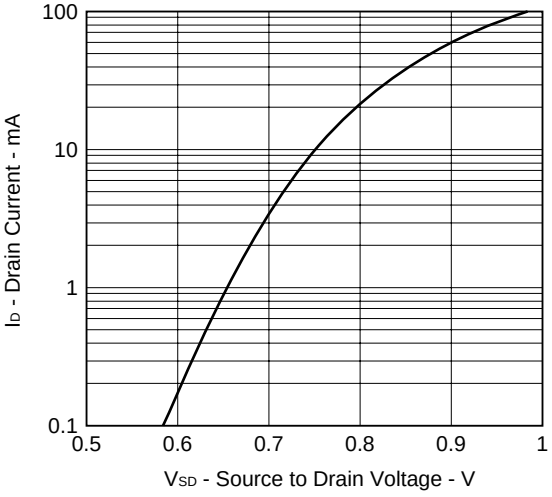
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E