P²CCD DELAY LINE AND MATRIX

GENERAL DESCRIPTION

The TDA8451A is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) delay line and matrix which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates two delay lines with a delay length of 1 line time for colour difference signals, adding circuits for the delayed and direct signals and clock drivers for the delay lines which are driven from an internal voltage controlled oscillator (VCO) locked to the sandcastle pulse.

The TDA8451A differs from the TDA8451 by the following:

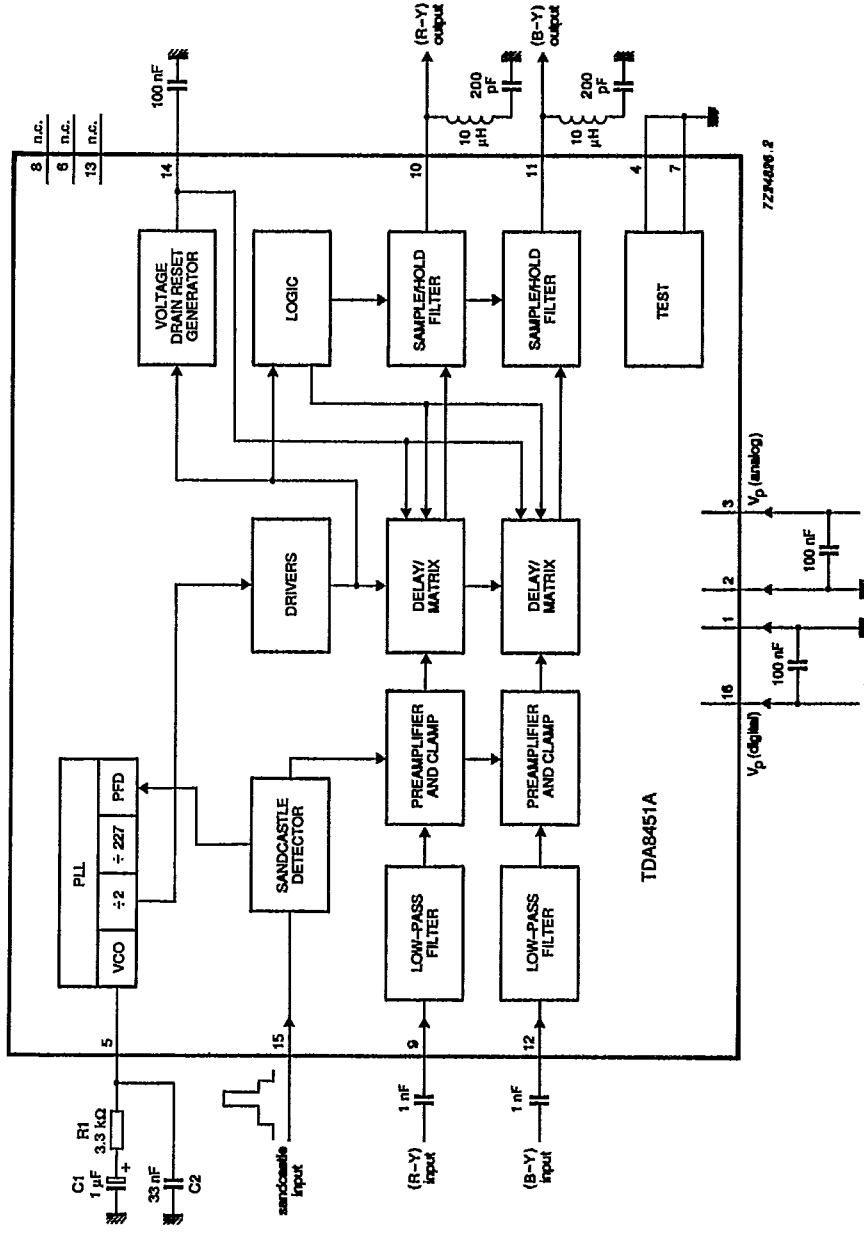
- The VCO is line locked instead of sub-carrier locked
- Adding direct and delayed signals occurs for PAL, SECAM and NTSC

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 3)		$V_{P(a)}$	10.8	12.0	13.2	V
digital (pin 16)		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 3)		$I_{P(a)}$	5	10	15	mA
digital (pin 16)		$I_{P(d)}$	10	22	35	mA
Colour difference input signals (peak-to-peak value)	PAL/NTSC mode	$V_{I(p-p)}$	–	–	1.1	V
	SECAM mode	$V_{I(p-p)}$	–	–	2.1	V
Output signals	PAL/NTSC mode 0.8 V(p-p) input	V_O	–	0.8	–	V
	SECAM mode 1.6 V(p-p) input	V_O	–	0.8	–	V
Output resistance		R_O	–	500	–	Ω
Frequency response		Δf	–	1.3	–	MHz
Additional delay		t_d	–	760	–	ns

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).



Notes to Fig.1

1. If the TDA8451A is followed by a TDA4566 (CTI), it is recommended to replace the LC trap (and the usual RC low-pass filter in front of the TDA4566) by an LC low-pass circuit where L = 47 µH and C = 270 pF.
2. For multistandard concepts, including NTSC, the following values are recommended; R1 = 47 kΩ, C1 = 100 nF and C2 = 2.2 nF.

Fig.1 Block diagram.

PINNING

1	Ground (digital)
2	Ground (analog)
3	Supply voltage input (analog)
4	Test pin (grounded for normal operation)
5	PLL filter
6	Not connected
7	Test pin (grounded for normal operation)
8	Not connected
9	(R-Y) input
10	(R-Y) output
11	(B-Y) output
12	(B-Y) input
13	Not connected
14	Voltage drain reset generator decoupling
15	Sandcastle input
16	Supply voltage input (digital)

FUNCTIONAL DESCRIPTION

When the (R-Y) and (B-Y) signals have been demodulated in the decoder, the resultant signals are applied to pins 9 and 12. The colour difference signals are then applied via a low-pass filter, preamplifier and clamp circuit to the delay lines. The delayed and direct signals are added in the matrix circuit.

This action occurs for PAL, SECAM and NTSC signals. Consequently, the NTSC colour difference signals are combed.

The frequency generated by the PLL circuit is 454 times the sandcastle frequency. The delay lines are driven by the internal clock drivers at half on the PLL frequency. The outputs from the delay lines are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.

The P^2CCD delay line and matrix requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 14. A circuit for the TDA8451A together with PAL decoder (TDA8391) is illustrated in Fig.2. A circuit for the TDA8451A together with the PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.3. The TDA8490 can also be used in combination with the TDA8391.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_{P(a)}$		13.2	V
Supply voltage (digital)		$V_{P(d)}$		13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	55 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified

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parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3) analog		$V_{P(a)}$	10.8	12.0	13.2	V
Supply current (pin 3) analog		$I_{P(a)}$	5	10	15	mA
Supply voltage (pin 3) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	10	–	dB
Supply voltage (pin 16) digital		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current (pin 16) digital		$I_{P(d)}$	10	22	35	mA
Supply voltage (pin 16) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	25	–	dB
Total power dissipation		P_{tot}	–	0.38	0.66	W
Inputs for demodulated colour difference signals (pins 9 and 12)						
AC coupled and clamped by sandcastle pulse						
Input signal PAL/NTSC mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	1.1	V
Input signal SECAM mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	2.1	V
Input current (outside clamping time)		I_I	–	–	0.1	μA
Input capacitance		C_I	–	10	–	pF
Sandcastle input (pin 15)						
Input resistance		R_{15}	1000	–	–	kΩ
Detection level		V_{15}	6.0	6.8	7.5	V
CD signal output (pins 10 and 11)						
Output signals where input signal is PAL/NTSC at 0.8 V (peak-to-peak value)		$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V
Output signals where input signal is SECAM at 1.6 V (peak-to-peak value)	note 2	$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V

parameter	conditions	symbol	min.	typ.	max.	unit
Output resistance		R_O	300	500	800	Ω
Internal current load of CD outputs		$I_{10;11}$	0.4	–	1.5	mA
DC output level		$V_{10;11}$	4	–	8	V
Rest clock signals (RMS value)	note 3					
at 3.55 MHz		$V_{10\text{-}11(rms)}$	–	–	5	mV
at 7.09 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
at 14.19 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
Signal-to-noise ratio	note 4	S/N	60	65	–	dB
Linearity of output signals (peak-to-peak value)	note 5					
(R-Y); pin 9 to 10 PAL/NTSC	V_I = 0.85 V	α	0.95	–	–	
(R-Y); pin 9 to 10 SECAM	V_I = 1.60 V	α	0.92	–	–	
(B-Y); pin 12 to 11 PAL/NTSC	V_I = 1.10 V	α	0.95	–	–	
(B-Y); pin 12 to 11 SECAM	V_I = 2.10 V	α	0.92	–	–	
Frequency response	at –3 dB	Δf	1.0	1.3	–	MHz
Difference in amplitude between delayed and undelayed signal			–	–	1.5	%
Difference in amplitude of the two output signals for equal input signals			–	–	5	%
Delay time with a 15625 kHz sandcastle pulse		t_d	–	760	–	ns

Notes to the characteristics

1. The SVRR is measured with a 100 Ω resistor in series with a 1 nF capacitor connected between pin 9 and pin 2 and between pin 12 and pin 2.
2. During SECAM the input signal is available during one of two sequential lines. The output signal is thereby halved in comparison with the PAL signal condition.
   To compensate for this the input signal to the TDA8451A during SECAM is twice that during PAL.
3. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) which is connected directly to pin 1 and pin 10 or pin 1 and pin 11.
4. The signal-to-noise ratio (in the PAL mode) is calculated by:

   $$\frac{V_{O(p\text{-}p)}}{V_{noise(rms)}\ (0\text{-}1\ MHz)}$$ at an input voltage of 0.8 V(p-p), 0 dB gain
5. The linearity is defined as the amplification of the given input voltage swing divided by the amplification when the input voltage swing is decreased to 70%.

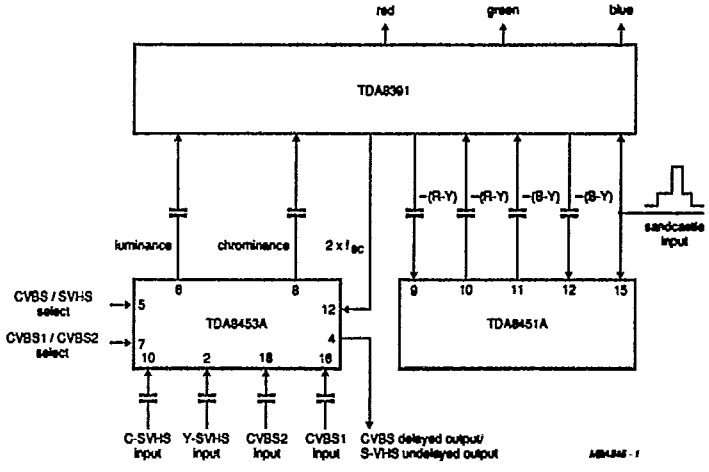

Fig.2 PAL decoder configuration.

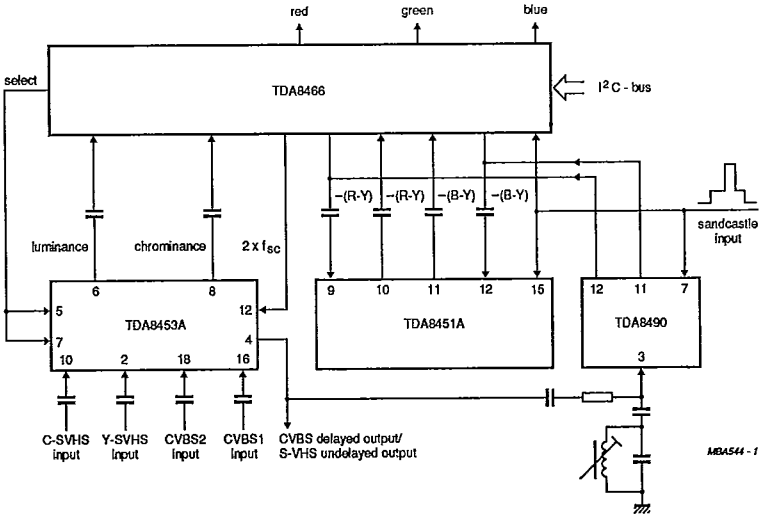

Fig.3 PAL-NTSC-SECAM decoder configuration.