Winbond Electronics Corp.

8-BIT OTP MICROCONTROLLER

GENERAL DESCRIPTION

The W78E52 is an 8-bit microcontroller that is functionally compatible with the W78C52, except that the mask ROM is replaced by a flash EEPROM with a size of 8 KB.

To facilitate programming and verification, the flash EEPROM inside the W78E52 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E52 microcontroller supplies a wider frequency range than most 8-bit microcontrollers on the market. It is functionally compatible with the industry-standard 80C52 microcontroller series.

The W78E52 contains four 8-bit bidirectional and bit-addressable I/O ports, three 16-bit timer/counters, and a serial port. These peripherals are supported by a six-source, two-level interrupt capability. There are 256 bytes of RAM and an 8 KB flash EEPROM for application programs.

The W78E52 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

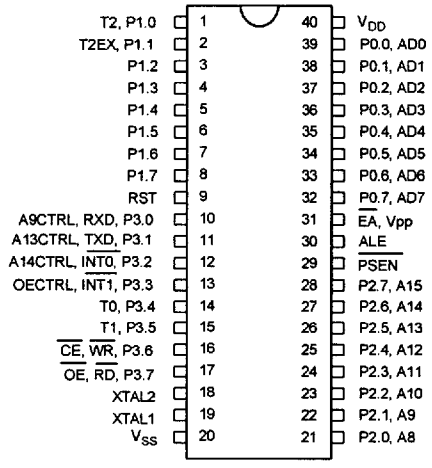
- 8-bit CMOS microcontroller
- Fully static design
- Low standby current at full supply voltage
- DC-40 MHz operation
- 256 bytes of on-chip scratchpad RAM
- 8 KB electrically erasable/programmable EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bidirectional ports
- Three 16-bit timer/counters
- One full duplex serial port
- Boolean processor
- Six-source, two-level interrupt capability
- Built-in power management
- Code protection mechanism
- Packages:
  - DIP 40: W78E52-16/24/33/40
  - PLCC 44: W78E52P-16/24/33/40

Publication Release Date: October 1996
Revision A2

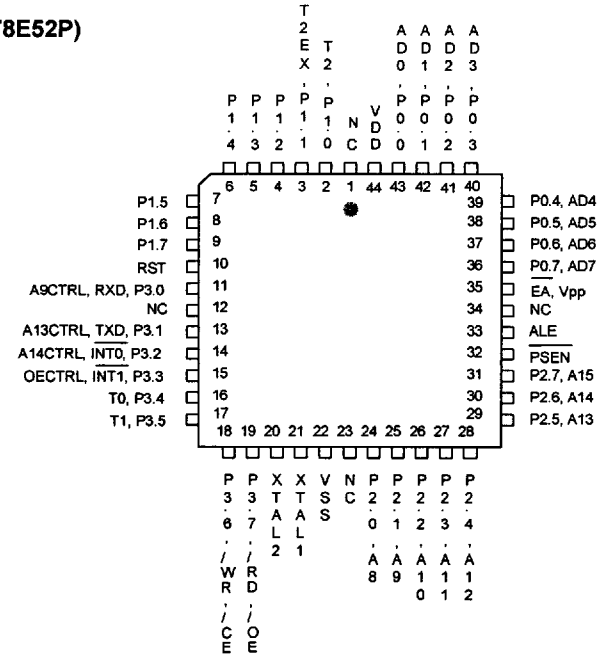
Winbond Electronics Corp.

PIN CONFIGURATIONS

40-pin DIP (W78E52)



44-Pin PLCC (W78E52P)



PIN DESCRIPTION

The W78E52 has two operating modes, normal and flash. In normal mode, the W78E52 corresponds to the W78C52. In flash mode, the user (the maker of the flash EEPROM writer) can access the lash EEPROM.

P0.7–P0.0 Port 0, Bits 7–0

MODE	DESCRIPTION
Normal	Functions are the same as those in the W78C52.
Flash	This port provides the data bus during access to the flash EEPROM.

P1.7–P1.0 Port 1, Bits 7–0

MODE	DESCRIPTION
Normal	Functions are the same as those in the W78C52.
Flash	This port provides the low-order address bus during access to the flash EEPROM.

P2.7–P2.0 Port 2, Bits 7–0

MODE	DESCRIPTION
Normal	Functions are the same as those in the W78C52.
Flash	This port provides the high-order address bus during access to the flash EEPROM.

P3.7–P3.0 Port 3, Bits 7–0

MODE	DESCRIPTION
Normal	Functions are the same as those in the W78C52.
Flash	P3.3–P3.0 and P3.7–P3.6 are the flash mode configuration pins, Input. P3.3–P3.0 and P3.7–P3.6 are configured to select or execute the flash operations. For details, see *Flash Operations*.

$\overline{EA}$/VPP

MODE	DESCRIPTION
Normal	$\overline{EA}$, External Access, Input, active low. This pin forces the processor to execute a program from the external ROM. When the internal flash EEPROM is accessed as in the W78C52, this pin should be kept high.
Flash	VPP, Program Power supply pin, Input. This pin accepts the high voltage (12V) needed for programming the flash EEPROM.

RST

MODE	DESCRIPTION
Normal	RST, Reset, Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.
Flash	Flash mode configuration pin, Input, active high. RST is used to configure the flash operations. For details, see *Flash Operations.*

ALE

MODE	DESCRIPTION
Normal	ALE, Address Latch Enable, Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high impedance state with a weak pull-up during reset state.
Flash	Flash mode configuration pin, Input, active low. ALE is used to configure the flash operations. For details, see *Flash Operations.*

$\overline{\text{PSEN}}$

MODE	DESCRIPTION
Normal	$\overline{\text{PSEN}}$, Program Store Enable, Output, active low. This pin enables the external ROM onto the Port 0 address/data bus during fetch and MOVC operations. $\overline{\text{PSEN}}$ goes to a high impedance state with a weak pull-up during reset state
Flash	Flash mode configuration pin, Input, active high. $\overline{\text{PSEN}}$ is used to configure the flash operations. For details, see *Flash Operations.*

XTAL1

MODE	DESCRIPTION
Normal	Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.
Flash	Connect to Vss.

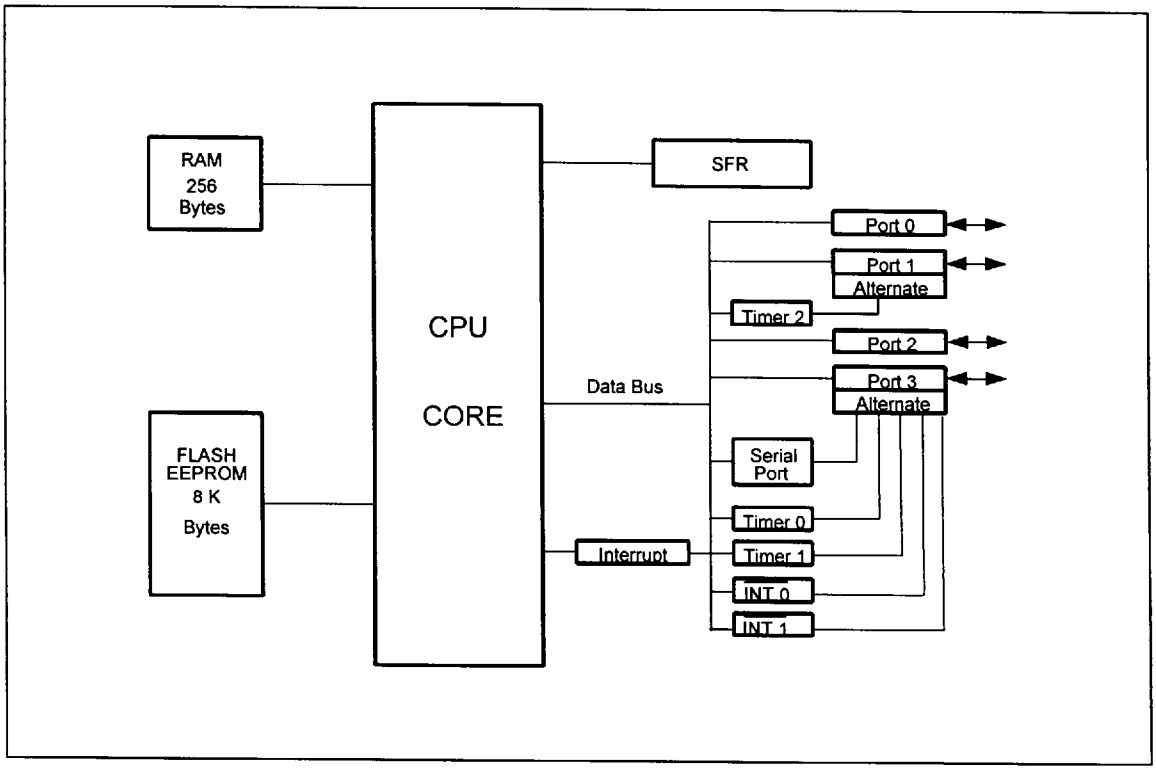
XTAL2

MODE	DESCRIPTION
Normal	Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.
Flash	No function in this mode.

Vss, Vcc

Power Supplies. These are the chip ground and positive supplies.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W78E52 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78E52: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

Clock

The W78E52 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78E52 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78E52 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

Power Reduction Function

The status of the external pins during the idle and power-down modes for the W78E52 is shown in the following table.

		ALE	$\overline{\text{PSEN}}$	P0	P1	P2	P3
Idle	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Addr.	Data
Power	Internal	0	0	Data	Data	Data	Data
Down	External	0	0	Float	Data	Addr.	Data

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E52 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

Option Setting

Users write programs into the W78E52 by using the Winbond proprietary writer. The writer programs the data into an internal 8 KB region and reads the data back for verification. After confirming that the program is correct, the user can lock the data so that they can no longer be read.

Lock Bit

This bit is used to protect the customer data in the W78E52. It may be turned on after the programmer finishes the programming and verify sequence. Once this bit is set to logic 0, no flash data can be accessed again.

MOVC Execute

This bit is used to restrict the region accessible to the MOVC instruction. It can prevent the program from being downloaded using this instruction if the program needs to jump outside to get data. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code in the external memory, but it will not be able to access code in the internal memory. A MOVC instruction in internal program memory space will always be able to access code in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Flash Operations

In normal operation, the W78E52 is functionally compatible with the W78C52. In the flash operating mode, the flash EEPROM can be programmed and verified repeatedly. Once the code inside the flash EEPROM is confirmed, the code can be protected. The flash EEPROM and the operations on it are described below.

All of the operations are configured by the pins RST, ALE, $\overline{PSEN}$, A9CTRL (P3.0), A13CTRL (P3.1), A14CTRL (P3.2), OECTRL (P3.3), $\overline{CE}$ (P3.6), $\overline{OE}$ (P3.7), A0 (P1.0) and V_{PP} ($\overline{EA}$). In these operations, A15 to A0 (P2.7 to P2.0, P1.7 to P1.0) and D7 to D0 (P0.7 to P0.0) serve as the address and data bus, respectively.

Read Operation

This operation enables customers to read their codes and the option bits. The data will not be valid if the lock bit is programmed to low.

Program Operation

This operation is used to program data to the flash EEPROM and the option bits. Programming is initiated when V_{PP} reaches V_{CP} (12V) level, $\overline{CE}$ is set to low, and $\overline{OE}$ is set to high.

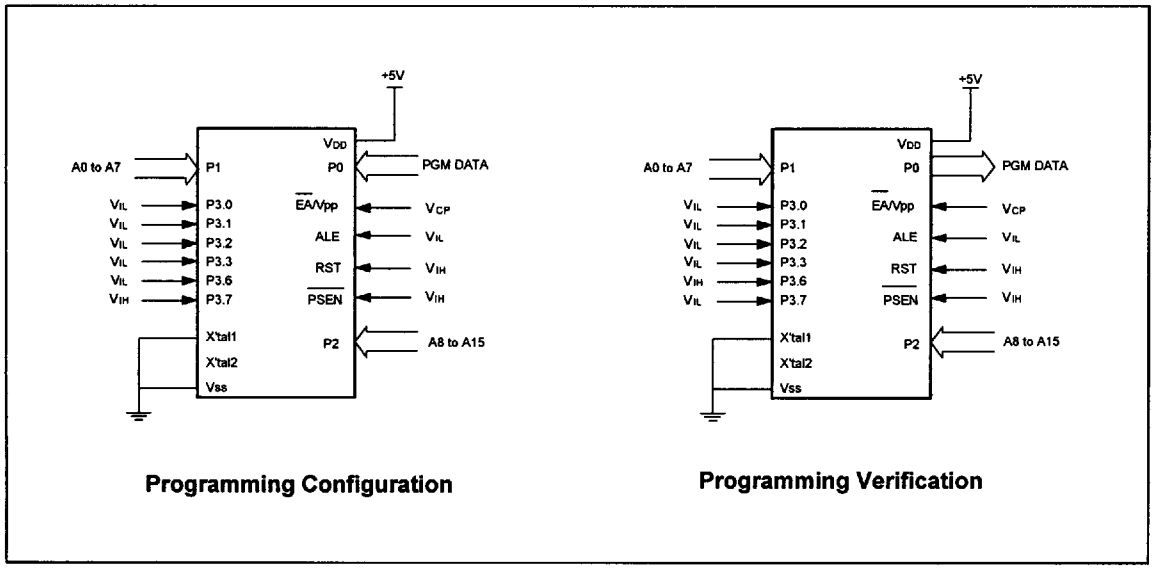
Program Verify Operation

All data must be checked after programming. This operation should be performed after each byte is programmed, and it will ensure a substantial program margin.

OPERATION	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ($\overline{CE}$)	P3.7 ($\overline{OE}$)	$\overline{EA}$ (V_{PP})	P2, P1 (A15 TO A0)	P0 (D7 TO D0)	NOTES
Read	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Address	Data Out	1, 2
Program	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{CP}	Address	Data In	1, 2
Program Verify	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CP}	Address	Data Out	3

Notes:

1. During all of these operations, RST = H, ALE = V_{IL}, and $\overline{PSEN}$ = V_{IH}.
2. V_{CP} = 12V, V_{IH} = V_{DD}, V_{IL} = Vss.
3. The program verify operation should follow the programming operaion.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability the device.

DC CHARACTERISTICS

V_{CC}–V_{SS} = 5V ±10%, T_A = 25° C, F_{OSC} = 20 MHz unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
			MIN.	MAX.	
Operating Voltage	V_{DD}		4.5	5.5	V
Operating Current	I_{DD}	No load V_{DD} = 5.5V	-	50	mA
Idle Current	I_{IDLE}	Idle mode V_{DD} = 5.5V	-	7	mA
Power Down Current	I_{PWDN}	Power-down mode V_{DD} = 5.5V	-	50	µA
Input Current P1, P2, P3	I_{IN1}	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}	-50	+10	µA
Logical 1-to-0 Transition Current P1, P2, P3 (*1)	I_{TL}	V_{DD} = 5.5V V_{IN} = 2.0V (*1)	-650	-	µA
Input Current RST (*2)	I_{IN2}	V_{DD} = 5.5V V_{IN} = V_{DD}	-	+200	µA
Input Leakage Current P0, $\overline{EA}$	I_{LK}	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}	-10	+10	µA
Output Low Voltage P1, P2, P3	V_{OL1}	V_{DD} = 4.5V I_{OL1} = +2 mA	-	0.45	V
Output Low Voltage ALE, $\overline{PSEN}$, P0 (*3)	V_{OL2}	V_{DD} = 4.5V I_{OL2} = +4 mA	-	0.45	V
Output High Voltage P1, P2, P3	V_{OH1}	V_{DD} = 4.5V I_{OH1} = -100 µA	2.4	-	V
Output High Voltage ALE, $\overline{PSEN}$, P0 (*3)	V_{OH2}	V_{DD} = 4.5V I_{OH2} = -400 µA	2.4	-	V
Input Low Voltage (Except RST)	V_{IL1}	V_{DD} = 4.5V	0	0.8	V
Input Low Voltage RST (*4)	V_{IL2}	V_{DD} = 4.5V	0	0.8	V
Input Low Voltage XTAL1 (*4)	V_{IL3}	V_{DD} = 4.5V	0	0.8	V
Input High Voltage (Except RST)	V_{IH1}	V_{DD} = 4.5V	2.4	V_{DD} +0.2	V

DC Characteristics, continued

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
			MIN.	MAX.	
Input High Voltage RST (*4)	V_{IH2}	V_{DD} = 4.5V	2.4	V_{DD} +0.2	V
Input High Voltage XTAL1 (*4)	V_{IH3}	V_{DD} = 4.5V	3.5	V_{DD} +0.2	V

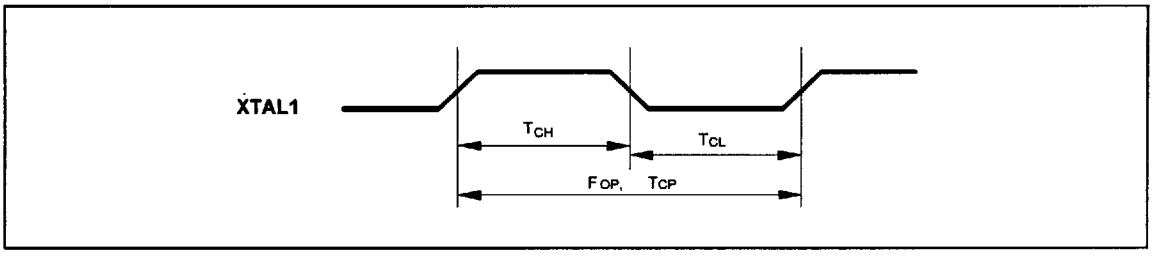
Notes:

1. Pins P1, P2 and P3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2V.
2. RST pin has an internal pull-down resistor.
3. P0, ALE, $\overline{PSEN}$ are in the external access mode.
4. XTAL1 is a CMOS input and RST is a Schmitt trigger input.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.8 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP -Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP -Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP -Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP -Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP -Δ	3 TCP	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP -Δ	-	3 TCP +Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP -Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{\text{WR}}$ Low	TDAW	3 TCP -Δ	-	3 TCP +Δ	nS
Data Valid to $\overline{\text{WR}}$ Low	TDAD	1 TCP -Δ	-	-	nS
Data Hold from $\overline{\text{WR}}$ High	TDWD	1 TCP -Δ	-	-	nS
$\overline{\text{WR}}$ Pulse Width	TDWR	6 TCP -Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

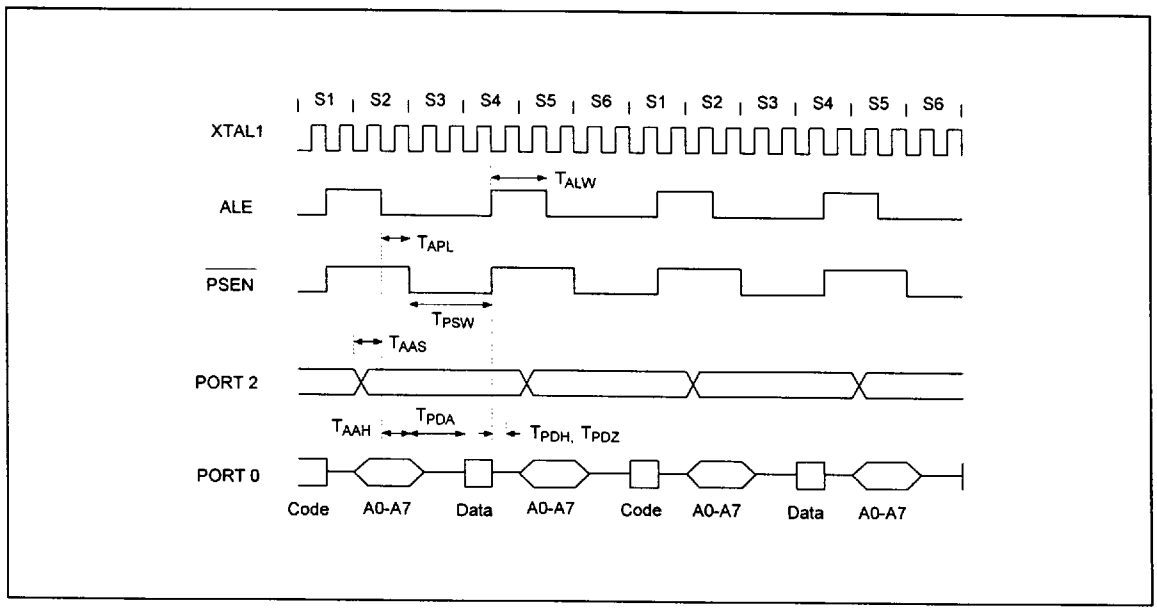
Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	TVPS	2.0	-	-	µS
Data Setup Time	TDS	2.0	-	-	µS
Data Hold Time	TDH	2.0	-	-	µS
Address Setup Time	TAS	2.0	-	-	µS
Address Hold Time	TAH	0	-	-	µS
$\overline{CE}$ Program Pulse Width for Program Operation	TPWP	95	100	105	µS
OECTRL Setup Time	TOCS	2.0	-	-	µS
OECTRL Hold Time	TOCH	2.0	-	-	µS
$\overline{OE}$ Setup Time	TOES	2.0	-	-	µS
$\overline{OE}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{OE}$	TOEV	-	-	150	nS

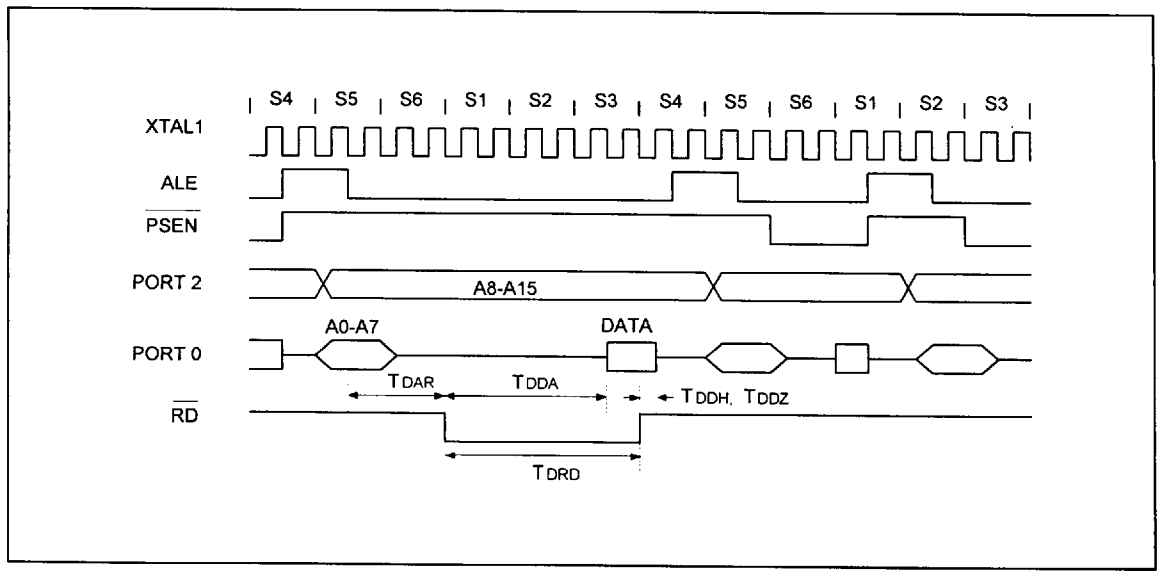
Note: Flash data can be accessed only in flash mode. The RST pin must pull in VH status, the ALE pin must pull in VL status, and the $\overline{PSEN}$ pin must pull in VH status.

TIMING WAVEFORMS

Program Fetch Cycle



Data Read Cycle



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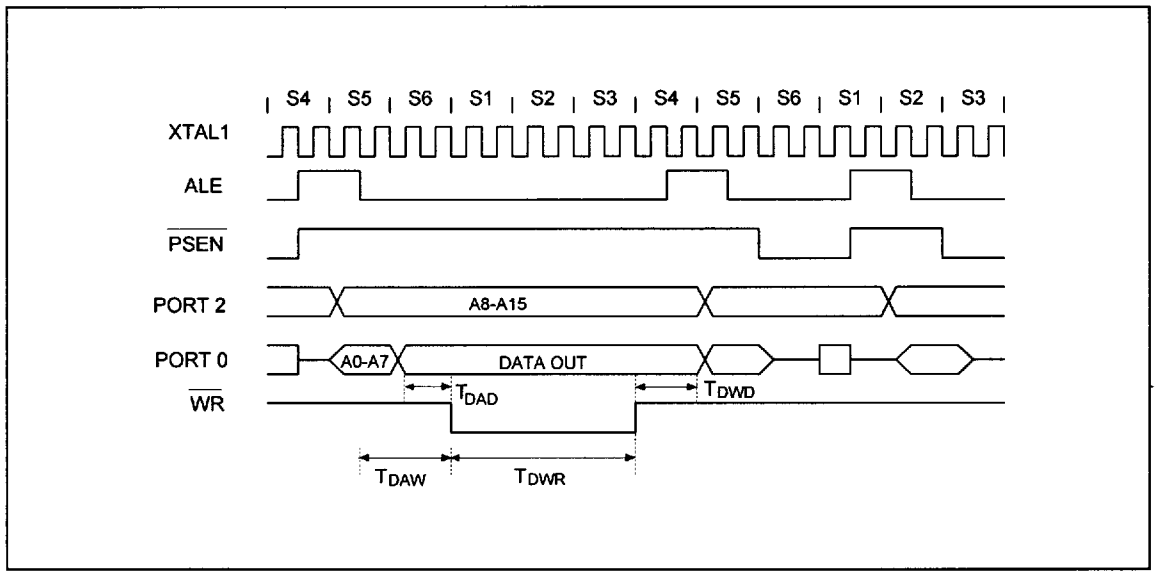
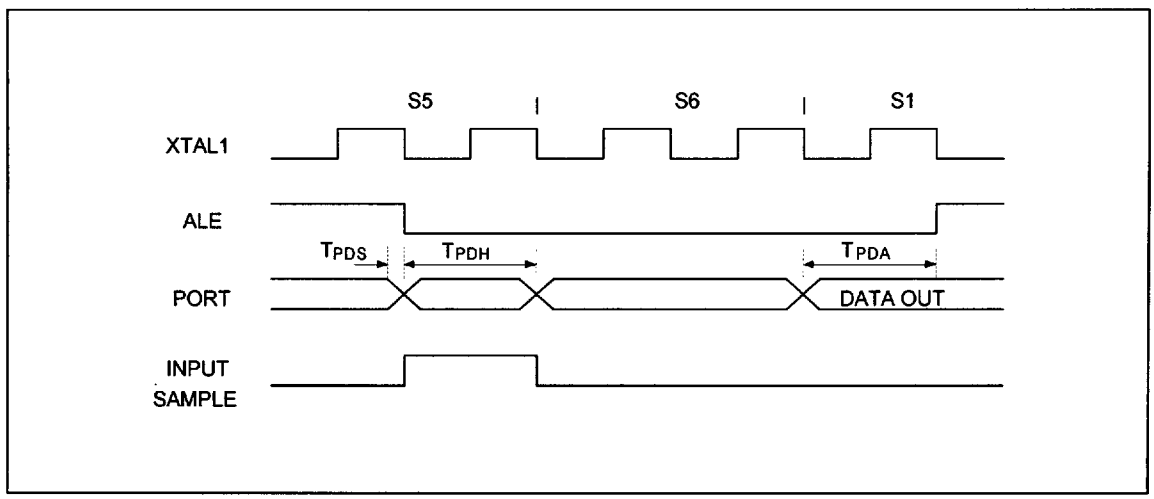
Timing Waveforms, continued

Data Write Cycle

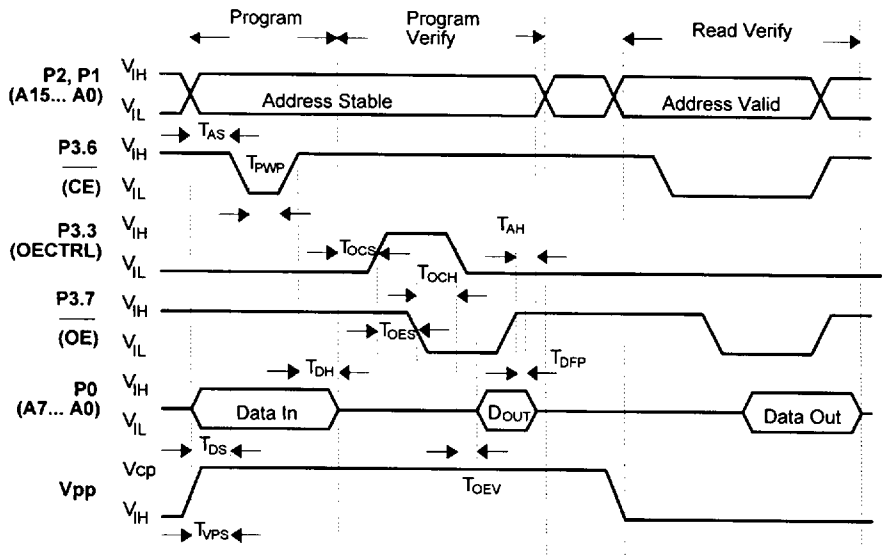


Port Access Cycle



Timing Waveforms, continued

Program Operation



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TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

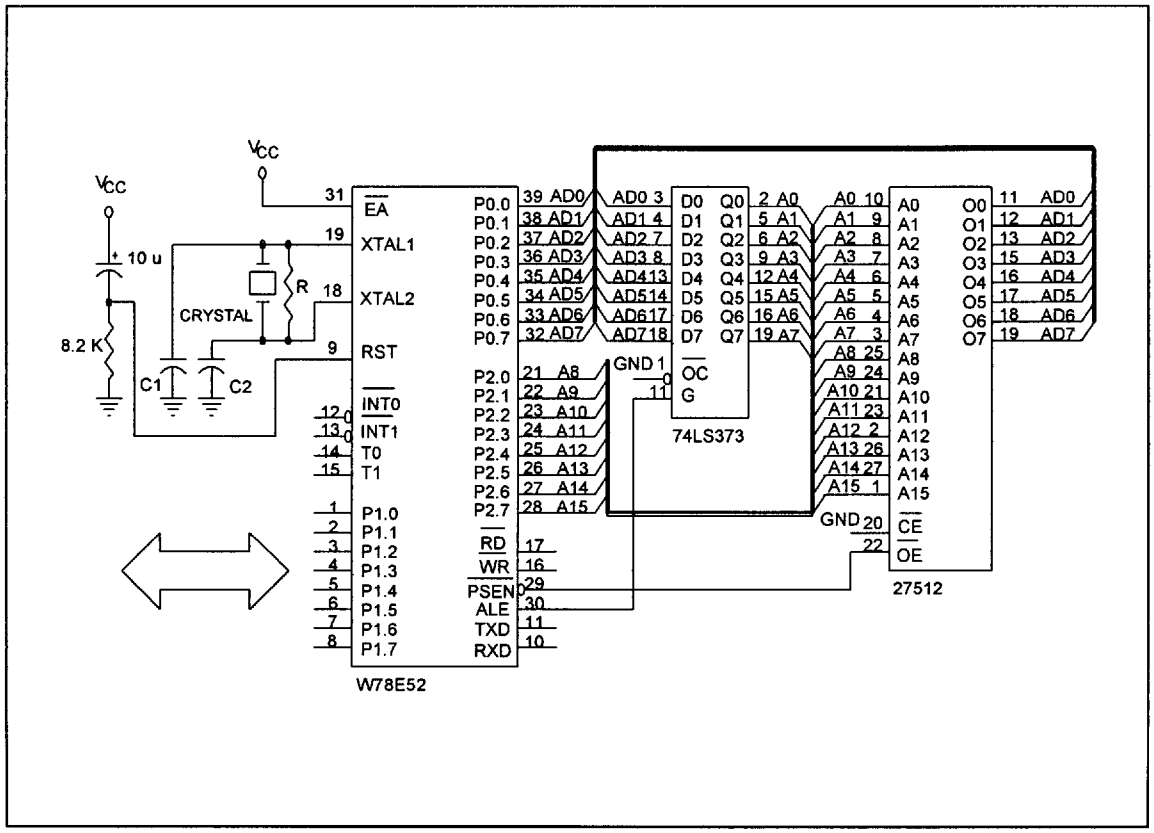

Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
24 MHz	15P	15P	-
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	6.8K

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

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Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

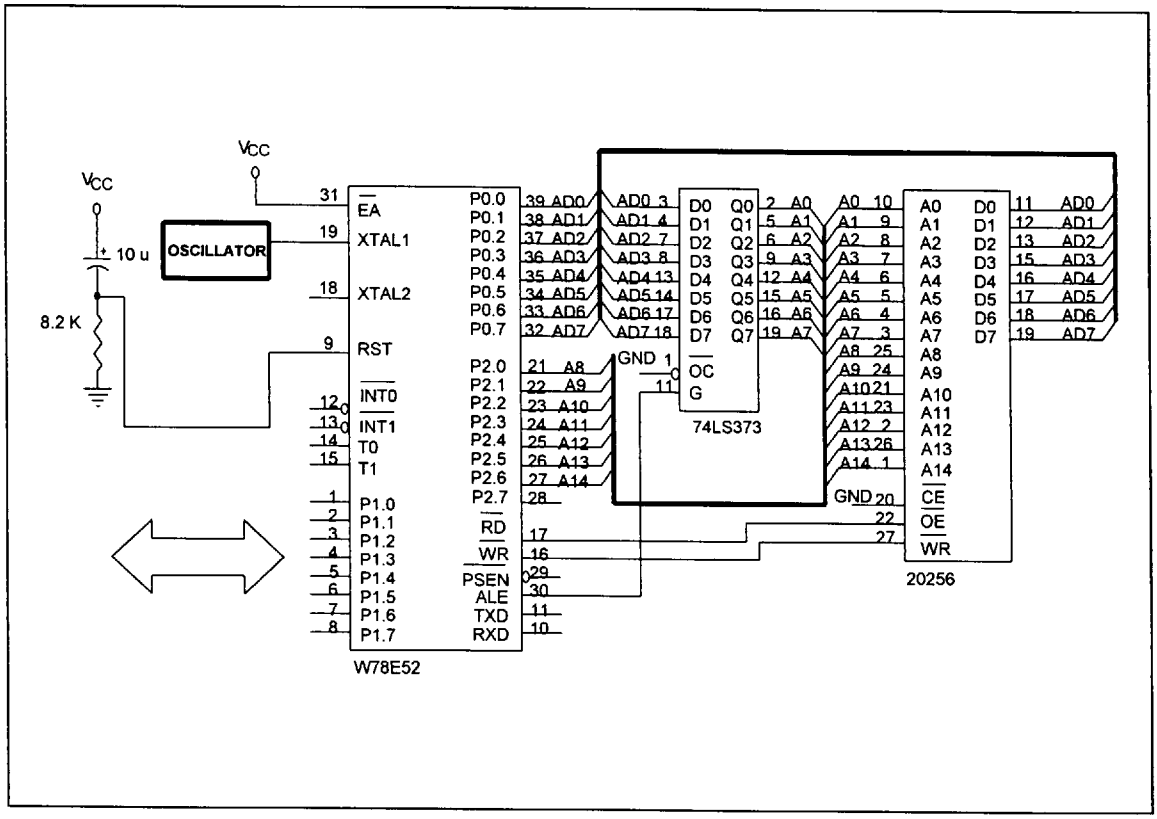

Figure B

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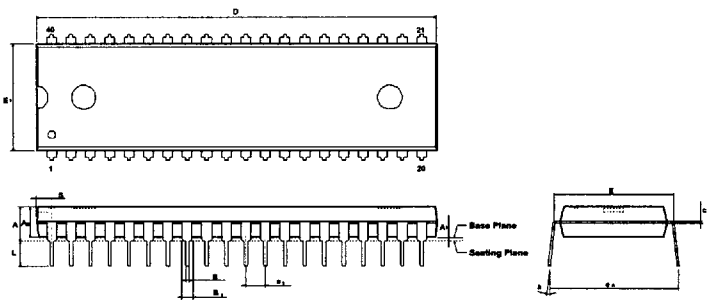
PACKAGE DIMENSIONS

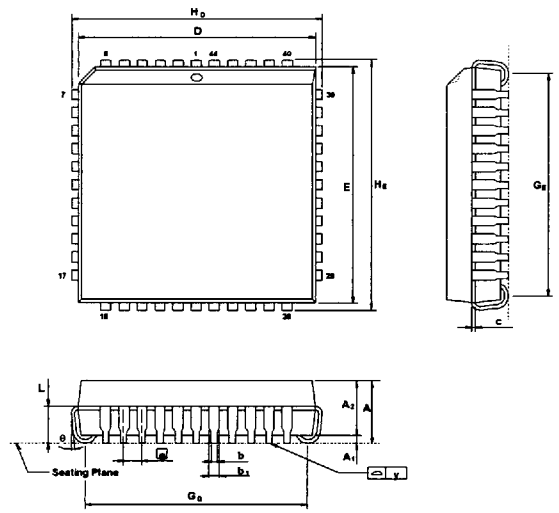
40-pin DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	15.90
G_E	0.590	0.610	0.630	14.99	15.49	15.90
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.286	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.