ADPCM VOICE SYNTHESIZER

PowerSpeech INTRODUCTION

The W523X series is a part of Winbond's line of *PowerSpeech* products. All of these products use similar programmable speech functions, instruction sets, mask options, pin configurations, and speech equations. Before developing their own *PowerSpeech* programs and codes, customers should review the application notes presented below.

1. Instruction Sets

Winbond *PowerSpeech* program instruction sets include unconditional instructions and conditional instructions. Most of these instructions are programmed by writing "LD (Load)" and "JP (Jump)" commands and by modifying the content of the R0, EN, STOP, and MODE registers.

Registers

A. R0 Register

R0 is an 8-bit register that stores the entry values of from 0 to 255 voice groups. The structure of this register is shown below:

R0:

Bit:	7	6	5	4	3	2	1	0

B. EN Register

EN is an 8-bit register that stores the rising/falling edge enable or disable status information for all trigger pins, which determines whether each trigger pin is retriggerable, non-retriggerable, overwrite, or non-overwrite. The 8-bit structure of this register and the rising or falling edge of the triggers corresponding to each bit are shown below:

EN:

Bit:	7	6	5	4	3	2	1	0
Trigger:	4r	3r	2r	1r	4f	3f	2f	1f

The digits 1 to 4 represent triggers 1 to 4, respectively; "r" represents the rising edge; and "f" represents the falling edge. When any one of the eight bits is set to "1," the rising or falling edge of the corresponding trigger pin can be enabled, interrupting the current state.

C. STOP Register

The STOP register stores stop output status information to determine the voltage level of each stop output pin. The 8-bit structure of this register and the stop output pin corresponding to each bit are shown below:

STOP:

Bit:	7	6	5	4	3	2	1	0
STOP:	X	X	X	X	X	STPC	STPB	STPA

"X" indicates a "don't care" bit.

D. MODE Register

The MODE register is used to store operand information to select among various operating modes as shown below.

MODE:

Bit:	7	6	5	4	3	2	1	0
MODE:	Flash/DC	LED2/STPC	TG4/LED2-STPC	X	X	X	X	X

Bit 7 is used to determine the output status of LED1 and/or LED2: Flash alternate or synchronous output (by mask option), or DC (LED will be lit constantly without flash).

Bit 6 and bit 5 together determine whether the I/O pin (i.e., pin 4) acts as a trigger input pin, LED output pin, or STOP output pin.

Commands

A. Unconditional Instructions

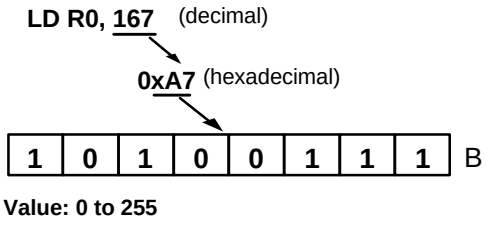
Load (LD) command:

This command can load value or operand data into the R0, EN, STOP, or MODE register.

LD R0, value:

This instruction is used to load a voice group entry value into register R0, as shown in the following example.

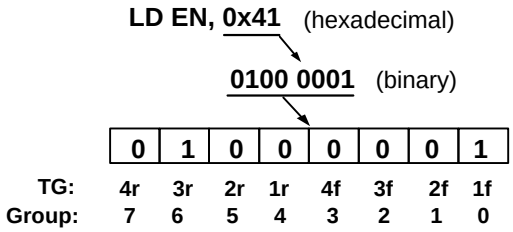
Example:



LD EN, operand:

This instruction is used to define the trigger interrupt settings by loading the operand message into register EN. The following example illustrates how the settings are defined.

Example:



a. When the rising edge of TG3 (3R) is activated, the EN register will cause TG3 to interrupt the current playing state and jump immediately to voice group 6, the voice group that corresponds to 3R.

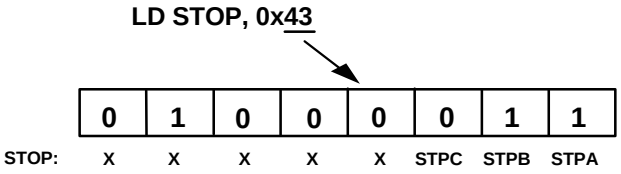
b. When the falling edge of TG1 goes active, the EN register will cause TG1 to interrupt the current playing state and jump immediately to voice group 0, the voice group that corresponds to 1F.

c. No action will be taken when the other trigger pins are pressed, because the corresponding bits are set to "0."

LD STOP, operand:

This instruction loads the operand message into the STOP register to set the output levels of the stop signals. When a particular STOP bit is set to "1," the corresponding stop signal will be an active low output.

Example:



a. The STPA and STPB output signals will be high active outputs.

b. The STPC output signal will be a low active output.

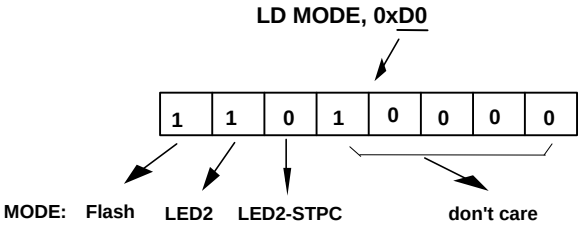
c. The second bit "1" is a "don't care" bit and so has no effect on the stop signal output setting.

LD MODE, operand:

This instruction is used to select among various operating modes. It loads an operand message into the MODE register to select one mode from each of several pairs of modes.

A "1" for one of these bits selects the first of the pair of modes indicated; a "0" selects the second of the pair. The following example describes the MODE setting of the W523X product.

Example:



a. The LED is set as a flash type

b. Pin 4 (TG4/LED2-STPC) is configured as either the LED2 or STPC output (determined by bit 6, LED2/STPC).

c. Pin 4 is configured as the LED2 output pin.

JUMP (JP) Command:

JP value:

Instructs device to jump directly to the voice group corresponding to the value indicated. The voice group value may range from 0 to 127.

JP R0:

Instructs device to jump to whatever voice group is indicated by the value currently stored in register R0.

B. Conditional Instructions:

Conditional instructions are executed only when the conditions specified in the instructions hold. The conditional instructions are listed below. An explanation of the notation used in the instructions follows.

(Note: There are no conditional instructions for LD MODE.)

Load (LD) command:

LD R0, value @LAST:

Load the voice group entry value into R0 when the last global repeat sound cycle is finished.

LD R0, value @TGn_HIGH (or_LOW):

If the n-th (n: 1 to 4) trigger pin status is kept at "High" (or "Low") voltage level, then load the value into R0 register.

LD EN, operand @LAST:

Load the operand message into EN register when the last global repeat sound cycle is finished.

LD STOP, operand @LAST:

Load the operand message into STOP register when the last global repeat sound cycle is finished.

Jump (JP) command:

JP value @LAST:

When the last global repeat sound cycle is finished, jump to the group entry value indicated (range: 0 to 127) and begin execution.

JP R0 @LAST:

When the last global repeat sound cycle is finished, jump to the group entry value indicated by the R0 register and begin execution.

JP value @TGn_HIGH (or _LOW):

If the n-th (n: 1 to 4) trigger pin is kept at "High" (or "Low") voltage level, then jump to the indicated value (range: 0 to 127) and begin execution.

JP R0 @TGn_HIGH (or _LOW):

If the n-th (n: 1 to 4) trigger pin is kept at "High" (or "Low") voltage level, then jump to the group entry value indicated by the R0 register and begin execution.

C. End Instruction:

END:

This command instructs the chip to cease all activity immediately.

D. Instruction Set List:

	INSTRUCTION	RANGE	DESCRIPTION	DEFAULT VALUE
Unconditional	LD R0, value	0–255	R0 ¡ö value	0000 0000
	LD EN, operand	–	EN ¡ö operand	1111 1111
	LD STOP, operand	–	STOP ¡ö operand	xxxx x111
	LD MODE, operand	–	MODE ¡ö operand	W523X: 111x xxxx
	JP value	0–127	Jump to the group entry value indicated	
	JP R0	0–255	Jump to the group entry indicated by R0	
Conditional	LD R0, value @LAST	0–255	If last global repeat finished, R0 ¡ö value	
	LD R0, value @TGn_HIGH	0–255	If TGn (n: 1–4) status is high level, R0 ¡ö value	
	LD R0, value @TGn_LOW	0–255	If TGn (n: 1–4) status is low level, R0 ¡ö value	
	LD EN, operand @LAST	–	If last global repeat finished, EN ¡ö operand	
	LD STOP, operand @LAST	–	If last global repeat finished, STOP ¡ö operand	
	JP value @LAST	0–127	If last global repeat finished, jump to the group entry value indicated	
	JP R0 @LAST	0–255	If last global repeat finished, jump to the group entry value indicated in R0	
	JP value @TGn_HIGH	0–127	If TGn (n: 1–4) status is high level, jump to the group entry value indicated	
	JP value @TGn_LOW	0–127	If TGn (n: 1–4) status is low level, jump to the group entry value indicated	
	JP R0 @TGn_HIGH	0–255	If TGn (n: 1–4) status is high level, jump to the group entry value indicated in R0	

Instruction Set List, continued

	INSTRUCTION	RANGE	DESCRIPTION	DEFAULT VALUE
Conditional	JP R0 @TGn_LOW	0–255	If TGn (n: 1–4) status is low level, jump to the group entry value indicated in R0	
END	END	–	Stop all activity and enter standby state	

2. Mask Option Description

The mask options of the *PowerSpeech* are used to select features that cannot be programmed through the chip's registers. The W523X provides four mask options, which are listed in the following table:

MASK OPTION	INSTRUCTION	DEMO CHIP OPTION
LED flash type (Asynchronous/Synchronous)	LED_ASYN; (default) LED_SYN	–
LED	LED_3Hz; (default) LED_6Hz	–
LED1: section-controlled (Yes/No)	LED1_S_CTL; (default) LED1_S_OFF	–
LED2: section-controlled /STPC-controlled	LED2_S_CTL; (default) LED2_STC_CTL	–

Notes:

1.The demo chip for the W523X series is the W5230.

2. The mask options can be configured automatically by the W5230.

3. Speech Equation Description

Speech equations are used to define the combination of playback sounds. The following is an example of the speech equation format:

```
GR = N
H4+m1*Sound1_FL+m2*Sound2_FL+SIL[1FFFF]+...T4
END
```

where

GR = N defines the number of global repeats (from 1 to 16);

m1 and **m2** define the number of local repeats (from 1 to 7);

Sound1 and **Sound2** are files containing ADPCM converted voice data;

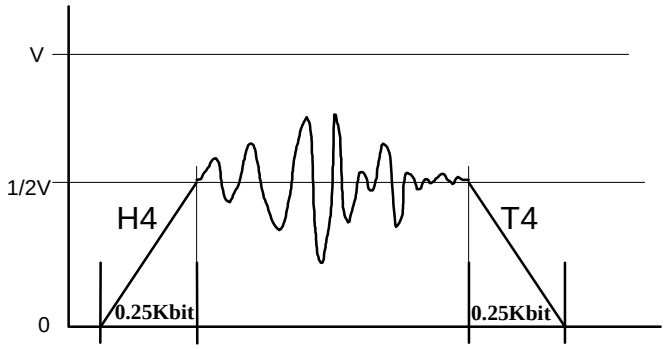
_FL is the section control setting, for which the parameters F and L are as follows:

F	2
Frequency	6 KHz

L	1	0
LED status	On	Off

SIL[1FFFF] is a period of silence of length 1FFFF.

H4 and **T4** are the Head file and Tail file with 4-bit ADPCM data format. These two files can be used to eliminate the popping sound when the sound starts and stops. The following is a sample waveform:

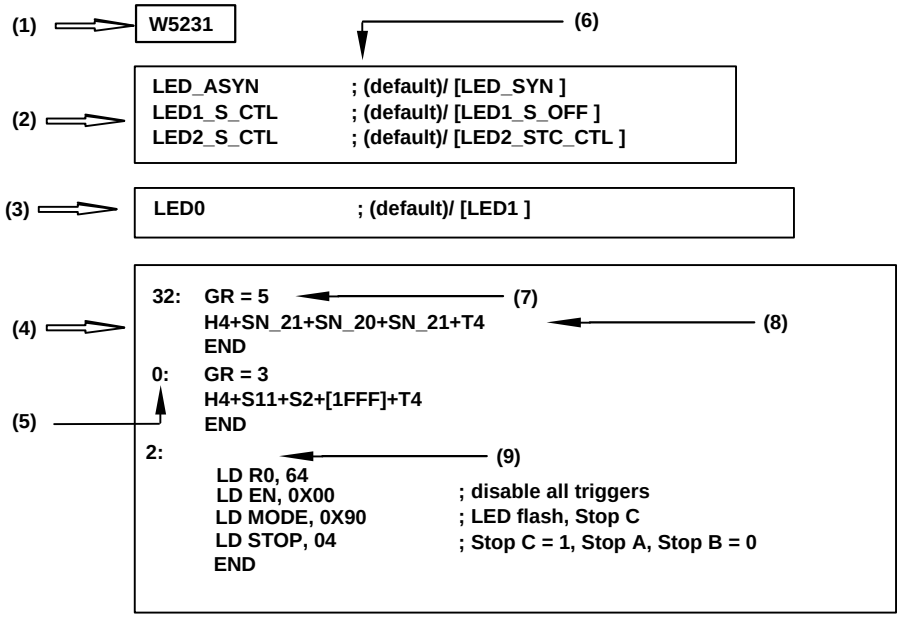


4. Programmable Power-on Initialization

Whenever the *PowerSpeech* is powered on, the programs contained in the 32nd voice group will be executed immediately. Thus the user can write programs into this group to set the initial power-on state. If the user does not wish to execute any programs at power-on, an "END" instruction should be entered in group 32.

5. *PowerSpeech* Program Format

The *PowerSpeech* enables users to define the functions of their products using the *PowerSpeech* programming language. An example (for reference only) of the *PowerSpeech* program format is shown below. (Explanatory notes follow the example.)



Notes:

(1) **Bodies:** The user must first define the *PowerSpeech* body to be used, or else an error message will appear during compiling. The *PowerSpeech* bodies include the following:

W523x: W5231, W5232, W5233, W5234

(2) **Mask Options:** See section 3.2.3 above.

(3) **Declarations:** LED on/off state, as follows:

LED on/off:

LED0: LED off (default)

LED1: LED on

(4) **Program body**: Write application program and speech operations, including the following:

Define entry point of speech group.

Determine number of global repeats.

Describe speech equations.

Define the register values.

(5) **Group body:** Define the voice group entry point.

PRODUCT	GROUP ENTRY POINTS	TG H/W ENTRY POINTS	POWER-ON ENTRY POINT
W523x	0-255	0-7	32

(6) **Note:** A semicolon (";") is used to distinguish characters that are not part of the program. Characters written to the right of the semicolon are not considered part of the content of the program.

(7) **Global Repeat:** The global repeat instruction is "GR = n," where n is from 1 to 16. This instruction must be placed on the same line as the group entry point. The global repeat instruction can be represented in three ways, as shown below.

```
0: GR = 3
    H4+sound+T4
    END
```

```
0: 3
    H4+sound+T4
    END
```

```
0:    ; default = 1
    H4+sound+T4
    END
```

(8) **Speech equation:** See section 3.2.4 above.

(9) **Blank:** A voice group entry point must be followed by one full blank line without any instructions or speech equations. The "GR = n" instruction must follow the entry point, however.

6. Programming Examples (for reference only)

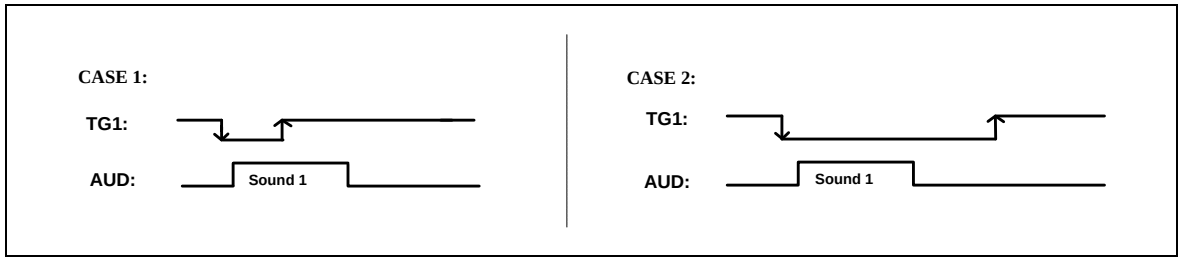
This section presents several examples of how the functions of the *PowerSpeech* may be programmed. Customer programs should be written in ASCII code using a text editor; after compiling, the sound effects resulting from the programs can be tested using a Winbond demo board.

Example1: Four playing mode settings:

a. One-shot Trigger Mode

```
0:                  ; TG1 falling edge group entry point
   LD EN, 0X01      ; Enable TG1 falling edge input only
   H4+sound+T4
   END
```

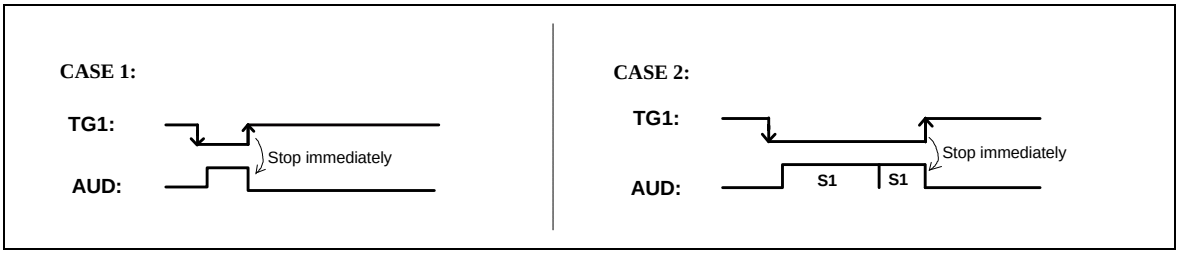
The timing diagram for this example is shown below:



b. Level Hold Trigger Mode

```
0:                  ; TG1 falling edge group entry point
   LD EN, 0X11      ; Enable TG1 falling and rising edge input
   H4+sound1+T4
   JP 0
4:                  ; TG1 rising edge group entry point
   END
```

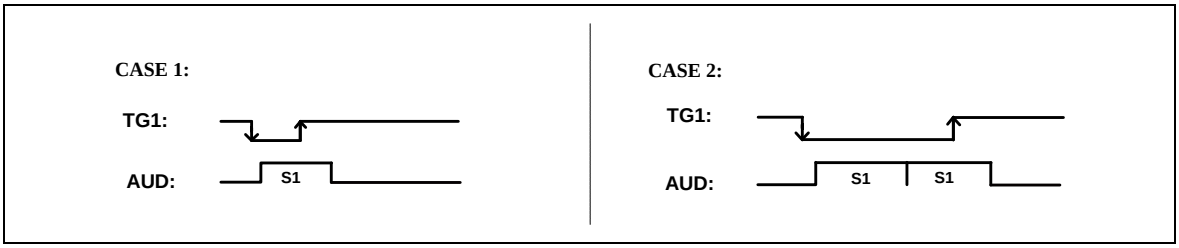
The timing diagram is shown below:



c. Completed Cycle Level Hold

```
0:                  ; TG1 falling edge group entry point
   LD EN, 0X01      ; Enable TG1 falling edge input only
   H4+sound1+T4
   JP 0 @TG1_LOW    ; If TG1 state is low, jump to 0 entry point
   END
```

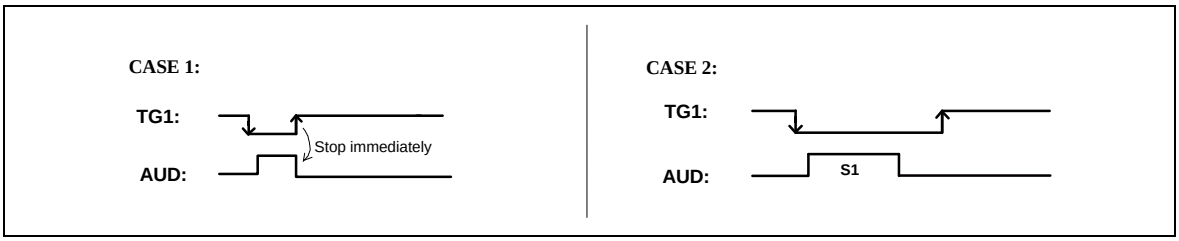
The timing diagram is shown below:



d. Single Cycle Level Hold

```
0:                  ; TG1 falling edge group entry point
   LD EN, 0X11      ; Enable TG1 falling and rising edge input
   H4+sound1+T4
   END
4:
   END
```

The timing diagram is shown below:



Example 2: Retriggerable and Non-retriggerable setting

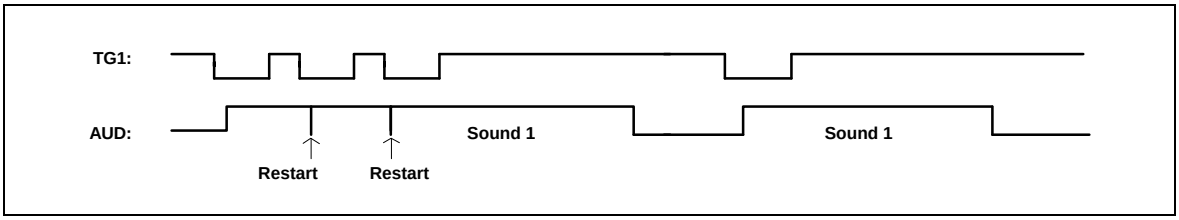
a. Retriggerable:

0: LD EN, 0x01

.
.
.

END

The timing diagram is shown below:



b. Non-retriggerable:

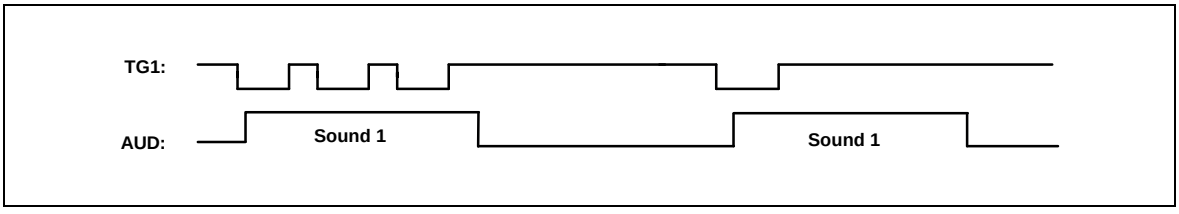
0: LD EN, 0x00

.
.
.

LD EN, 0x11

END

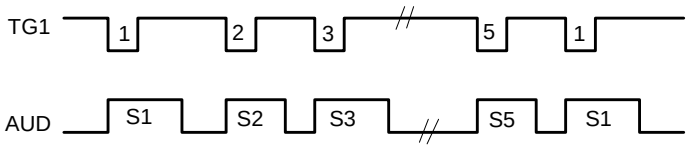
The timing diagram is shown below:



Example 3: Serial Playing Mode (5 segments)

```
W5231
32:
    LD R0, 8
    LD EN, 0X01
    END
0:
    JP R0
8:
    LD R0, 9
    H4+S1+T4
    END
9:
    LD R0, 10
    H4+S2+T4
    END
10:
    LD R0, 11
    H4+S3+T4
    END
11:
    LD R0, 12
    H4+S4+T4
    END
12:
    LD R0, 8
    H4+S5+T4
    END
```

The timing diagram is shown below:



Example 4: Random (1)

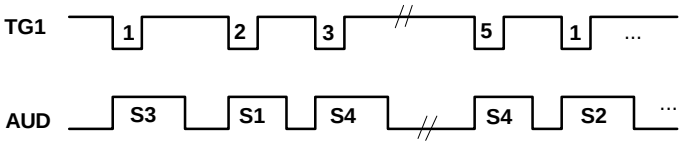
```
W5231
32:
    LD EN, 0X01
    LD R0, 8
    END
0:
    LD EN, 0X00
    JP R0
8:
    JP 18 @TG1_HIGH
9:
    JP 19 @TG1_HIGH
18:
    H4+S1+T4
    LD R0, 9
    JP 31
19:
    H4+S2+T4
    LD R0, 8
    JP 31
20:
    H4+S3+T4
    LD R0, 11
```

Example 4, continued

```
10:
    JP 20 @TG1_HIGH
11:
    JP 21 @TG1_HIGH
    JP 8
```

```
    JP 31
21:
    H4+S4+T4
    LD R0, 10
31:
    LD EN, 0X01
    END
```

The timing diagram is shown below:



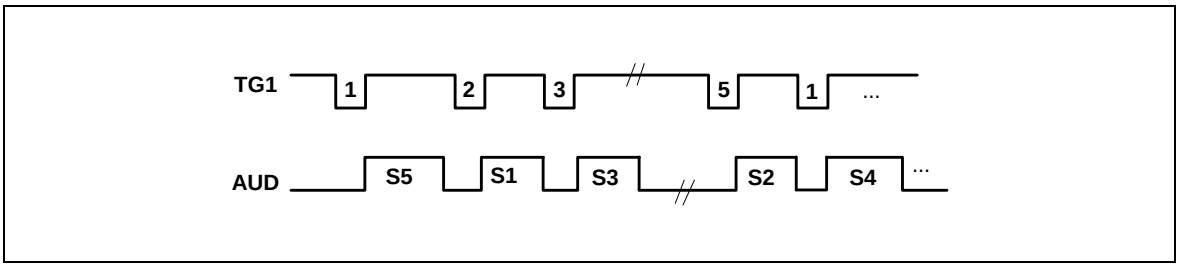
Example 5: Random (2)

```
W5231
32:
    LD EN, 0X11
    END
0:
    LD R0, 8
    [300]
    LD R0, 9
    [300]
    LD R0, 10
    [300]
    LD R0, 11
    [300]
    LD R0, 12

    JP 0
4:
    JP R0
```

```
8:
    H4+S4+T4
    END
9:
    H4+S1+T4
    END
10:
    H4+S5+T4
    END
11:
    H4+S3+T4
    END
12:
    H4+S2+T4
    END
```

The timing diagram is shown below:



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