**OKI** Semiconductor

# MSM6585

**ADPCM Voice Synthesis IC**

## GENERAL DESCRIPTION

The MSM6585 is an version-up product of the MSM5205 voice synthesis IC. Mainly improved points are improvement for the precision of an internal DA converter, a built-in low-pass filter, and expansion on the sampling frequency. The MSM6585 does not include a control circuit to drive an external memory similar to the MSM5205. Therefore, the MSM6585 can be connected with not only semiconductor memories, but other memory media (CD-ROM, etc.) by the control of CPU.

## FEATURES

- 4-bit ADPCM method
- Built-in 12-bit DA converter
- Built-in low-pass filter (LPF) (–40dB/oct)
- Sampling frequencies:  4k/8k/16k/32kHz
- Master clock frequency (ceramic oscillator) :  640kHz
- Voice data synthesis :  Supported by voice analysis editing tools AR76-202 and AR203
- Package options :
    18-pin plastic DIP (DIP18-P-300-2.54) (Product name :  MSM6585RS)
    24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name :  MSM6585 GS-K)
    30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name :  MSM6585 GS-AK)

## DIFFERENCES BETWEEN MSM6585 AND MSM5205

|  | MSM6585 | MSM5205 |
|---|---|---|
| • Master clock frequency: | 640kHz | 384kHz |
| • Sampling frequency: | 4k/8k/16k/32kHz | 4k/6k/8kHz |
| • ADPCM bit length: | 4-bit | 3-bit/4-bit |
| • DA Converter: | 12-bit | 10-bit |
| • Low-pass filter: | Included (–40dB/oct) | Not included |
| • Overflow preventing circuit: | Included | Not included |
| • Power supply voltage: | 4.5 to 5.5V | 3.0 to 6.0V |
| • Operating current consumption: | 10mA | 4mA |
| • Operating temperature: | –40 to +85°C | –30 to +70°C |

- D3 to D0 input timing
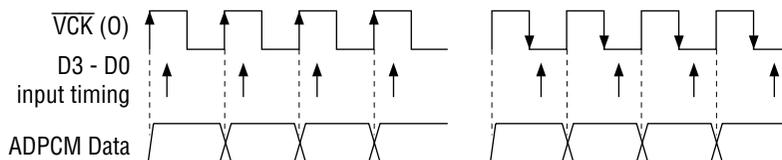
## BLOCK DIAGRAM
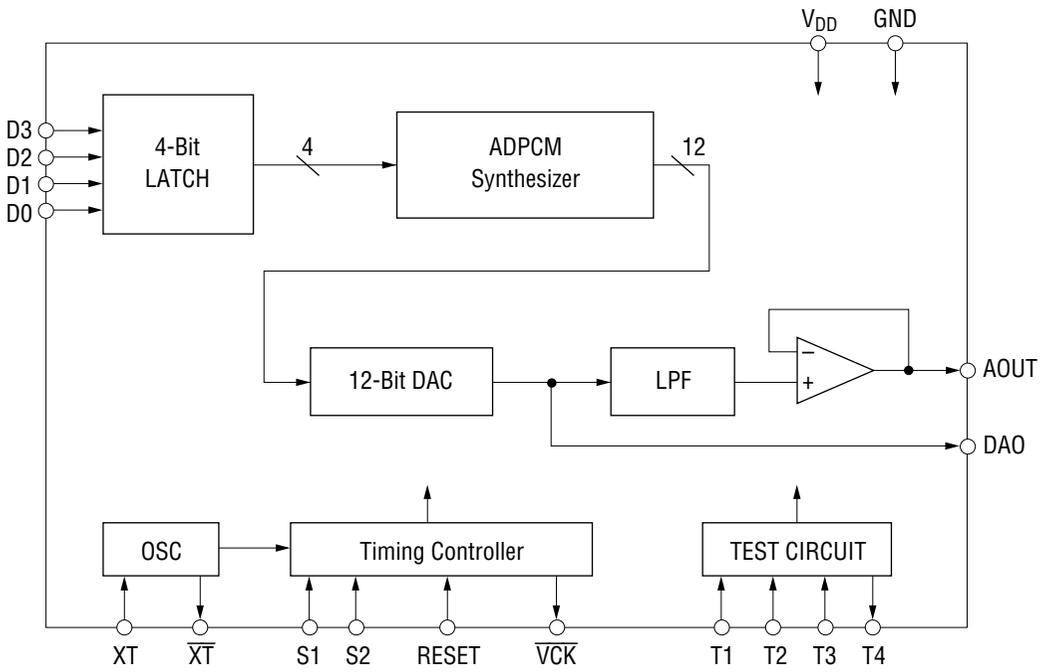
## PIN CONFIGURATION (TOP VIEW)

| | | |
|---|---|---|
| S1 | 1 | 18 | $V_{DD}$ |
| S2 | 2 | 17 | $\overline{XT}$ |
| T3 | 3 | 16 | XT |
| D0 | 4 | 15 | RESET |
| D1 | 5 | 14 | $\overline{VCK}$ |
| D2 | 6 | 13 | T2 |
| D3 | 7 | 12 | T1 |
| T4 | 8 | 11 | DAO |
| GND | 9 | 10 | AOUT |

**18-Pin Plastic DIP**

| | | |
|---|---|---|
| S1 | 1 | 24 | $V_{DD}$ |
| S2 | 2 | 23 | $\overline{XT}$ |
| T3 | 3 | 22 | XT |
| NC | 4 | 21 | NC |
| D0 | 5 | 20 | RESET |
| NC | 6 | 19 | NC |
| D1 | 7 | 18 | $\overline{VCK}$ |
| D2 | 8 | 17 | T2 |
| NC | 9 | 16 | T1 |
| D3 | 10 | 15 | NC |
| T4 | 11 | 14 | DAO |
| GND | 12 | 13 | AOUT |

NC : No connection

**24-Pin Plastic SOP**

| | | |
|---|---|---|
| S1 | 1 | 30 | $V_{DD}$ |
| S2 | 2 | 29 | $\overline{XT}$ |
| NC | 3 | 28 | NC |
| NC | 4 | 27 | NC |
| NC | 5 | 26 | NC |
| T3 | 6 | 25 | XT |
| D0 | 7 | 24 | RESET |
| D1 | 8 | 23 | $\overline{VCK}$ |
| D2 | 9 | 22 | T2 |
| D3 | 10 | 21 | T1 |
| NC | 11 | 20 | NC |
| NC | 12 | 19 | NC |
| NC | 13 | 18 | NC |
| T4 | 14 | 17 | DAO |
| GND | 15 | 16 | AOUT |
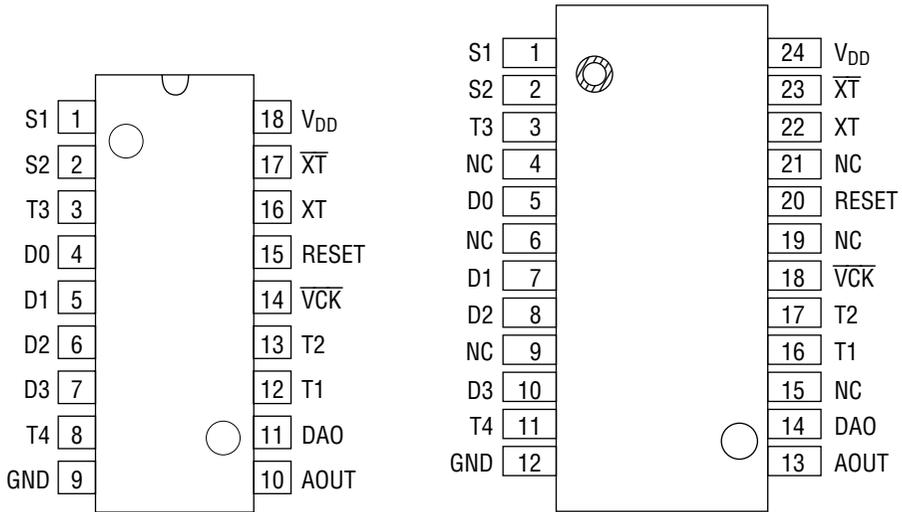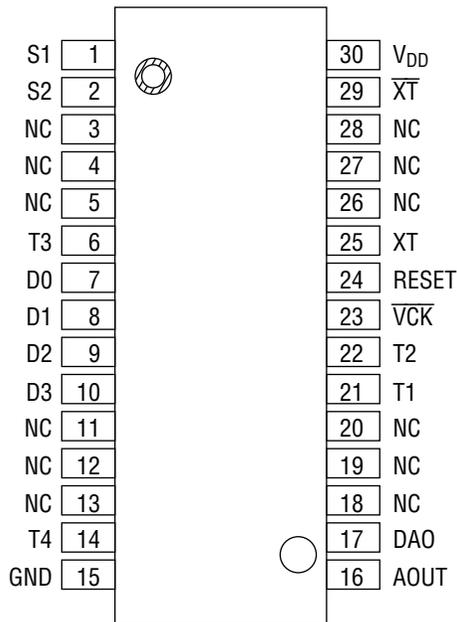
NC : No connection

**30-Pin Plastic SSOP**

## PIN DESCRIPTION

| Pin | | | Symbol | Type | Description |
|---|---|---|---|---|---|
| DIP | SOP | SSOP | | | |
| 1 | 1 | 1 | S1 | I | Pins to determine the sampling frequency. The sampling frequencies of 32k, 16k, 8k, and 4kHz can be selected by combinations. (See the sampling frequencies in FUNCTIONAL DESCRIPTION on the selection of combinations.) |
| 2 | 2 | 2 | S2 | | |
| 3 | 3 | 6 | T3 | I | Pin to test the internal circuit. Set this pin to a high level or make it open because it has a built-in pull-up resistor. |
| 4-7 | 5, 7, 8, 10 | 7-10 | D0-D3 | I | Input pins for ADPCM data. Pin to test the internal circuit. Make this pin open. |
| 8 | 11 | 14 | T4 | O | Pin to test the internal circuit. Make this pin open. |
| 9 | 12 | 15 | GND | — | Ground pin |
| 10 | 13 | 16 | AOUT | O | Pin to output the analog voice from the low-pass filter. Connect a 0.01 $\mu$F capacitor to this pin. (See the AOUT connecting circuit in FUNCTIONAL DESCRIPTION on the connecting circuit.) |
| 11 | 14 | 17 | DAO | O | Pin to output the analog voice from the DA converter. |
| 12 | 16 | 21 | T1 | I | Pins to test the internal circuit. Set these pins to a low level or make them open because pull-down resistors are included. |
| 13 | 17 | 22 | T2 | | |
| 14 | 18 | 23 | $\overline{\text{VCK}}$ | O | This pin outputs the sampling frequency selected by the combinations of S1 and S2. The voice synthesis starts or stops by synchronizing with $\overline{\text{VCK}}$. |
| 15 | 20 | 24 | RESET | I | Reset pin. The voice synthesis circuit is initialized by synchronizing with $\overline{\text{VCK}}$. If this pin is set to a high level, the D0 to D3 data inputs are disabled by synchronizing with $\overline{\text{VCK}}$. The AOUT and DA0 pins output 1/2 $V_{DD}$ and become the state of no voice. |
| 16 | 22 | 25 | XT | I | Pin to connect an oscillator. When the external clock is used, input it from this pin. |
| 17 | 23 | 29 | $\overline{\text{XT}}$ | O | Pin to connect an oscillator. When the external clock is used, make this pin open. |
| 18 | 24 | 30 | $V_{DD}$ | — | Power supply pin. Insert a bypass capacitor of 0.1 $\mu$F or more between this pin and the GND pin. |

## ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | Ta = 25°C | −0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | Ta = 25°C | −0.3 to $V_{DD}$+0.3 | V |
| Storage Temperature | $T_{STG}$ | — | −55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | — | 4.5 to 5.5 | V |
| Operating Temperature | $T_{op}$ | — | −40 to +85 | °C |
| Master Clock Frequency | $f_{OSC}$ | oscillator connection | 640 | kHz |

## ELECTRICAL  CHARACTERISTICS

### DC Characteristics

($V_{DD}$=4.5 to 5.5V, GND=0V, Ta=−40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| "H" Input Voltage | $V_{IH}$ | — | $0.8{\times}V_{DD}$ | — | $V_{DD}$+0.1 | V |
| "L" Input Voltage | $V_{IL}$ | — | −0.1 | — | $0.2{\times}V_{DD}$ | V |
| "H" Output Voltage | $V_{OH}$ | VCK: $I_{OH}$ = −40µA | $V_{DD}$−0.4 | — | — | V |
| "L" Output Voltage | $V_{OL}$ | VCK: $I_{OL}$ = 40µA | — | — | 0.4 | V |
| "H" Input Current | $I_{IH1}$ | T1, T2, RESET: $V_{IH}$ = $V_{DD}$ | 20 | 150 | 400 | µA |
| "H" Input Current | $I_{IH2}$ | S1, S2, D0 - D3, T3: $V_{IH}$ = $V_{DD}$ | — | — | 10 | µA |
| "H" Input Current | $I_{IH3}$ | XT: $V_{IH}$ = $V_{DD}$ | — | — | 20 | µA |
| "L" Input Current | $I_{IL1}$ | T3: $V_{IL}$ = 0V | −400 | −120 | −20 | µA |
| "L" Input Current | $I_{IL2}$ | S1, S2, D0 - D3, T1, T2, RESET: $V_{IL}$=0V | −10 | — | — | µA |
| "L" Input Current | $I_{IL3}$ | XT=$V_{IL}$=0V | −20 | — | — | µA |
| Current Consumption | $I_{DD}$ | $f_{OSC}$=640kHz, No load | — | 5 | 10 | mA |
| DA Output Relative Error | $\lvert V_{DAE} \rvert$ | No load | — | — | 40 | mV |
| DA Output Impedance | $R_{DAO}$ | — | 10 | — | 40 | kΩ |
| LPF Load Resistance | $R_{AOUT}$ | — | 50 | — | — | kΩ |

## AC Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Original Oscillation Duty Cycle | $f_{duty}$ | — | 40 | 50 | 60 | % |
| RESET Input Pulse Width | $t_{W(RST)}$ | $f_{SAM} =$ 4kHz ⋯      $t_{VCK} =$ 250µs | $2 \times t_{VCK}$ | — | — | µs |
| Data Setup Time | $t_S$ | = 8kHz ⋯      = 125µs<br>=16kHz ⋯      = 62.5µs | — | — | 3 | µs |
| Data Hold Time | $t_H$ | =32kHz ⋯      =31.25µs | $t_{VCK}/2$ | — | — | µs |

When data is shared with the MSM5205, note that the D3 to D0 selection timings of the MSM6585 and MSM5205 are different. (Refer to DIFFERENCES BETWEEN MSM6585 AND MSM5205.)

## TIMING DIAGRAM
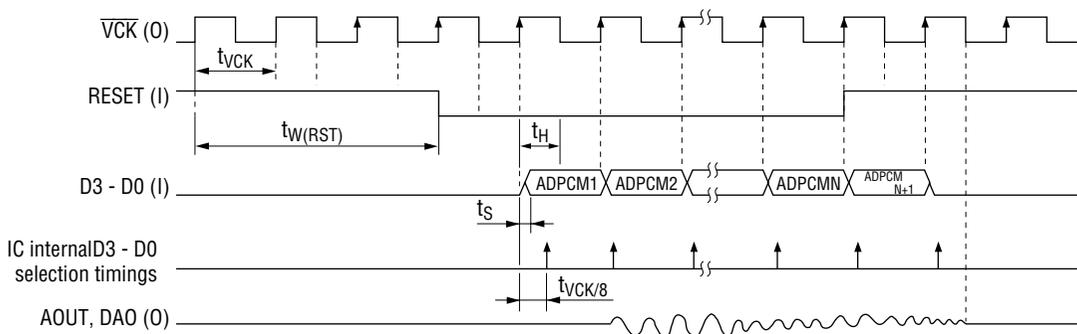


The $\overline{VCK}$ clock rising and falling edges are reversed between the MSM5205 and the MSM6588, as indicated in DIFFERENCES BETWEEN MSM6585 AND MSM5205.
Note that the MSM6585 cannot accept data if the MSM5205 controls to repeat valid and invalid each half cycle, when the MSM5205 is replaced with the MSM6585.

## FUNCTIONAL DESCRIPTION

1.　　　Sampling Frequency

The relationship of the sampling frequencies on S1 and S2, and the cutoff frequencies are listed below.

| S1 | S2 | Sampling frequency ($f_{SAM}$) | Cutoff frequency ($f_{CUT}$) |
|----|----|-------------------------------|------------------------------|
| L | L | 4 kHz | 1.6 kHz |
| H | L | 8 kHz | 3.2 kHz |
| L | H | 16 kHz | 6.4 kHz |
| H | H | 32 kHz | 12.8 kHz |

2.　　　AOUT Connecting Circuit

Connect a 0.01µF capacitor to the AOUT pin. The circuit diagram is as shown below.
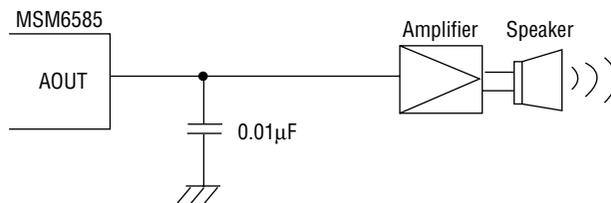


Even when the DAO pin is used, connect a 0.01µF capacitor to the AOUT pin. This capacitor is used for the improvement of a voice quality.

3.　　　Voice Output

The MSM6585 has two voice output pins. The DAO is direct output pin from the internal DA converter. The AOUT is a pin to output a voice after which the DAO output passed a built-in LPF.

3.1　　　DA Converter Output Waveform

The output amplitude from the DA converter is max. $(4095/4096) \times V_{DD}$ and becomes a stair step waveform synchronized with the sampling frequency. The DAO output impedance varies in the ranges from 10kΩ to 40kΩ. Therefore, determine the filter constant so that the resistor variation does not have influence on the cutoff frequency of the filter.

3.2     Low-pass Filter Output

The cutoff frequency of the low-pass filter varies in proportion to the sampling frequency. The following figure shows the low-pass filter characteristics in the sampling frequency 8kHz.
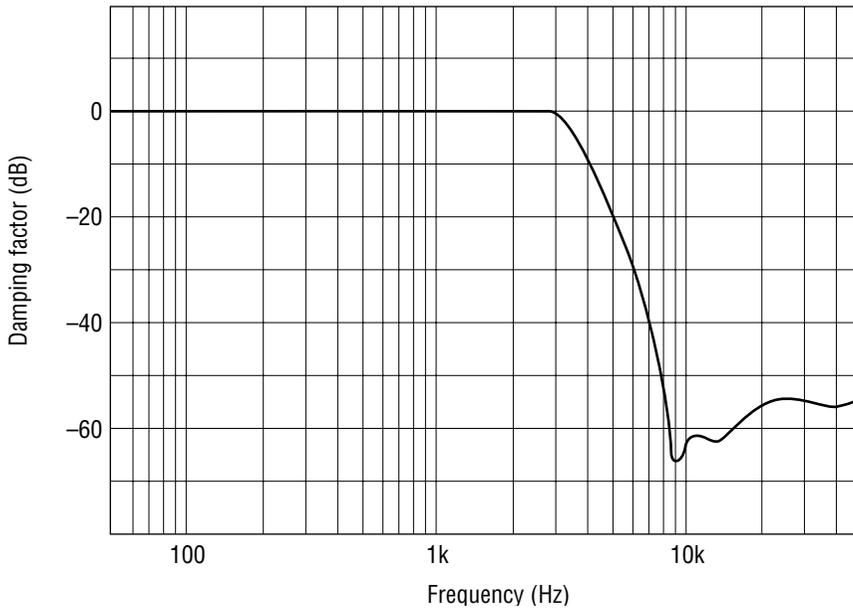


4.      Oscillation

Following show external circuit diagrams using a ceramic resonator, KBR-640B made by Kyocera Corp. and CSB640P made by Murata MFG. Co., Ltd.
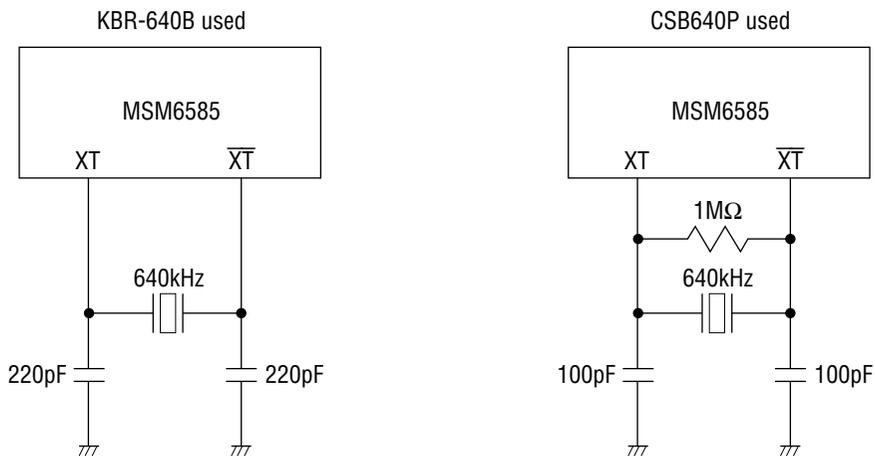
## APPLICATION CIRCUITS

### Centronics Interface Circuit (sampling frequency : 8kHz)
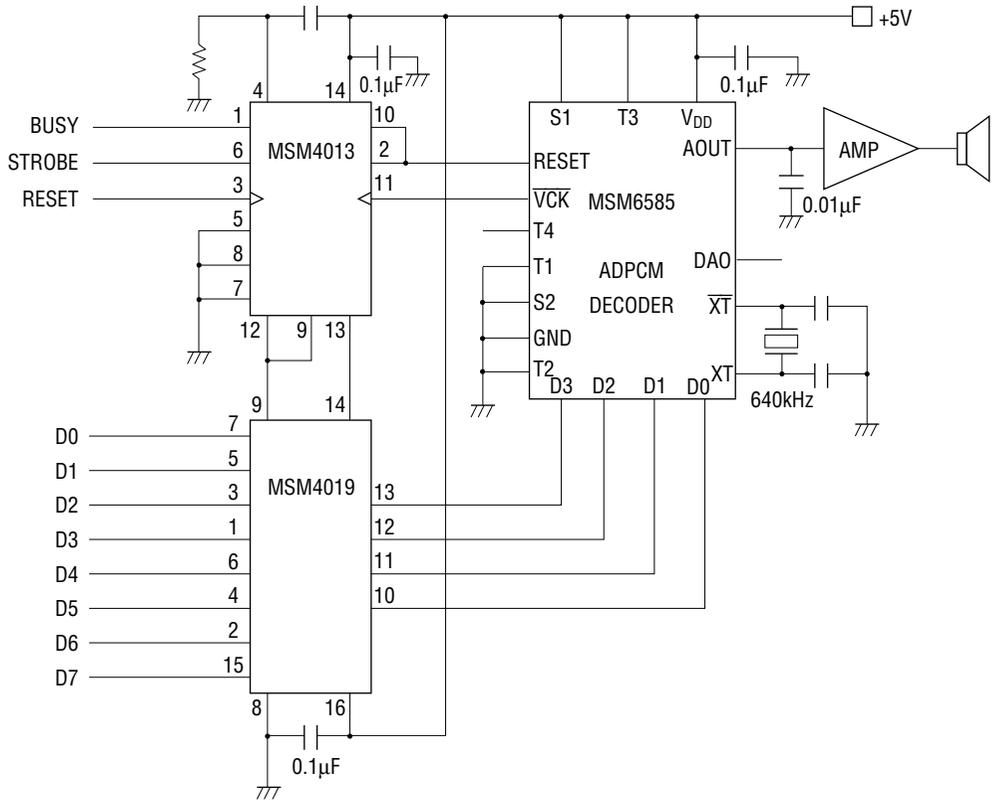


### Centronics Timing Chart
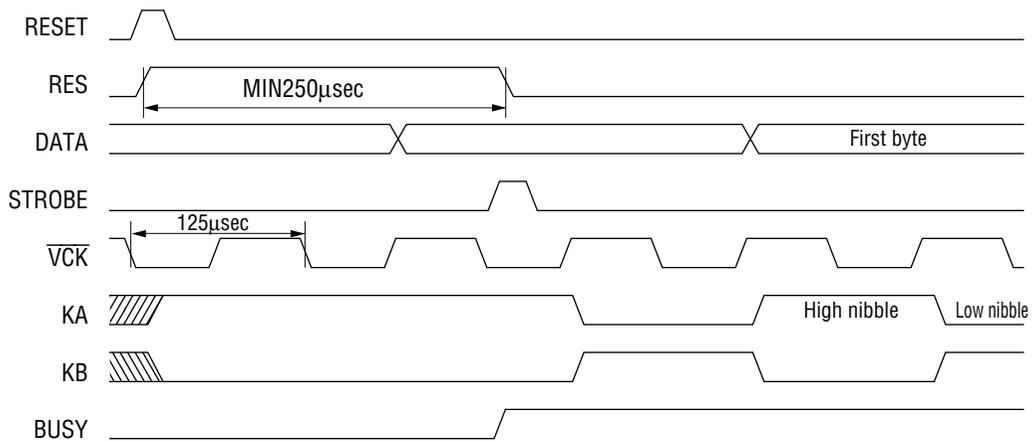
## Example of Interface Circuit with 256K-bit EPROM

The circuit example and timing diagram that used the 256K-bit EPROM are shown below.
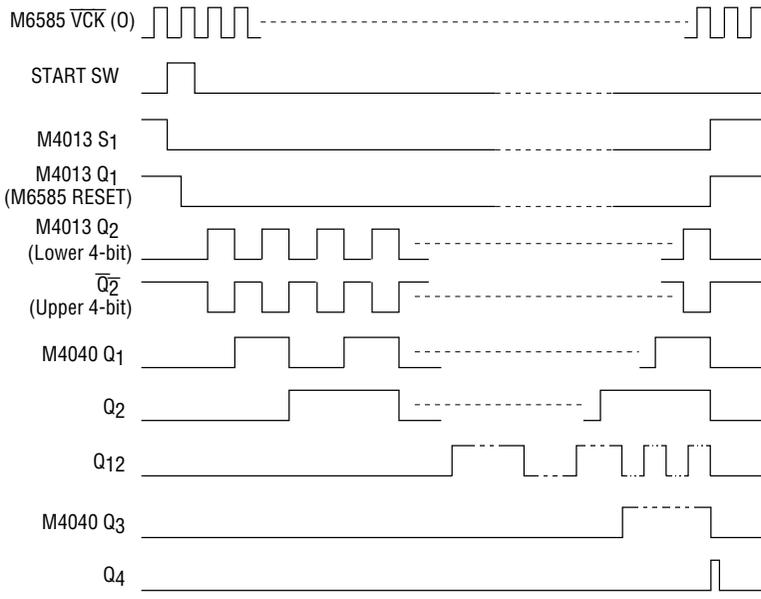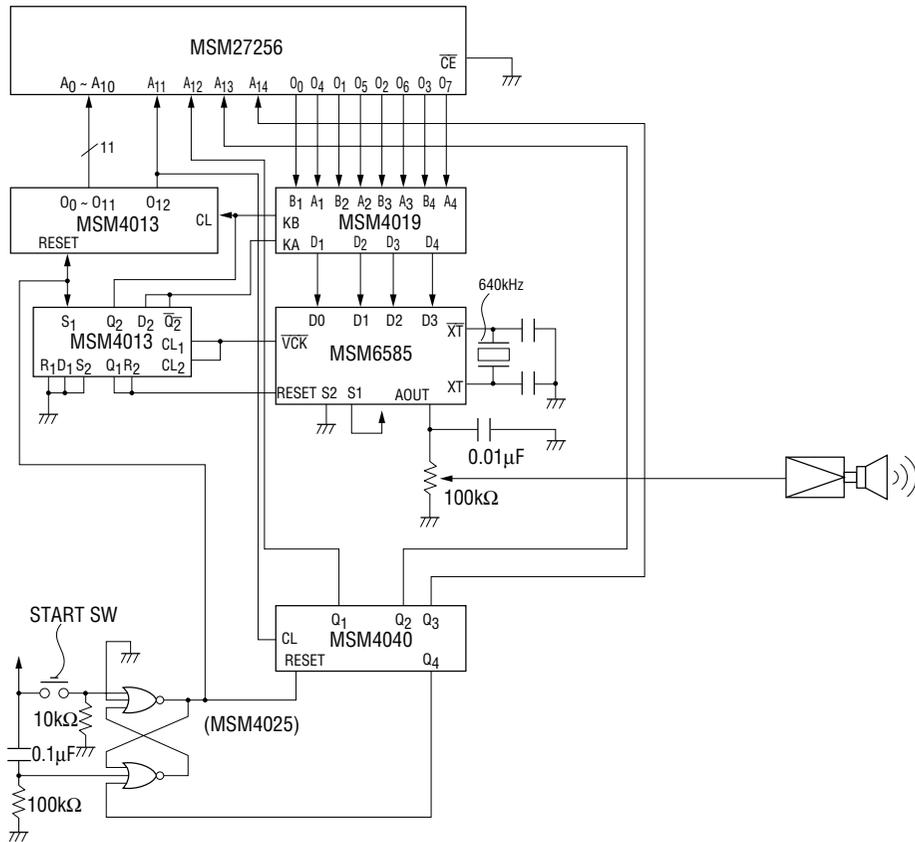
## PAD CONFIGURATION

### Pad Layout

| | |
|---|---|
| Product name | MSM6585 |
| Function | ADPCM voice synthesis IC |
| Die size | $\times$ = 2.92 mm, Y = 3.58 mm |
| Die thickness | 350 µm ±30 µm |
| Pad size | 130 µm × 130 µm |
| Substrate voltage | GND |
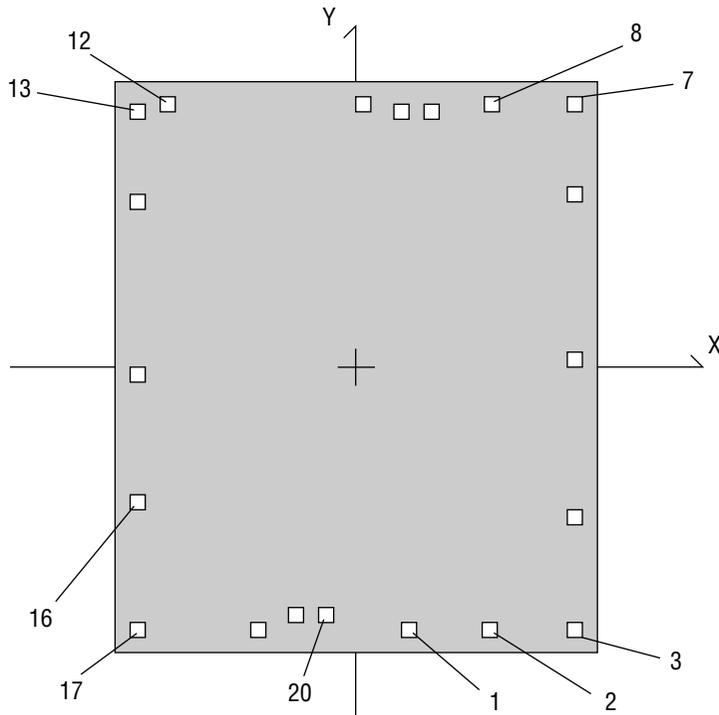


### Pad Coordiantes
(The die center is located at X=0, Y=0)

(Unit: µm)

| PAD No. | PAD Name | X-axis | Y-axis | PAD No. | PAD Name | X-axis | Y-axis |
|---|---|---|---|---|---|---|---|
| 1 | S1 | 377 | −1635 | 11 | AOUT | 38 | 1635 |
| 2 | S2 | 819 | −1635 | 12 | DAO | −1125 | 1635 |
| 3 | T3 | 1305 | −1635 | 13 | T1 | −1305 | 1579 |
| 4 | D0 | 1305 | −943 | 14 | T2 | −1305 | 1009 |
| 5 | D1 | 1305 | 44 | 15 | $\overline{VCK}$ | −1305 | −88 |
| 6 | D2 | 1305 | 1095 | 16 | RESET | −1305 | −818 |
| 7 | D3 | 1305 | 1635 | 17 | XT | −1281 | −1635 |
| 8 | T4 | 830 | 1635 | 18 | $\overline{XT}$ | −529 | −1635 |
| 9 | AV$_{SS}$ | 447 | 1580 | 19 | V$_{DD}$ | −299 | −1549 |
| 10 | V$_{SS}$ | 267 | 1580 | 20 | AV$_{DD}$ | −119 | −1549 |

## PACKAGE DIMENSIONS

(Unit : mm)
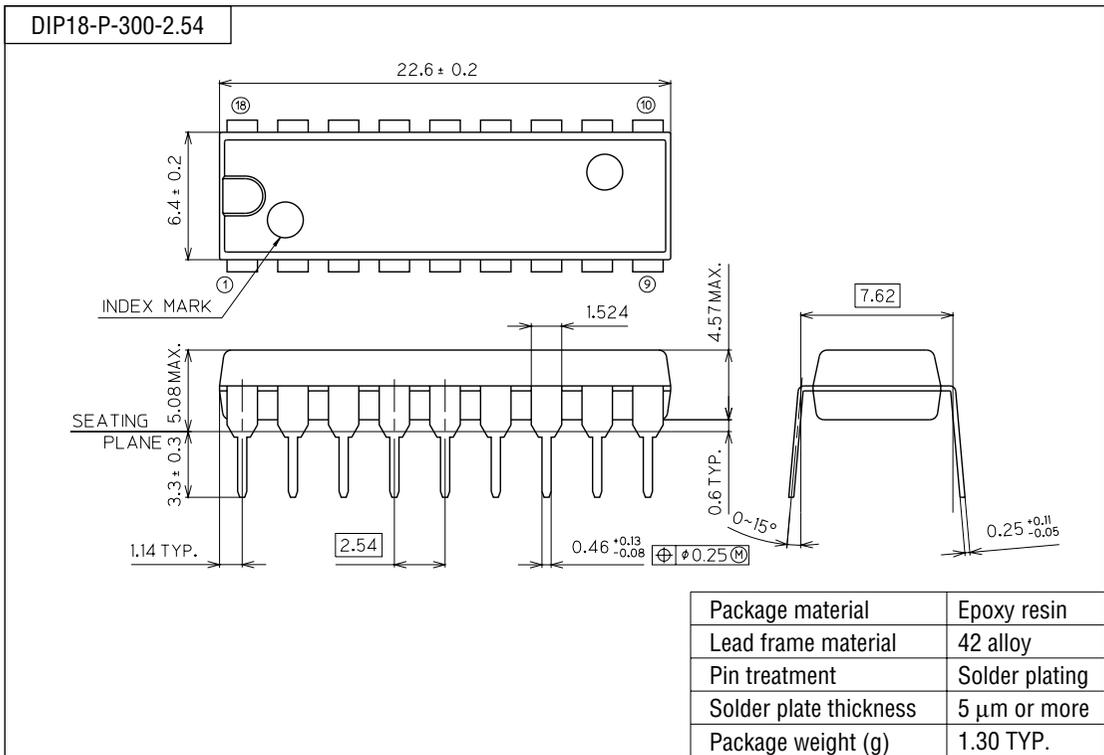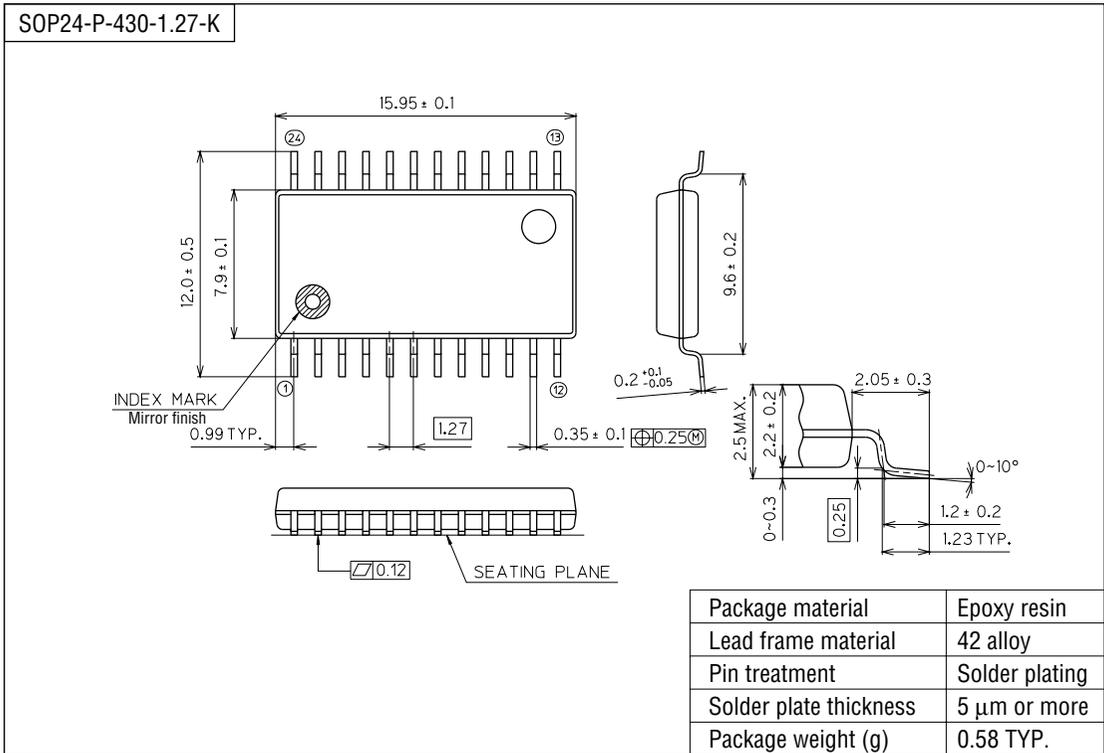
DIP18-P-300-2.54

22.6 ± 0.2

6.4 ± 0.2

INDEX MARK

1.524

4.57 MAX.

5.08 MAX.

SEATING
PLANE

3.3 ± 0.3

0.6 TYP.

7.62

1.14 TYP.

2.54

$0.46^{+0.13}_{-0.08}$

$\oplus$ $\phi$ 0.25 Ⓜ

0~15°

$0.25^{+0.11}_{-0.05}$

| Package material | Epoxy resin |
|---|---|
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.30 TYP. |

(Unit : mm)

SOP24-P-430-1.27-K



| Package material | Epoxy resin |
|---|---|
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 0.58 TYP. |

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SSOP30-P-56-0.65-K



| Package material | Epoxy resin |
|---|---|
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 0.19 TYP. |

Notes for Mounting the Surface Mount Type Package

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