MBM27C256A-20-W
MBM27C256A-25-W

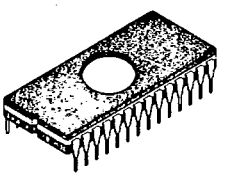
CMOS 32,768 x 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

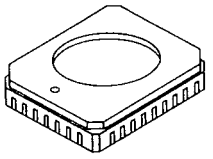
The Fujitsu MBM27C256A-W is a high speed 262,144-bits UV erasable and electrically reprogrammable read only memory (EPROM) with CMOS technology. It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM27C256A-W. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C256A-W is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01



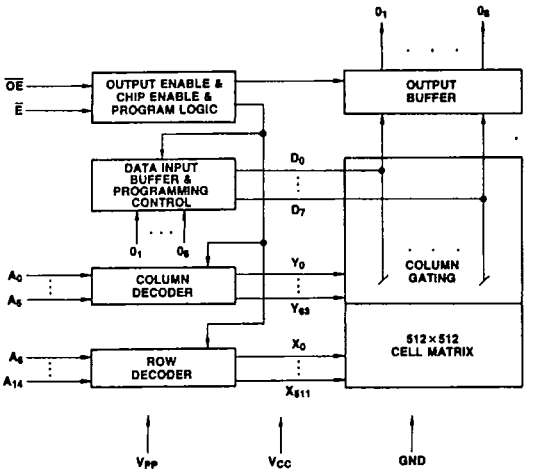
Leadless Chip Carrier LCC-32C-A01

Features

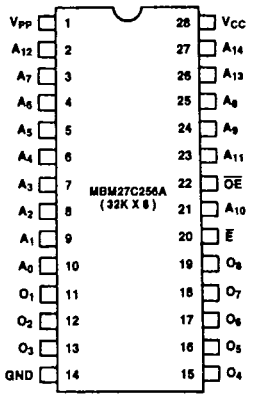
- Wide temperature range: −55°C to +125°C
- CMOS Power Consumption: 550 μW max. (Standby) 41 mW/MHz (Active)
- 32,768 words by 8-bits organization, fully decoded
- Simple programming requirements
- Single location programming
- High speed programming algorithm (typically two 1 ms pulses)
- No clock required (fully static operation)
- Programming voltage: 12.5V
- Single +5V supply, ±10%
- TTL compatible inputs and outputs
- 3-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Fast access time: MBM27C256A-20-W 200 ns max. MBM27C256A-25-W 250 ns max.
- Single +5V operation
- Standard 28-pin DIP package/32-pad LCC

MBM27C256A-20-W
MBM27C256A-25-W

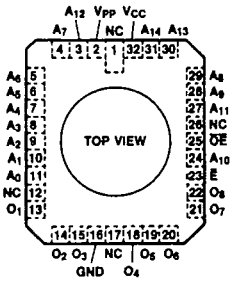
MBM27C256A Block Diagram and Pin Assignments



C256-3



C256-4



C256-5

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Temperature under bias	T_{BIAS}	−65 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C
Inputs/outputs with respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} with respect to GND	V_{PP}	−0.6 to +14	V
V_{CC} with respect to GND	V_{CC}	−0.6 to +7	V

Note:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM27C256A-20-W
MBM27C256A-25-W

Functions and Pin Connections

Mode (Function / Pin No.)	Address Input (2~10, 21, 23~27)	A_9 (24)	Data I/O (11~13, 15~19)	$\overline{E}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	OUT	V_{IL}	V_{IL}	+5V	+5V	GND
Output disable	A_{IN}	A_{IN}	High Z	V_{IL}	V_{IH}	+5V	+5V	GND
Stand by	Don't care	Don't care	High Z	V_{IH}	Don't care	+5V	+5V	GND
Program	A_{IN}	A_{IN}	IN	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program verify	A_{IN}	A_{IN}	OUT	V_{IL}	V_{IL}	+6V	+12.5V	GND
Program inhibit	Don't care	Don't care	High Z	V_{IH}	Don't care	+6V	+12.5V	GND
Electronic signature	A_{IN}	+12V	Code	V_{IL}	V_{IL}	+5V	+5V	GND

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} supply voltage (1)	V_{CC}	4.5	5.0	5.5	V	−55°C to +125°C
V_{PP} supply voltage	V_{PP}	$V_{CC}-0.6$		$V_{CC}+0.6$	V	
Input high voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input low voltage	V_{IL}	−0.1		0.8	V	

Note:
1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input load current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} supply current	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = $V_{CC}-0.3$V to $V_{CC}+0.3$V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output high voltage (I_{OH} = −100 μA)	V_{OH2}	$V_{CC}-0.7$			V

MBM27C256A-20-W
MBM27C256A-25-W

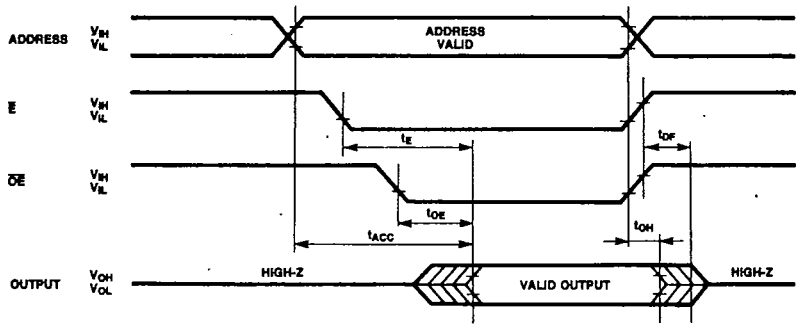
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256A-20 Min	MBM27C256A-20 Max	MBM27C256A-25 Min	MBM27C256A-25 Max	Unit
Address access time (1) ($\overline{E}$ = $\overline{OE}$ = V_{IL})	t_{ACC}		200		250	ns
$\overline{E}$ to output valid ($\overline{OE}$ = V_{IL})	t_E		200		250	ns
$\overline{OE}$ to output valid ($\overline{E}$ = V_{IL}) (1)	t_{OE}		75		100	ns
$\overline{OE}$, $\overline{E}$ high to output float (2, 3)	t_{DF}	0	60	0	60	ns
Address to output hold (3)	t_{OH}	0		0		ns

Notes:
1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the following edge of $\overline{E}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$, $\overline{E}$, whichever occurs first. Output float is defined as the point where data is no longer driven.
3. Sampling, not 100% tested.

Operation Timing Diagram

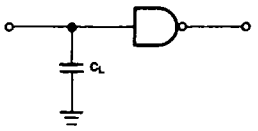


C256-6

AC Test Conditions

(Including programming)

Input Pulse Levels: .....0.45V to 2.4V
Input Rise and Fall Time: .....≤20 ns
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
Output Load: .....1 TTL gate and C_L = 100 pF



C256-7

Programming/Erasing Information

Memory Cell Description

The MBM27C256A-W is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate as shown in Memory Cell diagram. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold as shown in Memory Cell Threshold Shift diagram. In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line as shown in Memory Cell Threshold Shift diagram.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256A-W has all 262,144-bits in the "1", or high, state. "0's" are loaded into the MBM27C256A-W through the procedure of programming.

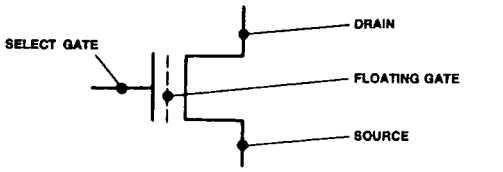
The MBM27C256A-W is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{E}$ and $\overline{OE}$ are at V_{IH}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. The 8-bit pattern is placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of single TTL low-level pulses are applied to the $\overline{E}$ pin followed by an additional pulse to the $\overline{E}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (start address = G).
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If the programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails.
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify all the data. If the programmed data is not the same as the input data, the part failed. If it is the same, the program is completed.

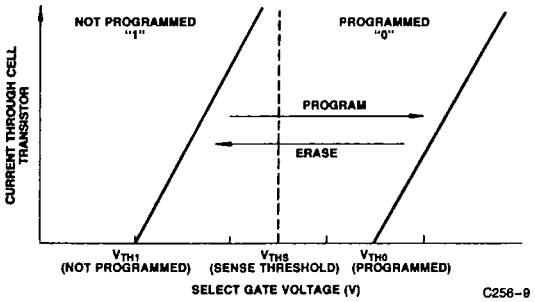
A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

Memory Cell



C256-8

Memory Cell Threshold Shift



C256-9

Quick Pro™ is a trademark of Fujitsu Limited.

Programming/Erasing Information (Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256A-W to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C256A-W. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000 μW/cm^2) for 15 to 20 minutes. The MBM27C256A-W should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C256A-W and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256A-W and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

AC Characteristics

(T_A = 25°C ± 5°C,
V_{CC} = 6V ± 0.25V,
V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
Chip enable setup time	t_{CES}	2			μs
Output enable setup time	t_{OES}	2			μs
Data setup time	t_{DS}	2			μs
V_{PP} setup time	t_{VS}	2			μs
Address hold time	t_{AH}	2			μs
Output enable hold time (1)	t_{OEH}	2			μs
Data hold time	t_{DH}	2			μs
Output enable recovery time (1)	t_{OR}	2			μs
Chip enable to data valid	t_{DV}			1	μs
Output disable to output float delay	t_{DF}			105	ns
Programming pulse width	t_{PW}	0.95	1	1.05	ms
Additional programming pulse width	t_{APW}	2.85		78.75	ms
Programming pulse number	X	1		25	times

Note:
1. $t_{OEH} + t_{OR} \geq 50$ μs.

Electronic Signature

The MBM27C256A-W has electronic signature mode which is intended to be used with programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM27C256A-W. Two identifier bytes are read out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 and A_{13} must be held at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	1	1	0	Device

Notes:
A_9 = 12V ± 0.5V.
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = Either V_{IL} or V_{IH}.

Programming/Erasing Information (Continued)

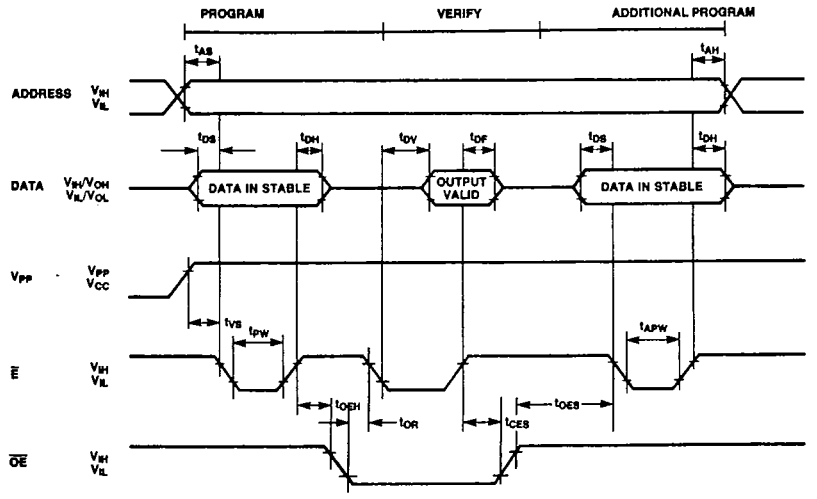
DC Characteristics
(T_A = 25°C ± 5°C,
V_{CC} = 6V ± 0.25V,
V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} supply current during programming pulse ($\overline{E}$ = V_{IL})	I_{PP}			40	mA
V_{CC} supply current	I_{CC}			30	mA
Input low level	V_{IL}	−0.1		0.8	V
Input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage during verify (I_{OH} = −400 μA)	V_{OH}	2.4			V

Notes:
V_{CC} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.

V_{PP} must not be greater than 21.5V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 21V. Also, during $\overline{E}$ = V_{IL}, V_{PP} must not be switched from 5V to 21V or vice-versa.

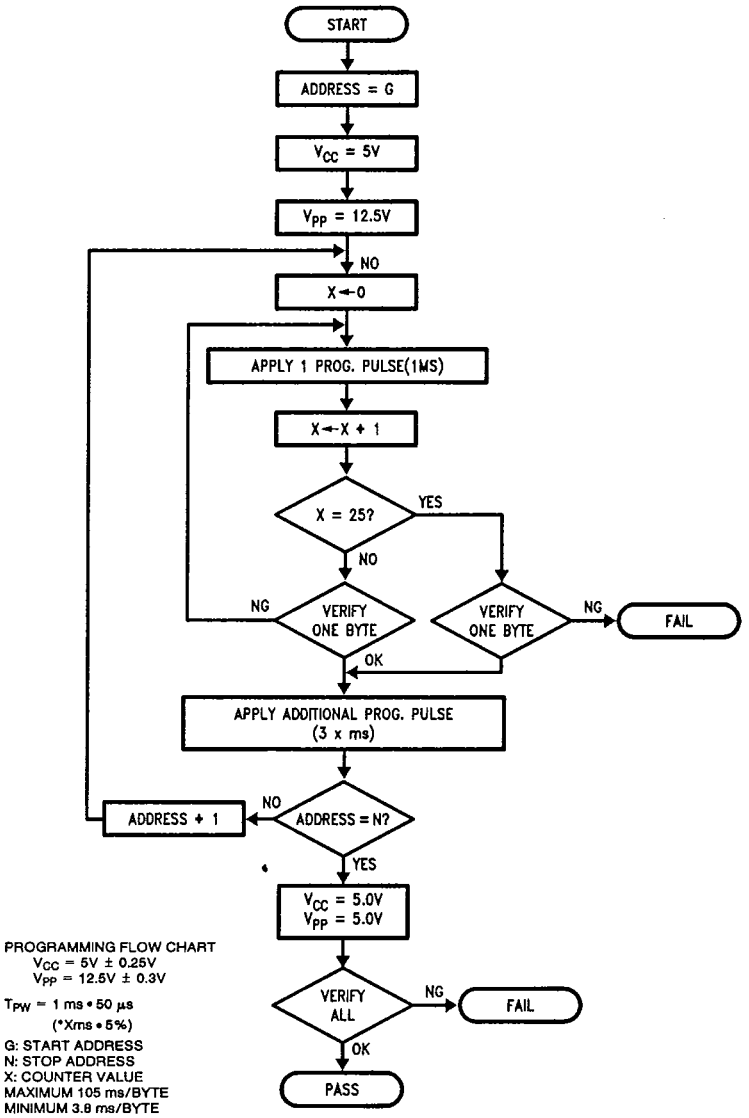
Programming Waveform



C256-10

Programming/Erasing Information (Continued)

Quick Program Flow Chart



PROGRAMMING FLOW CHART
V_{CC} = 5V ± 0.25V
V_{PP} = 12.5V ± 0.3V

T_{PW} = 1 ms • 50 µs
(*Xms • 5%)

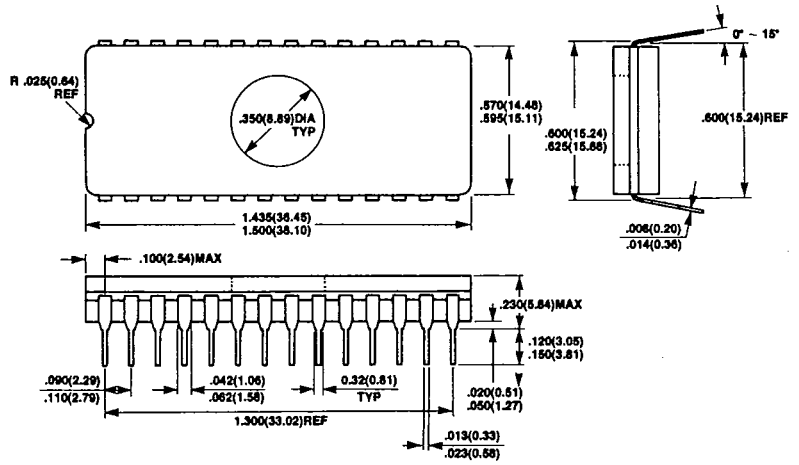
G: START ADDRESS
N: STOP ADDRESS
X: COUNTER VALUE
MAXIMUM 105 ms/BYTE
MINIMUM 3.8 ms/BYTE

C256-11

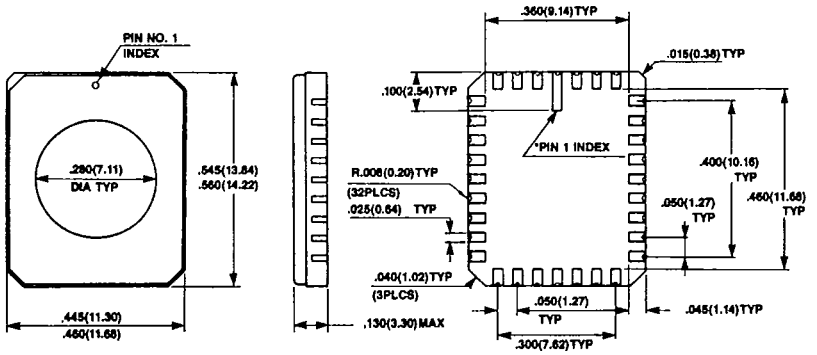
MBM27C256A-20-W
MBM27C256A-25-W

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid)
Dual In-Line Package
(Case No.: DIP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE.