

TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

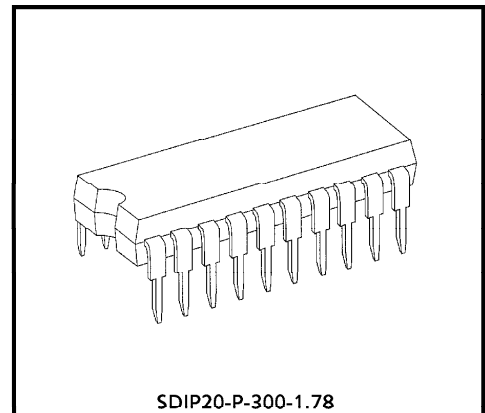
TA1226N

Y LUMINANCE TRANSIENT IMPROVER IC

TA1226N integrates Y luminance transient improver circuits (black stretch, DC transfer ratio compensation, super real transient, noise reduction) in a 20-pin shrink DIP. TA1226N functions are controlled via I²C bus.

FEATURES

- Black stretch circuit
- DC transfer ratio compensation circuit
- Super real transient circuit (SRT)
- Noise reduction
- 1-bit DAC output
- Velocity modulation output

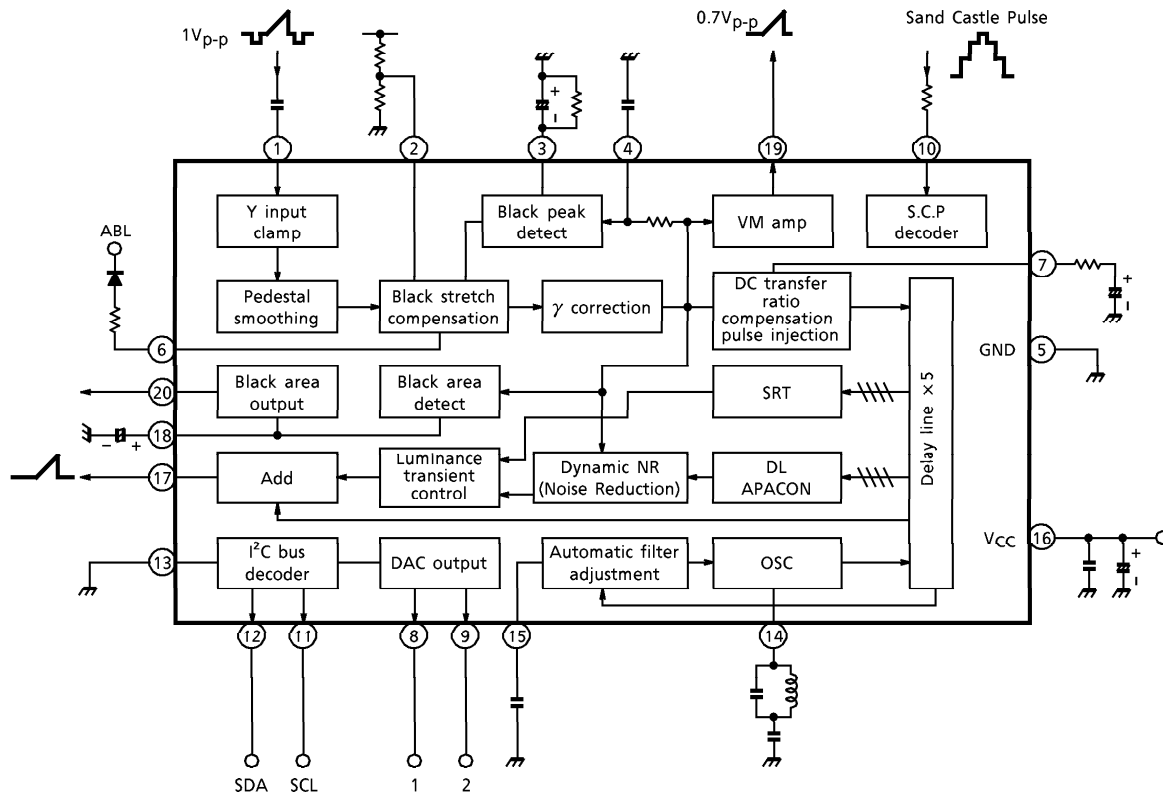


Weight : 1.02g (Typ.)

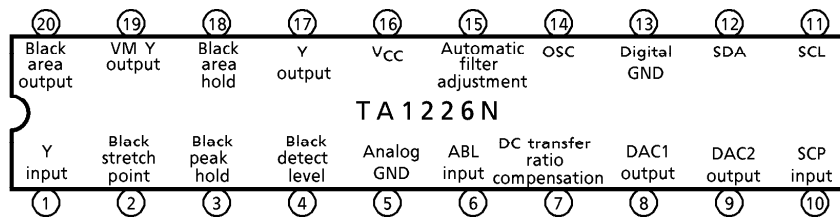
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BLOCK DIAGRAM

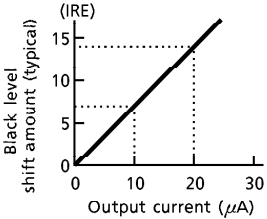
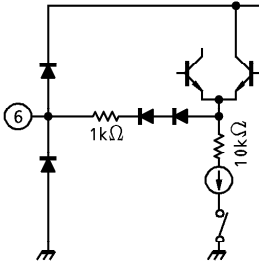
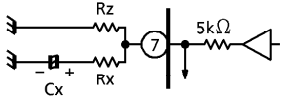
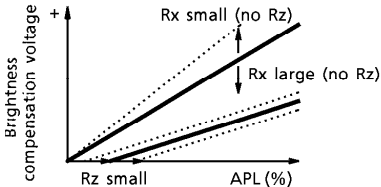
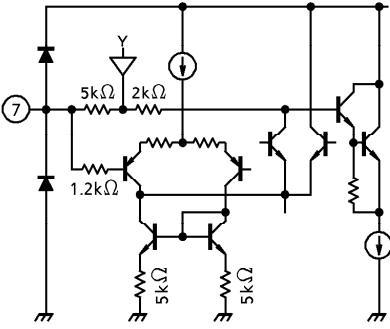
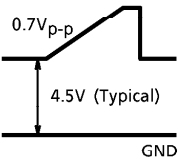
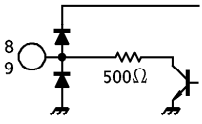
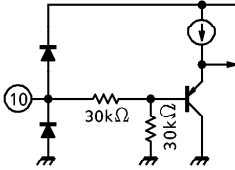
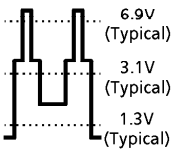


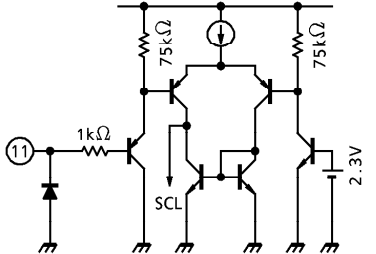
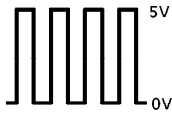
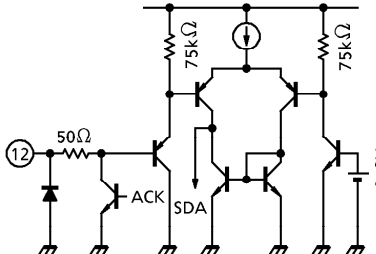
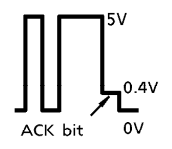
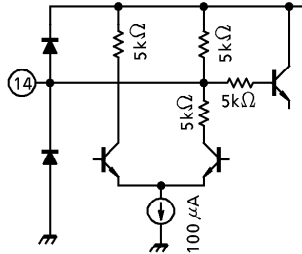

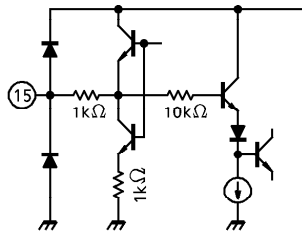
TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

| Pin No. | PIN NAME | FUNCTION | INTERFACE | I / O SIGNAL |
|---------|---------------------|--|-----------|------------------------|
| 1 | Y input | Luminance signal input pin. Input luminance signal after eliminating chrome signal via capacitor. After luminance signal is input to this pin, Y signal is clamped to 4.5V pedestal level. Standard input level is 1V _{p-p} (including sync signal). | | |
| 2 | Black stretch point | Used to set black stretch start point using external resistance (DC level). Note that setting this pin to 1.5V or below enters test mode. | | <p>DC 3.5~7.0V</p> |
| 3 | Black peak hold | Used to connect filter which detects highest black level of luminance signal. Voltage on this pin determines black stretch gain. | | <p>DC 3.8~5.2V</p> |
| 4 | Black detect level | Used to control frequency (area) of black level to be detected. Set area to be detected using external capacitance and internal resistance. In application circuit example, setting is made so that frequency of black level to be detected is 100kHz or less. | | |

| PIN No. | PIN NAME | FUNCTION | INTERFACE | I/O SIGNAL |
|---------|--------------------------------|---|--|---|
| 5 | Analog GND | GND for analog circuit | — | — |
| 6 | ABL input | Used to apply control current for ABL and black level compensation.  |  | — |
| 7 | DC transfer ratio compensation | Used to compensate DC transfer ratio. Smaller Rx, larger compensation amount. Injection of Rz varies start point of DC transfer ratio compensation. $\text{DC transfer ratio TDC (\%)} = 5k\Omega / (5k\Omega + R_x) \times 30 + 100$   |  | When pin 7 is open :  |
| 8 9 | DAC1 output DAC2 output | Open collector switches. Maximum, input current value : 2mA (minimum, drive resistance value : 6kΩ) |  | DC VCC or GND |
| 10 | SCP input | SCP (Sand Castle Pulse) input pin. Typical thresholds for CP (Clamp Pulse), HP (Horizontal Pulse), and VP (Vertical Pulse) are 6.9V, 3.1V, and 1.3V respectively. |  |  |

| PIN No. | PIN NAME | FUNCTION | INTERFACE | I/O SIGNAL |
|---------|-----------------------------|---|--|---|
| 11 | SCL | I ² C bus SCL pin. Because surge breakdown voltage is low, take external countermeasure if necessary. |  |  |
| 12 | SDA | I ² C bus SDA pin. Because surge breakdown voltage is low, take external countermeasure if necessary. When Vcc voltage is 3.2V or more, power-on reset is applied. |  |  |
| 13 | Digital GND | Logic circuit GND pin. | — | — |
| 14 | OSC | Used to connect filter for obtaining 4MHz. Using 4-MHz oscillation, automatically adjusts built-in delay line. |  | <p>DC 11.7V (Typical)</p> <p>AC 420mV_{p-p} (Typical) (at 4MHz)</p>  |
| 15 | Automatic filter adjustment | Used to connect filter which automatically adjusts delay time of IC built-in delay line. Directly connecting external pull-up resistor increases peak frequency. Pulling down decreases peak frequency. |  | <p>DC 5.9V (Typical)</p> |

| PIN No. | PIN NAMA | FUNCTION | INTERFACE | I/O SIGNAL |
|---------|-------------------|---|-----------|----------------|
| 16 | V _{CC} | V _{CC} pin. Connect 12V (typical). | — | — |
| 17 | Y output | Output pin for luminance signal on which Y is processed. Max. output current value : 2mA (min. drive resistance value : 3.8kΩ) | | |
| 18 | Black area hold | Used to connect filter which detects black area of input luminance signal. Voltage changes depending on black area of input signal pin. Black area detection of bus control can vary threshold of black area detect. | | DC 0.2~6.7V |
| 19 | Y output for VM | Y output pin for VM (Velocity Modulation). Maximum output current value : 2mA (minimum drive resistance : 2.4kΩ). | | |
| 20 | Black area output | Output pin for black area detected by black area hold circuit. Outputs DC current depending on input black area. Larger black area, higher pin voltage. Control is possible using output of this pin, depending on input signal black area. | | DC 0.5~6.8V |

BUS CONTROL MAP

Y luminance transient improver IC

Slave address : 10111010 (BA (h))

| SUB ADDRESS | 7 MSB | 6 | 5 | 4 | 3 | 2 | 1 | 0 LSD | POWER-ON INITIAL VALUE | |
|-------------|-------------------|-----------|---|---------------|------------------------------------|---------------------|-----|-------|------------------------|------|
| | | | | | | | | | MSB | LSD |
| 00 | APAC | Sharpness | | | | | | | 0100 | 0000 |
| 01 | Black area detect | SRT level | | * | YNR | γ correction | | | 0000 | 1011 |
| 02 | DAC1 | DAC2 | VM gain | Black stretch | γ curve | Black compensa-tion | SRT | | 0011 | 0011 |
| 03 | TEST | | Frequency characteristics compensation (RS) | | Luminance transient tracking (RTC) | | | | 1100 | 0100 |

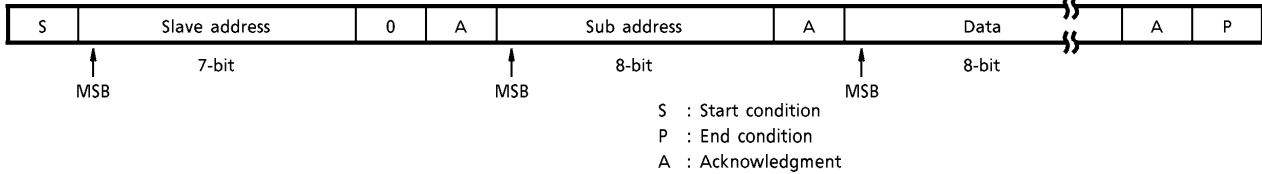
(Note) * : Ignore data.

| FUNCTION | CONTROL DATA | CONTROL CONTENTS | PRESET VALUE |
|---|--|---|-----------------------|
| APACON | 0 : ON 1 : OFF | Controls ON/OFF of DL (Delay Line) APACON in micro signal amplitude (approx. 20mV _{p-p}) range. | ON (0) |
| Sharpness | 7F : MAX 00 : MIN | Controls both DL APACON and SRT. | Center value (40h) |
| Black area detect | 11 : 40 IRE 10 : 30 IRE 01 : 20 IRE 00 : 10 IRE | Controls maximum level of black area detect from pedestal of black area detector circuit (pin 20 output). | 10 IRE (00) |
| SRT level | 11 : 28 IRE 10 : 14 IRE 01 : 10 IRE 00 : 7 IRE | Controls signal amplitude at which SRT becomes valid. | 28 IRE (00) |
| YNR | 0 : ON 1 : OFF | Controls YNR ON/OFF. | OFF (1) |
| γ correction | 11 : OFF 10 : 90 IRE 01 : 80 IRE 00 : 70 IRE | Controls start point of γ correction (broken line at one point) | OFF (11) |
| DAC1 | 0 : OPEN 1 : ON | Controls 1-bit DAC (open collector transistor output) | OPEN (0) |
| DAC2 | 0 : OPEN 1 : ON | Controls 1-bit DAC (open collector transistor output) | OPEN (0) |
| VM gain | 11 : 0dB 10 : -3dB 01 : -6dB 00 : OFF | Controls gain between Y input and VM output. | 0dB (00) |
| Black stretch | 0 : ON 1 : OFF | Controls black stretch ON/OFF. | OFF (0) |
| γ curve | 0 : -2.4dB 1 : -1.6dB | Controls curve of γ correction (broken line at one point) | -2.4dB (0) |
| Black compensation | 0 : ON 1 : OFF | Controls automatic black level compensation (max. 7.5IRE). (When black stretch gain is maximum, if highest black level floats above pedestal level, DC-shifts maximum of 7.5IRE picture duration up to pedestal level.) | ON (0) |
| SRT | 0 : OFF 1 : ON | Controls SRT ON/OFF. | ON (1) |
| TEST | 11 : Test3 10 : RTC 01 : SHR 00 : RS | Controls pin 20 output signal in test mode. | Test3 (11) |
| 8MHz frequency characteristics compensation | 111 : MAX (+6dB) 000 : MIN (0dB) | Controls gain of DL APACON at 8MHz peak. | 0dB (000) |
| Luminance transient tracking | 111 : MAX 000 : MIN | Controls compensation ratio of SRT and DL APACON. (Controls SRT level to be added to DL APACON.) | Center value (100) |

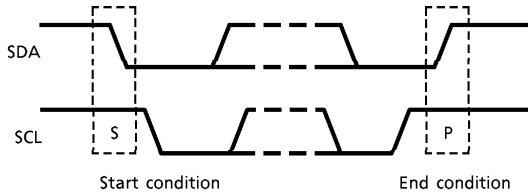
OVERVIEW OF I²C BUS CONTROL FORMAT

The bus control format for TA1226N conforms to the Philips standard.

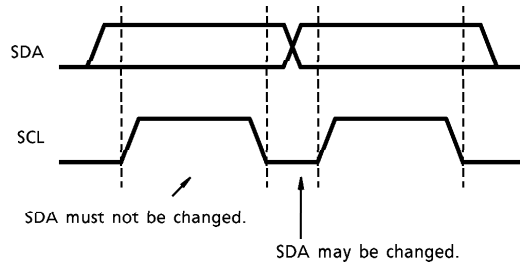
Data transfer format



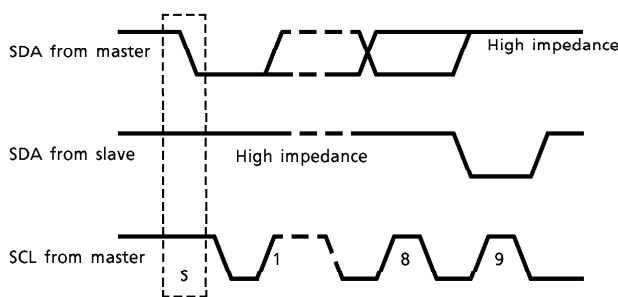
(1) Start and end conditions



(2) Bit transfer



(3) Acknowledgment



(4) Slave addresses

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/ \bar{W} |
|----|----|----|----|----|----|----|--------------|
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | |

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MAXIMUM RATINGS ($T_a = 25 \pm 3^\circ\text{C}$)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|----------------------------------|----------------|----------|------------------------------|
| Supply Voltage | V_{ccmax} | 14 | V |
| Input Pin Signal Voltage | e_{inmax} | 12 | V_{p-p} |
| Power Dissipation | P_D (Note 1) | 1400 | mW |
| Power Dissipation Decrease Ratio | $1 / Q_{jp}$ | - 11.2 | $\text{mW} / ^\circ\text{C}$ |
| Operating Temperature | T_{opr} | - 20~65 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | - 55~150 | $^\circ\text{C}$ |

(Note 1) See figure below.

(Note 2) Since the device is susceptible to surge voltage, take great care when handling.

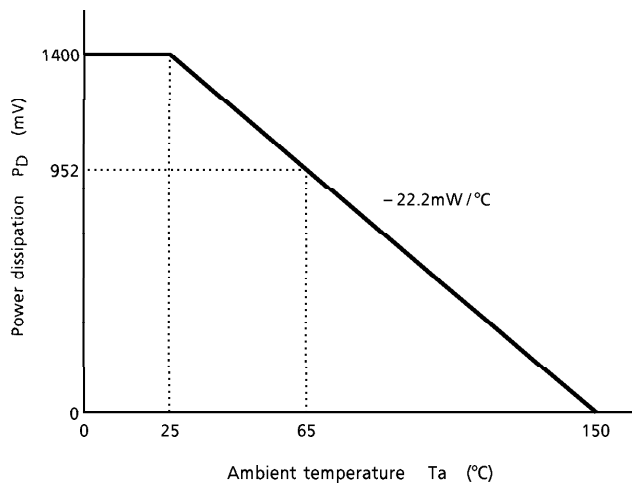


Figure Temperature decrease curve of power dissipation

RECOMMENDED SUPPLY VOLTAGE

| PIN No. | PIN NAME | MIN | TYP | MAX | UNIT |
|---------|-----------------|------|------|------|------|
| 16 | V _{CC} | 11.0 | 12.0 | 13.0 | V |

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 12V, Ta = 25 ± 3°C)

DC characteristics

Supply voltage

| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNIT |
|----------------|-----------------|------|------|------|------|
| Supply Voltage | I _{CC} | 26.0 | 35.5 | 48.0 | mA |

Pin voltage

| PIN No. | PIN NAME | SYMBOL | MIN | TYP | MAX | UNIT | REMARKS |
|---------|--------------------------------|--------|------|------|------|------|-------------------------------|
| 1 | Y input | V1 | 4.20 | 4.50 | 4.80 | V | No input, SCP input |
| 4 | Black detect level | V4 | 4.20 | 4.50 | 4.80 | | |
| 6 | ABL input | V6 | 2.00 | 2.50 | 2.90 | | |
| 7 | DC transfer ratio compensation | V7 | 4.20 | 4.50 | 4.80 | | No input, Pin open, SCP input |
| 8 | DAC1 output | V8 | 11.5 | 11.9 | 12.0 | | No input, SCP input |
| 9 | DAC2 output | V9 | 11.5 | 11.9 | 12.0 | | |
| 17 | Y output | V17 | 7.45 | 7.80 | 8.15 | | |
| 19 | VM Y output | V19 | 3.30 | 3.75 | 4.20 | | |

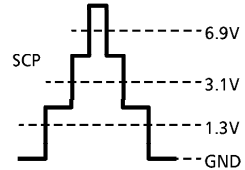
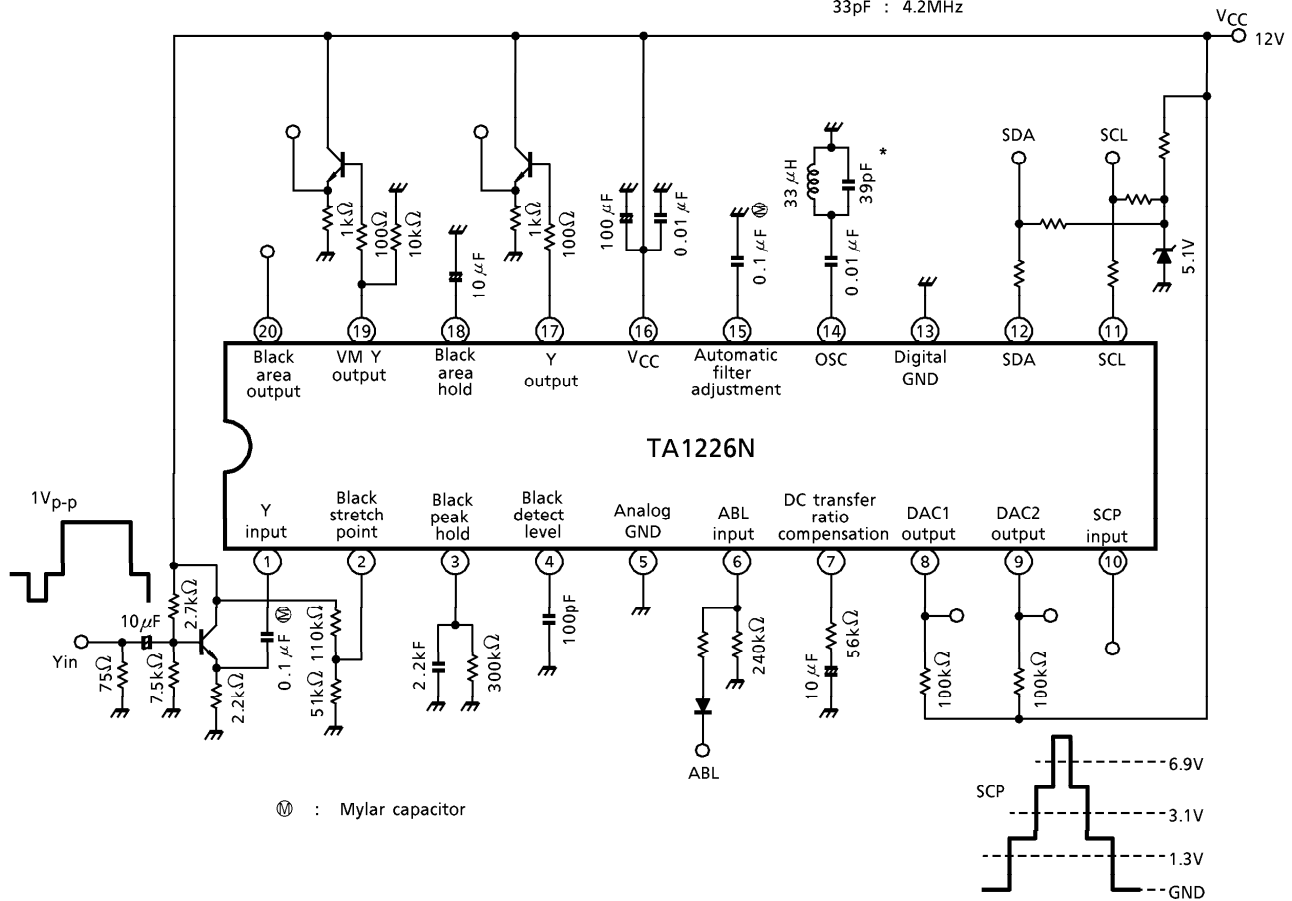
AC characteristics (Unless otherwise specified, V_{CC} = 12V, Ta = 25 ± 3°C)

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--|--------------------|---------------|----------------|------|------|------|---------|
| Y Input Pedestal Clamp Voltage | V1 | — | (Note 1) | 4.2 | 4.5 | 4.8 | V |
| Pin 7 Output Impedance | Z _{OUT7} | — | (Note 2) | 4.3 | 5.5 | 6.7 | kΩ |
| DC Transfer Ratio Compensation Amp Gain | A _{V7} | — | (Note 3) | 0.25 | 0.34 | 0.45 | — |
| Dynamic ABL Maximum Sensitivity | G _{V6} | — | (Note 4) | 3.4 | 5 | 6.6 | mV / μA |
| Black Stretch Amp Maximum Gain | G _{VBE} | — | (Note 5) | 1.30 | 1.40 | 1.50 | — |
| Y Input Dynamic Range | DR ₁ | — | (Note 6) | 0.9 | 1.0 | 1.2 | V |
| Luminance Transient Control Peaking Frequency | F _p | — | (Note 7) | 3.6 | 4 | 4.4 | MHz |
| Luminance Transient Control Range | G _S MAX | — | (Note 8) | 9 | 12 | 15 | dB |
| | G _S MIN | | | -12 | -9 | -6 | |
| Luminance Transient Control Center Characteristics | G _S CT | — | (Note 9) | 4 | 5.5 | 7 | dB |
| Peaking Frequency Change Range | F _P MAX | — | (Note 10) | 4.3 | 5.9 | 7.8 | MHz |
| | F _P MIN | | | 1.8 | 2.7 | 3.6 | |

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|------------------------------------|---------------|----------------|------|------|------|------|
| Super Real Transient 2T Pulse Response | SRT _{MAX} | — | (Note 11) | 20 | 40 | 60 | ns |
| | SRT _{CEN} | | | 110 | 130 | 150 | |
| | SRT _{MIN} | | | 170 | 190 | 210 | |
| Noise Reduce | GNR | — | (Note 12) | -15 | -7 | -1.0 | dB |
| Black Stretch Point | V _{ST1} | — | (Note 13) | 250 | 310 | 370 | mV |
| | V _{ST2} | | | 340 | 430 | 520 | |
| Black Peak Detect On Voltage | V _{BPON} | — | (Note 14) | 1.2 | 1.5 | 1.8 | V |
| Black Detect Delay Time | T _{BP1} | — | (Note 15) | 0 | 50 | 170 | ns |
| | T _{BP2} | | | | | | |
| VM Output Y Gain | G _{VM00} | — | (Note 16) | — | -40 | -20 | dB |
| | G _{VM01} | | | -7 | -6 | -5 | |
| | G _{VM10} | | | -4 | -3 | -2 | |
| | G _{VM11} | | | -1 | 0 | 1 | |
| γ Correction Point | V _{γ00} | — | (Note 17) | 530 | 575 | 620 | mV |
| | V _{γ01} | | | 600 | 645 | 690 | |
| | V _{γ10} | | | 620 | 665 | 710 | |
| γ Correction Curve | G _{γ0} | — | (Note 18) | -3.2 | -2.4 | -1.6 | dB |
| | G _{γ1} | | | -2.4 | -1.6 | -0.8 | |
| Black Peak Detect Level | V _{BP} | — | (Note 19) | 5 | 20 | 35 | mV |
| DL APACON Limiter Range | V _{AL} | — | (Note 20) | 20 | 45 | 70 | mV |
| Black Area Detected Level | V _{BS00} | — | (Note 21) | 50 | 80 | 110 | mV |
| | V _{BS01} | | | 130 | 160 | 190 | |
| | V _{BS10} | | | 200 | 230 | 260 | |
| | V _{BS11} | | | 280 | 310 | 340 | |
| Black Area Hold Pin Voltage | Δ V _{BS00} | — | (Note 22) | -260 | 0 | 260 | mV |
| Black Area Output Pin Voltage Difference | Δ V _{BS01} | | | | | | |
| Black Area Output Pin Voltage Change With Respect To Black Area Hold Pin Voltage Change | Δ V _{BS10} | — | (Note 23) | 410 | 500 | 610 | mV |
| | Δ V _{BS11} | | | | | | |
| | Δ V ₂₀₀₀ | | | | | | |
| | Δ V ₂₀₀₁ | | | | | | |
| Frequency Characteristics Compensation | FT _{MAX} | — | (Note 24) | 5 | 6 | 7 | dB |
| | FT _{MIN} | | | -1.5 | 0 | -1.5 | |
| Clamp Voltage On Voltage | V _{CLON} | — | (Note 25) | 6.7 | 6.9 | 7.1 | V |
| Horizontal Blanking On Voltage | V _{HP} | — | — | 2.9 | 3.1 | 3.3 | V |
| Vertical Blanking On Voltage | V _{VP} | — | — | 1.1 | 1.3 | 1.5 | V |
| OSC Oscillation Frequency | F _{OSC} | — | (Note 26) | 3.9 | 4.0 | 4.1 | MHz |

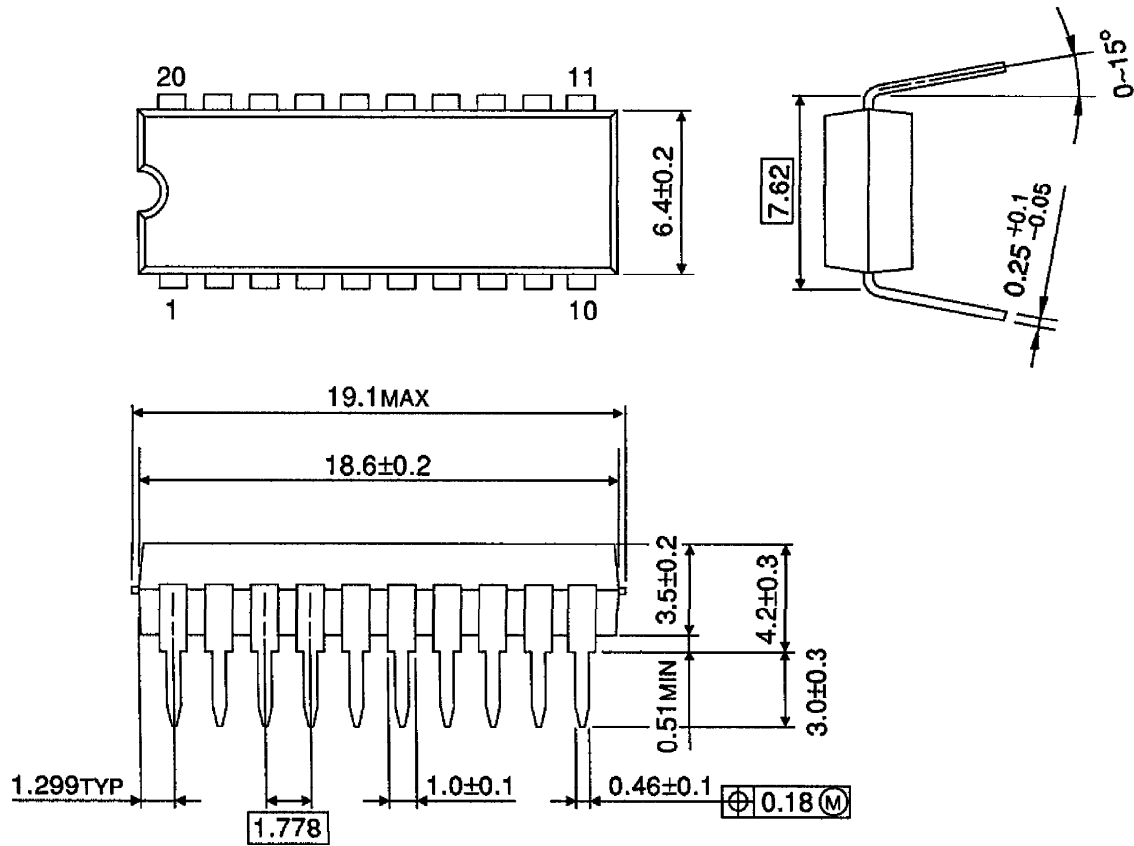
APPLICATION CIRCUIT

Peak Frequency
 * 39pF : 4.0MHz
 33pF : 4.2MHz



OUTLINE DRAWING
SDIP20-P-300-1.78

Unit : mm



Weight : 1.02g (Typ.)