TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX163245FT

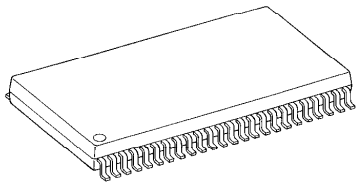
16-BIT DUAL SUPPLY VOLTAGE INTERFACE BUS TRANSCEIVER

The TC74LCX163245 is a dual supply, advanced high speed CMOS 16 bit DUAL SUPPLY VOLTAGE INTERFACE BUS TRANSCEIVER fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 3.3 V bus and a 5 V bus in mixed 3.3 V / 5 V supply systems' it achieves high speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated. The B-port interfaces with the 3 V bus, the A-port with the 5 V bus.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



TSSOP48-P-0061-0.50

Weight : 0.25 g (Typ.)

FEATURES

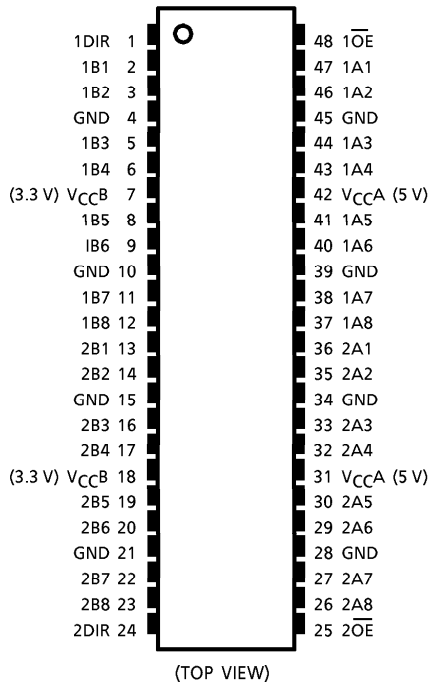
- Bidirectional interface between 3.3 V and 5 V buses
- High speed : t_{pd} = 7.0 ns (max)
  (V_{CCB} = 3.3 ± 0.3 V / V_{CCA} = 5 ± 0.5 V, Ta = −40~85°C)
- Low power dissipation : I_{CC} = 80 μA (max) (Ta = −40~85°C)
- Symmetrical output impedance : I_{OUTA} = ±24 mA (min)
  I_{OUTB} = ±24 mA (min)
  (V_{CCA} = 4.5 V / V_{CCB} = 3.0 V)
- Power Down Protection is provided on all inputs and outputs.
- Package : TSSOP (Thin Shrink Small Outline Package)

APPLICATION NOTES

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

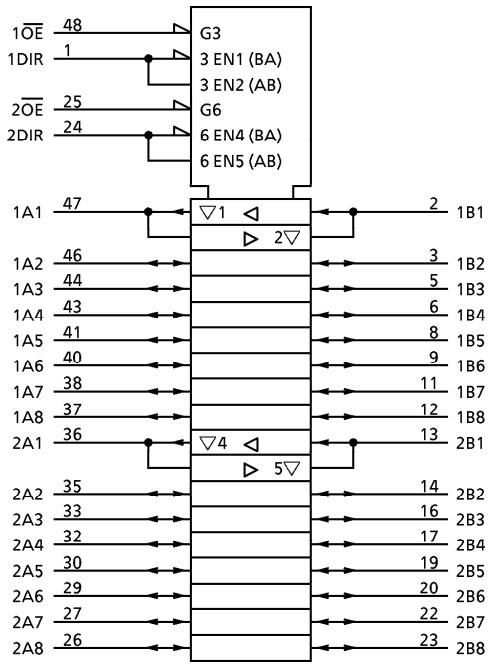
All floating (high impedance) bus terminals must have their input fixed by means of pull up or pull down resistors.

PIN CONNECTION



(TOP VIEW)

IEC LOGIC SYMBOL



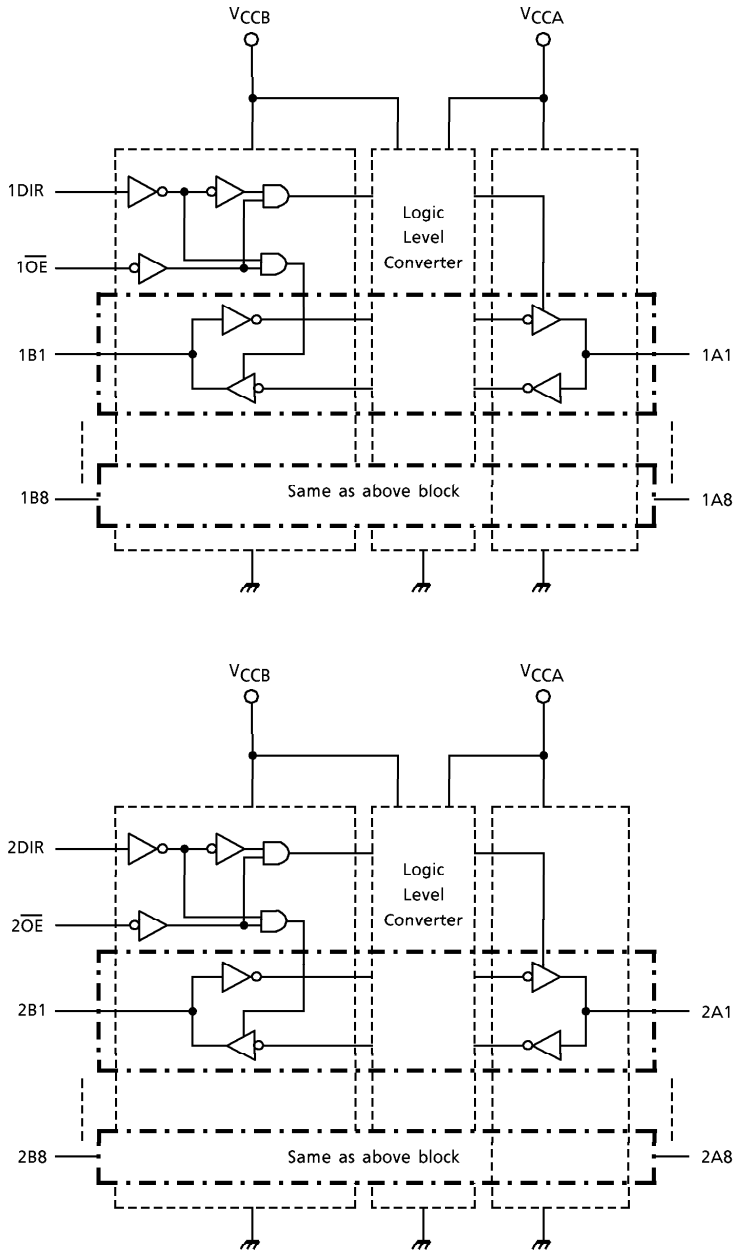
TRUTH TABLE

INPUT		FUNCTION		OUTPUT
$1\overline{OE}$	1DIR	BUS 1A1-1A8	BUS 1B1-1B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

INPUT		FUNCTION		OUTPUT
$2\overline{OE}$	2DIR	BUS 2A1-2A8	BUS 2B1-2B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

X : Don't Care
Z : High impedance

BLOCK DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage (Note 1)	V_{CCB}	−0.5~7.0	V
	V_{CCA}	−0.5~7.0	
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/OB}$	−0.5~7.0 (Note 2)	V
		−0.5~V_{CCB} + 0.5 (Note 3)	
	$V_{I/OA}$	−0.5~7.0 (Note 2)	
		−0.5~V_{CCA} + 0.5 (Note 3)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	$I_{I/OK}$	±50 (Note 4)	mA
DC Output Current	I_{OUTB}	±50	mA
	I_{OUTA}	±50	
DC V_{CC}/Ground Current Per Supply Pin	I_{CCB}	±100	mA
	I_{CCA}	±100	
Power Dissipation	P_D	400	mW
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) : Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.
(Note 2) : Off-State
(Note 3) : High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 4) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CCB}	2.3~3.6	V
	V_{CCA}	4.5~5.5	
Input Voltage (DIR, $\overline{OE}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/OB}$	0~5.5 (Note 5)	V
		−0.5~V_{CCB} + 0.5 (Note 6)	
	$V_{I/OA}$	0~5.5 (Note 5)	
		−0.5~V_{CCA} + 0.5 (Note 6)	
Output Current	I_{OUTB}	±24 (Note 7)	mA
		±8 (Note 8)	
	I_{OUTA}	±24 (Note 9)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~10 (V_{CCB} = 2.3~3.6 V)	ns/V
		0~10 (V_{CCA} = 4.5~5.5 V)	

(Note 5) : Off-State
(Note 6) : High or Low State
(Note 7) : V_{CCB} = 3.0~3.6 V
(Note 8) : V_{CCB} = 2.3~2.7 V
(Note 9) : V_{CCA} = 4.5~5.5 V

ELECTRICAL CHARACTERISTICS

DC Characteristics

PARAMETER	SYM-BOL	TEST CONDITION		V_{CCB} (V)	V_{CCA} (V)	Ta = −40~85°C MIN	Ta = −40~85°C MAX	UNIT
"H" Level Input Voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	5.0 ± 0.5	1.7	—	V
				3.3 ± 0.3	5.0 ± 0.5	2.0	—	
	V_{IHA}	An		2.3~3.6	5.0 ± 0.5	2.0	—	
"L" Level Input Voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	5.0 ± 0.5	—	0.7	V
				3.3 ± 0.3	5.0 ± 0.5	—	0.8	
	V_{ILA}	An		2.3~3.6	5.0 ± 0.5	—	0.8	
"H" Level Output Voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OHB} = −100 μA	2.3~3.6	5.0 ± 0.5	V_{CCB} − 0.2	—	V
			I_{OHB} = −24 mA	3.0	5.0 ± 0.5	2.2	—	
			I_{OHB} = −8 mA	2.3	5.0 ± 0.5	1.8	—	
	V_{OHA}		I_{OHA} = −100 μA	2.3~3.6	5.0 ± 0.5	V_{CCA} − 0.2	—	
			I_{OHA} = −24 mA	2.3~3.6	4.5	3.8	—	
"L" Level Output Voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OHB} = 100 μA	2.3~3.6	5.0 ± 0.5	—	0.2	V
			I_{OHB} = 24 mA	3.0	5.0 ± 0.5	—	0.55	
			I_{OHB} = 8 mA	2.3	5.0 ± 0.5	—	0.6	
	V_{OHA}		I_{OHA} = 100 μA	2.3~3.6	5.0 ± 0.5	—	0.2	
			I_{OHA} = 24 mA	2.3~3.6	4.5	—	0.44	
3-State Output Off-State Current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} $V_{I/OB}$ = V_{CCB} or GND		2.3~3.6	5.0 ± 0.5	—	±5.0	μA
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} $V_{I/OA}$ = V_{CCA} or GND		2.3~3.6	5.0 ± 0.5	—	±5.0	
Input Leakage Current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = V_{CCB} or GND		3.6	5.5	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{INA}, V_{INB} = 0~5.5		0	0	—	10	μA
Quiescent Supply Current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.6	5.5	—	50 50	μA
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.6	5.5	—	80	
	I_{CCTB}	V_{INB} = V_{CCB} − 0.6 V PER INPUT		3.6	5.0 ± 0.5	—	500	
	I_{CCTA}	V_{INA} = 3.4 V PER INPUT		2.3~3.6	5.5	—	2.0	mA

AC Characteristics (Input $t_r = t_f = 3$ ns, $R_L = 500\ \Omega$)
$V_{CCB} = 3.3 \pm 0.3$ V

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CCA} (V)	Ta = −40~85°C		UNIT
					MIN	MAX	
Propagation Delay Time (Bn ⇒ An)	t_{pLH} t_{pHL}	Input : Bn Ouptut : An (DIR = "L")	50	5.0 ± 0.5	1.0	6.0	ns
3-State Output Enable Time ($\overline{OE}$ ⇒ An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	9.0	
3-State Output Disable Time ($\overline{OE}$ ⇒ An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.0	
Propagation Delay Time (An ⇒ Bn)	t_{pLH} t_{pHL}	Input : An Ouptut : Bn (DIR = "H")	50	5.0 ± 0.5	1.0	7.0	ns
3-State Output Enable Time ($\overline{OE}$ ⇒ Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	9.0	
3-State Output Disable Time ($\overline{OE}$ ⇒ Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 10)	50	5.0 ± 0.5	—	1.0	ns

$V_{CCB} = 2.5 \pm 0.2$ V

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CCA} (V)	Ta = −40~85°C		UNIT
					MIN	MAX	
Propagation Delay Time (Bn ⇒ An)	t_{pLH} t_{pHL}	Input : Bn Ouptut : An (DIR = "L")	50	5.0 ± 0.5	1.0	8.0	ns
3-State Output Enable Time ($\overline{OE}$ ⇒ An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	12.0	
3-State Output Disable Time ($\overline{OE}$ ⇒ An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	12.0	
Propagation Delay Time (An ⇒ Bn)	t_{pLH} t_{pHL}	Input : An Ouptut : Bn (DIR = "H")	30	5.0 ± 0.5	1.0	9.0	ns
3-State Output Enable Time ($\overline{OE}$ ⇒ Bn)	t_{pZL} t_{pZH}		30	5.0 ± 0.5	1.0	12.0	
3-State Output Disable Time ($\overline{OE}$ ⇒ Bn)	t_{pLZ} t_{pHZ}		30	5.0 ± 0.5	1.0	10.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 10)	30 or 50	5.0 ± 0.5	—	1.0	ns

(Note 10) : Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

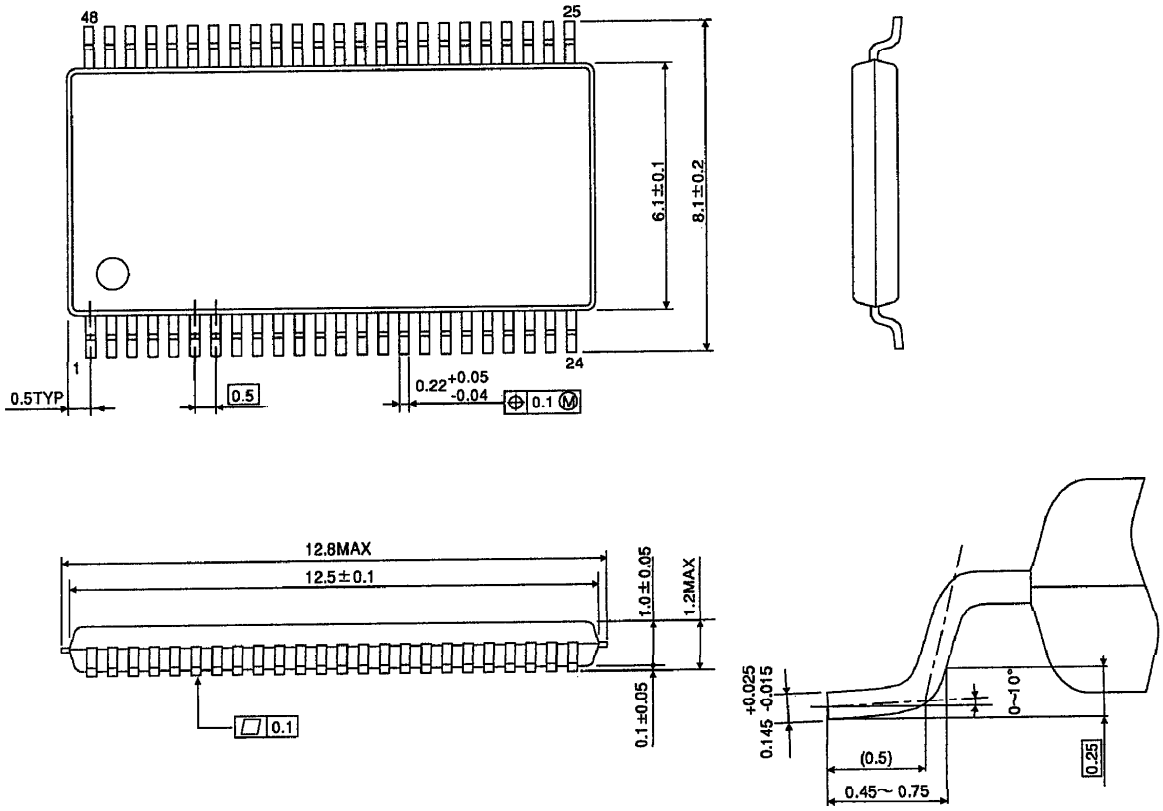
Capacitive characteristics (Ta = 25°C)
V_{CCB} = 2.5, 3.3 V

PARAMETER	SYMBOL	TEST CONDITION	V_{CCA} (V)	TYP.	UNIT
Input Capacitance	C_{IN}	DIR, $\overline{OE}$	5.0	TBD	pF
Output Capacitance	$C_{I/O}$	An, Bn	5.0	TBD	pF
Power Dissipation Capacitance (Note 11)	C_{PDA}	A ⇒ B (DIR = "H")	5.0	20	pF
		B ⇒ A (DIR = "L")	5.0	66	
	C_{PDB}	A ⇒ B (DIR = "H")	5.0	34	
		B ⇒ A (DIR = "L")	5.0	4	

(Note 11) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16$ (per bit)

OUTLINE DRAWING

TSSOP48-P-0061-0.50 Unit : mm



Weight : 0.25 g (Typ.)