Micropower, Single Supply Rail-to-Rail Output Instrumentation Amplifier

FEATURES

- **Micropower: 95μA Max Supply Current**
- **Low Input Offset Voltage: 100μV Max**
- **Low Input Offset Voltage Drift: 0.5μV/°C Max**
- **Single Gain Set Resistor: G = 1 to 1000**
- **Inputs Common Mode to V⁻**
- **Wide Supply Range: 2.2V to 36V Total Supply**
- CMRR: G = 10, 96dB Min
- Gain Error: G = 10, 0.25% Max
- Gain Nonlinearity: G = 10, 40ppm Max
- Input Bias Current: 40nA Max
- PSRR: G = 10, 100dB Min
- Rail-to-Rail Output
- 100Hz Voltage Noise: 48nV/√Hz
- 0.1Hz to 10Hz Noise: 1.5μV$_{P-P}$

APPLICATIONS

- Portable Instrumentation
- Bridge Amplifiers
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Differential to Single-Ended Converters
- Medical Instrumentation

DESCRIPTION

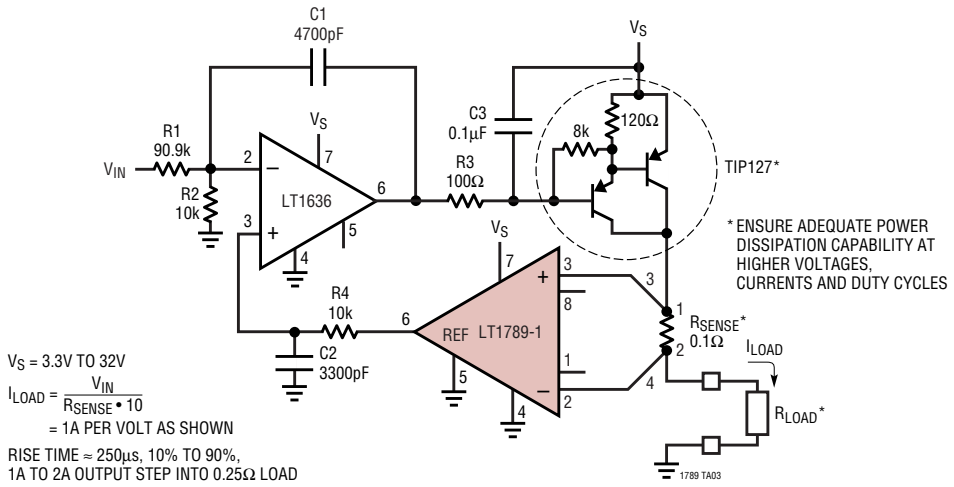
The LT®1789-1 is a micropower, precision instrumentation amplifier that is optimized for low voltage single supply operation, with a quiescent current of 95μA max for 2.2V to 36V supplies, inputs that common mode to ground and an output that swings within 100mV of ground. The LT1789-1 requires only one external resistor to set gains of 1 to 1000.

The high accuracy of the LT1789-1 (40ppm maximum nonlinearity and 0.25% max gain error) is unmatched by other micropower instrumentation amplifiers. The LT1789-1 is laser trimmed for very low input offset voltage (100μV max), drift (0.5μV/°C), high CMRR (96dB, G = 10) and PSRR (100dB, G = 10). The output can handle capacitive loads up to 400pF in any gain configuration while the inputs are ESD protected up to 10kV (human body model).

The LT1789-1 is offered in the 8-pin SO package, requiring significantly less PC board area than discrete multi op amp and resistor designs. The LT1789-1 is the best choice for circuits requiring precision, micropower and low supply voltage operation.

TYPICAL APPLICATION

0.5A to 4A Voltage Controlled Current Source

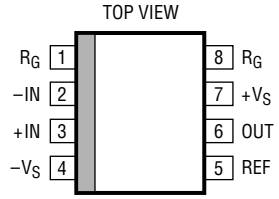


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage 36V
Input Current (Note 3) ..... ±20mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 4)
LT1789C-1 (Note 4) ..... –40°C to 85°C
LT1789I-1 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1789CS8-1 LT1789IS8-1
S8 PART MARKING
17891 1789I1

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = 3V, 0V; V_S = 5V, 0V; R_L = 20k, V_{CM} = V_{REF} = half supply, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G	Gain Range	G = 1 + (200k/R_G)	1		1000	
	Gain Error (Note 6)	G = 1, V_O = (–V_S) + 0.1V to (+V_S) – 1V G = 10, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V (Note 2) G = 100, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V (Note 2) G = 1000, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V (Note 2)		0.02 0.06 0.06 0.13	0.20 0.25 0.27	% % % %
	Gain Nonlinearity (Note 6)	G = 1, V_O = (–V_S) + 0.1V to (+V_S) – 1V G = 10, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V G = 100, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V G = 1000, V_O = (–V_S) + 0.1V to (+V_S) – 0.3V		35 12 18 90	100 40 75	ppm ppm ppm ppm
V_{OST}	Total Input Referred Offset Voltage	V_{OST} = V_{OSI} + V_{OSO}/G				
V_{OSI}	Input Offset Voltage	G = 1000		15	100	µV
V_{OSO}	Output Offset Voltage	G = 1		150	750	µV
I_{OS}	Input Offset Current	(Note 6)		0.2	4	nA
I_B	Input Bias Current	(Note 6)		19	40	nA
e_n	Input Noise Voltage, RTI (Referred to Input)	G = 1, f_O = 0.1Hz to 10Hz G = 10 G = 100, 1000		5.0 1.5 1.0		μV_{P-P} μV_{P-P} μV_{P-P}
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$						
e_{ni}	Input Noise Voltage Density, RTI	f_O = 100Hz (Note 7)		48	85	$nV/\sqrt{Hz}$
e_{no}	Output Noise Voltage Density, RTI	f_O = 100Hz		330		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f_O = 0.1Hz to 10Hz		16		pA_{P-P}
	Input Noise Current Density	f_O = 100Hz		100		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{IN} = 0V to (+V_S) – 1V (Note 6)	0.75	1.6		GΩ
C_{IN}	Input Capacitance	Differential Common Mode		20 17		pF pF
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	0		(+V_S) – 1	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to (+V_S) – 1V (Note 6) G = 1 G = 10 G = 100, 1000	 79 96 100	 88 106 114		 dB dB dB

ELECTRICAL CHARACTERISTICS

V_S = 3V, 0V; V_S = 5V, 0V; R_L = 20k, V_{CM} = V_{REF} = half supply, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V, V_{CM} = V_{REF} = 1V G = 1 G = 10 G = 100, 1000	 90 100 102	 100 113 116		 dB dB dB
	Minimum Supply Voltage			2.2	2.5	V
I_S	Supply Current	(Note 7)		67	95	µA
V_{OL}	Output Voltage Swing LOW			54	100	mV
V_{OH}	Output Voltage Swing HIGH		$(+V_S) - 0.3$	$(+V_S) - 0.19$		V
I_{SC}	Short-Circuit Current	Short to GND Short to $+V_S$		1.9 7.6		mA mA
BW	Bandwidth	G = 1 G = 10 G = 100 G = 1000		60 30 3 0.2		kHz kHz kHz kHz
SR	Slew Rate	G = 1, V_{OUT} = 0.1V to 2.1V		0.021		V/µs
	Settling Time to 0.01%	4V Step, G = 1, V_S = 5V		260		µs
R_{REFIN}	Reference Input Resistance			220		kΩ
I_{REFIN}	Reference Input Current			2.7		µA
AV_{REF}	Reference Gain to Output			1 ±0.0001		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $0°C \le T_A \le 70°C$. V_S = 3V, 0V; V_S = 5V, 0V; R_L = 20k, $V_{CM} = V_{REF}$ = half supply, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Error (Note 6)	G = 1, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 1V$ G = 10, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$ (Note 2) G = 100, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$ (Note 2)	● ● ●			0.25 0.30 0.32	% % %
	Gain Nonlinearity (Note 6)	G = 1, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 1V$ G = 10, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$ G = 100, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$	● ● ●			185 90 120	ppm ppm ppm
G/T	Gain vs Temperature	G < 1000 (Notes 2, 3)	●		5	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$					
V_{OSI}	Input Offset Voltage	G = 1000	●			150	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●		3	10	µV
V_{OSO}	Output Offset Voltage	G = 1	●			950	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●		50	100	µV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●		0.2	0.5	µV/°C
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●		1.5	4	µV/°C
I_{OS}	Input Offset Current	(Note 6)	●			4.5	nA
I_{OS}/T	Input Offset Current Drift		●		3		pA/°C
I_B	Input Bias Current	(Note 6)	●			45	nA
I_B/T	Input Bias Current Drift		●		50		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	●	0.2		$(+V_S) - 1$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0.2V to $(+V_S) - 1V$ (Note 6) G = 1 G = 10 G = 100, 1000	 ● ● ●	 77 94 98			 dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V, $V_{CM} = V_{REF}$ = 1V G = 1 G = 10 G = 100, 1000	 ● ● ●	 88 98 100			 dB dB dB
	Minimum Supply Voltage		●			2.5	V
I_S	Supply Current	(Note 7)	●			115	µA
V_{OL}	Output Voltage Swing LOW		●			110	mV
V_{OH}	Output Voltage Swing HIGH		●	$(+V_S) - 0.38$			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40°C \le T_A \le 85°C$. V_S = 3V, 0V; V_S = 5V, 0V; R_L = 20k, $V_{CM} = V_{REF}$ = half supply, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Error (Note 6)	G = 1, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 1V$	●			0.30	%
		G = 10, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$ (Note 2)	●			0.35	%
		G = 100, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$ (Note 2)	●			0.37	%
	Gain Nonlinearity (Note 6)	G = 1, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 1V$	●			250	ppm
		G = 10, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$	●			105	ppm
		G = 100, $V_O = (-V_S) + 0.3V$ to $(+V_S) - 0.5V$	●			160	ppm
G/T	Gain vs Temperature	G < 1000 (Notes 2, 3)	●		5	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$					
V_{OSI}	Input Offset Voltage	G = 1000	●			175	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●		3	10	µV
V_{OSO}	Output Offset Voltage	G = 1	●			1050	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●		50	100	µV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●		0.2	0.5	µV/°C
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●		1.5	4	µV/°C
I_{OS}	Input Offset Current	(Note 6)	●			5	nA
I_{OS}/T	Input Offset Current Drift		●		3		pA/°C
I_B	Input Bias Current	(Note 6)	●			50	nA
I_B/T	Input Bias Current Drift		●		50		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	●	0.2		$(+V_S) - 1$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0.2V to $(+V_S) - 1V$ (Note 6)					
		G = 1	●	75			dB
		G = 10	●	92			dB
		G = 100, 1000	●	96			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V, $V_{CM} = V_{REF}$ = 1V					
		G = 1	●	86			dB
		G = 10	●	96			dB
		G = 100, 1000	●	98			dB
	Minimum Supply Voltage		●			2.5	V
I_S	Supply Current	(Note 7)	●			125	µA
V_{OL}	Output Voltage Swing LOW		●			120	mV
V_{OH}	Output Voltage Swing HIGH		●	$(+V_S) - 0.40$			V

ELECTRICAL CHARACTERISTICS

V_S = ±15V, R_L = 20k, V_{CM} = V_{REF} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G	Gain Range	G = 1 + (200k/R_G)	1		1000	
	Gain Error	V_O = ±10V				
		G = 1		0.01	0.10	%
		G = 10 (Note 2)		0.04	0.15	%
		G = 100 (Note 2)		0.04	0.15	%
		G = 1000 (Note 2)		0.07	0.20	%
	Gain Nonlinearity	V_O = ±10V				
		G = 1		8	20	ppm
		G = 10		1	10	ppm
		G = 100		6	20	ppm
		G = 1000		20	100	ppm
V_{OST}	Total Input Referred Offset Voltage	V_{OST} = V_{OSI} + V_{OSO}/G				
V_{OSI}	Input Offset Voltage	G = 1000		30	235	µV
V_{OSO}	Output Offset Voltage	G = 1		200	1	mV
I_{OS}	Input Offset Current			0.2	4	nA
I_B	Input Bias Current			17	40	nA
e_n	Input Noise Voltage, RTI	f_O = 0.1Hz to 10Hz				
		G = 1		5.0		μV_{P-P}
		G = 10		1.5		μV_{P-P}
		G = 100, 1000		1.0		μV_{P-P}
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$						
e_{ni}	Input Noise Voltage Density, RTI	f_O = 100Hz		49	80	$nV/\sqrt{Hz}$
e_{no}	Output Noise Voltage Density, RTI	f_O = 100Hz		330		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f_O = 0.1Hz to 10Hz		19		pA_{P-P}
	Input Noise Current Density	f_O = 100Hz		100		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance		2	4.7		GΩ
C_{IN}	Input Capacitance	Differential		20		pF
		Common Mode		17		pF
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	–15		14	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = –15V to 14V				
		G = 1	80	89		dB
		G = 10	98	108		dB
		G = 100, 1000	102	117		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.25V to ±16V				
		G = 1	94	107		dB
		G = 10	104	118		dB
		G = 100, 1000	106	121		dB
	Minimum Supply Voltage				±1.25	V
I_S	Supply Current			85	130	µA
V_O	Output Voltage Swing		±14.5	±14.7		V
I_{SC}	Short-Circuit Current	Short to –V_S		2.2		mA
		Short to +V_S		8.5		mA

ELECTRICAL CHARACTERISTICS

V_S = ±15V, R_L = 20k, V_{CM} = V_{REF} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BW	Bandwidth	G = 1 G = 10 G = 100 G = 1000		60 30 3 0.2		kHz kHz kHz kHz
SR	Slew Rate	G = 1, V_{OUT} = ±10V	0.012	0.026		V/µs
	Settling Time to 0.01%	10V Step, G = 1		460		µs
R_{REFIN}	Reference Input Resistance			220		kΩ
I_{REFIN}	Reference Input Current	V_{REF} = 0		2.7		µA
AV_{REF}	Reference Gain to Output			1 ±0.0001		

The ● denotes the specifications which apply over the temperature range of 0°C ≤ T_A ≤ 70°C. V_S = ±15V, R_L = 20k, V_{CM} = V_{REF} = 0V, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Error	V_O = ±10V					
		G = 1	●			0.15	%
		G = 10 (Note 2)	●			0.20	%
		G = 100 (Note 2)	●			0.20	%
		G = 1000 (Note 2)	●			0.30	%
	Gain Nonlinearity	V_O = ±10V					
		G = 1	●			25	ppm
		G = 10	●			15	ppm
		G = 100	●			25	ppm
		G = 1000	●			120	ppm
G/T	Gain vs Temperature	G < 1000 (Notes 2, 3)	●		5	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	V_{OST} = V_{OSI} + V_{OSO}/G					
V_{OSI}	Input Offset Voltage	G = 1000	●			285	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●		8	30	µV
V_{OSO}	Output Offset Voltage	G = 1	●			1.2	mV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●		50	120	µV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●		0.2	0.7	µV/°C
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●		1.5	5	µV/°C
I_{OS}	Input Offset Current		●			4.5	nA
I_{OS}/T	Input Offset Current Drift		●		2		pA/°C
I_B	Input Bias Current		●			45	nA
I_B/T	Input Bias Current Drift		●		35		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	●	–14.8		14	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = –14.8V to 14V					
		G = 1	●	78			dB
		G = 10	●	96			dB
		G = 100, 1000	●	100			dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $0°C \le T_A \le 70°C$. $V_S = \pm15V$, $R_L = 20k$, $V_{CM} = V_{REF} = 0V$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.25V$ to $\pm16V$					
		G = 1	●	92			dB
		G = 10	●	102			dB
		G = 100, 1000	●	104			dB
	Minimum Supply Voltage		●			±1.25	V
I_S	Supply Current		●			150	µA
V_O	Output Voltage Swing		●	±14.25			V
SR	Slew Rate	G = 1, $V_{OUT} = \pm10V$	●	0.010			V/µs

The ● denotes the specifications which apply over the temperature range of $-40°C \le T_A \le 85°C$. $V_S = \pm15V$, $R_L = 20k$, $V_{CM} = V_{REF} = 0V$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Error	$V_O = \pm10V$					
		G = 1	●			0.20	%
		G = 10 (Note 2)	●			0.25	%
		G = 100 (Note 2)	●			0.25	%
		G = 1000 (Note 2)	●			0.40	%
	Gain Nonlinearity	$V_O = \pm10V$					
		G = 1	●			30	ppm
		G = 10	●			20	ppm
		G = 100	●			30	ppm
		G = 1000	●			130	ppm
G/T	Gain vs Temperature	G < 1000 (Notes 2, 3)	●		5	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$					
V_{OSI}	Input Offset Voltage	G = 1000	●			305	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●		8	30	µV
V_{OSO}	Output Offset Voltage	G = 1	●			1.3	mV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●		50	120	µV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●		0.2	0.7	µV/°C
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●		1.5	5	µV/°C
I_{OS}	Input Offset Current		●			5	nA
I_{OS}/T	Input Offset Current Drift		●		2		pA/°C
I_B	Input Bias Current		●			50	nA
I_B/T	Input Bias Current Drift		●		35		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded	●	−14.8		$(+V_S) - 1$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = -14.8V$ to 14V					
		G = 1	●	76			dB
		G = 10	●	94			dB
		G = 100, 1000	●	98			dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40°C \le T_A \le 85°C$. $V_S = \pm15V$, $R_L = 20k$, $V_{CM} = V_{REF} = 0V$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.25V$ to $\pm16V$					
		G = 1	●	90			dB
		G = 10	●	100			dB
		G = 100, 1000	●	102			dB
	Minimum Supply Voltage		●	±1.25			V
I_S	Supply Current		●			160	µA
V_O	Output Voltage Swing		●	±14.15			V
SR	Slew Rate	G = 1, $V_{OUT} = \pm10V$	●	0.008			V/µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Does not include the effect of the external gain resistor R_G.

Note 3: This parameter is not 100% tested.

Note 4: The LT1789C-1 is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. The LT1789I-1 is guaranteed to meet the extended temperature limits.

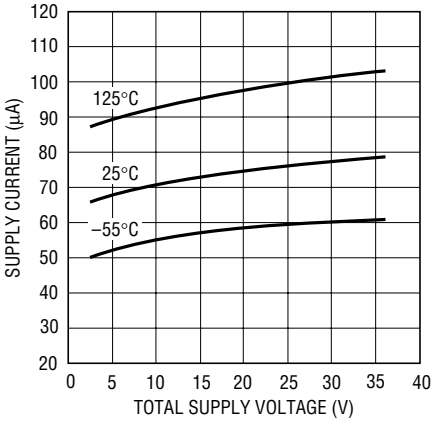
Note 5: Hysteresis in offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage hysteresis is always measured at 25°C, but the IC is cycled to 85°C I-grade (or 70°C C-grade) or –40°C I-grade (0°C C-grade) before successive measurement. 60% of the parts will pass the typical limit on the data sheet.

Note 6: $V_S = 5V$ limits are guaranteed by correlation to $V_S = 3V$ and $V_S = \pm15V$ tests.

Note 7: $V_S = 3V$ limits are guaranteed by correlation to $V_S = 5V$ and $V_S = \pm15V$ tests.

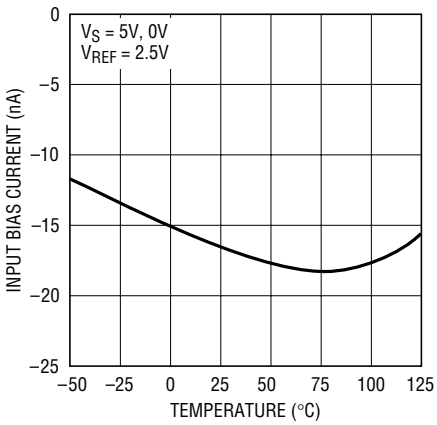
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



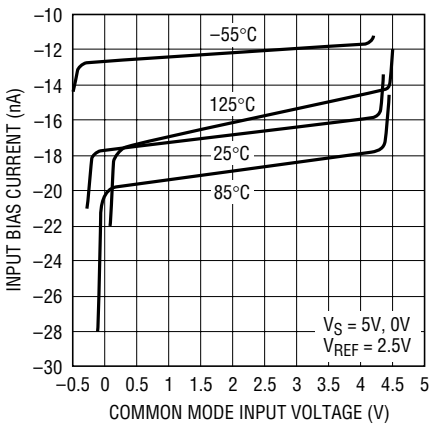
1789 G01

Input Bias Current vs Temperature



1789 G02

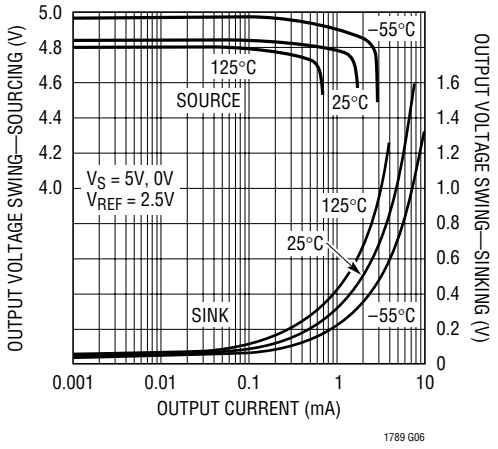
Input Bias Current vs Common Mode Input Voltage



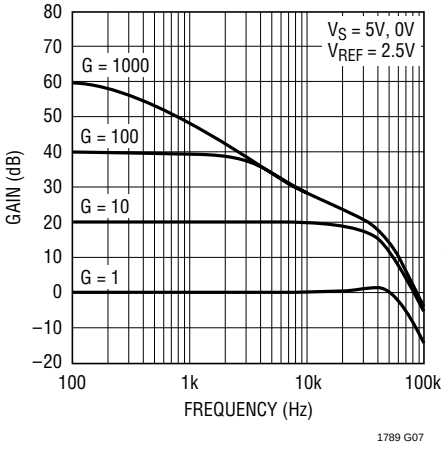
1789 G03

TYPICAL PERFORMANCE CHARACTERISTICS

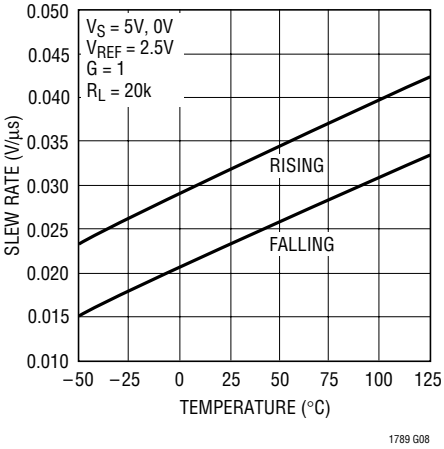
Output Voltage Swing vs Load Current



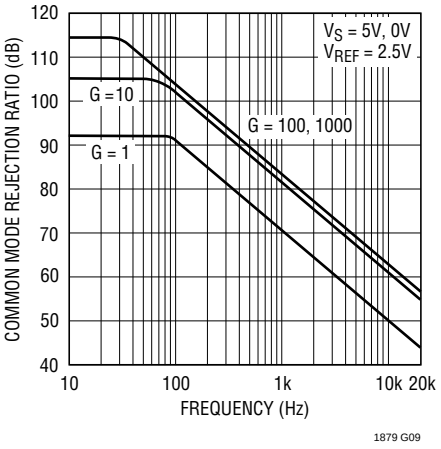
Gain vs Frequency



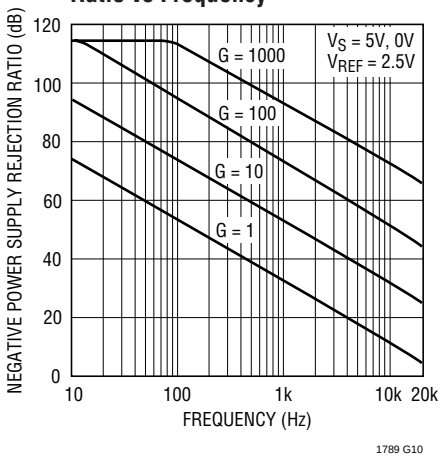
Slew Rate vs Temperature



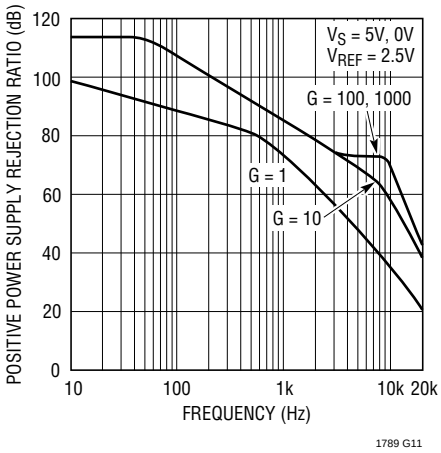
Common Mode Rejection Ratio vs Frequency



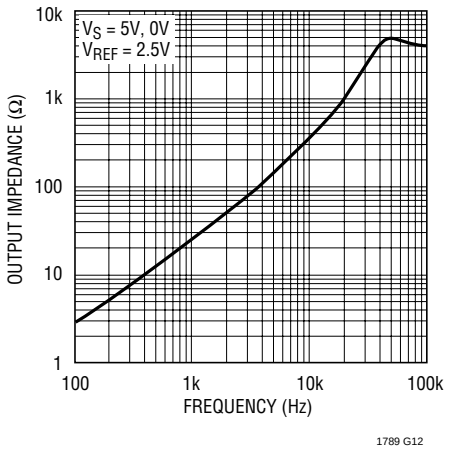
Negative Power Supply Rejection Ratio vs Frequency



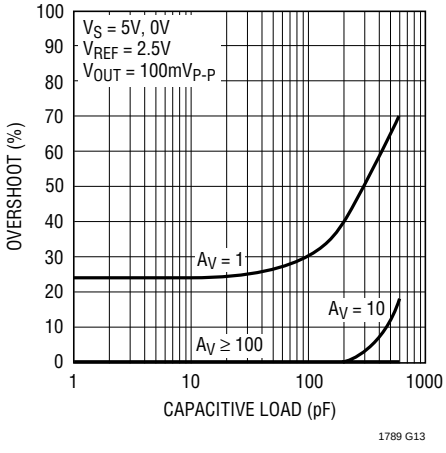
Positive Power Supply Rejection Ratio vs Frequency



Output Impedance vs Frequency

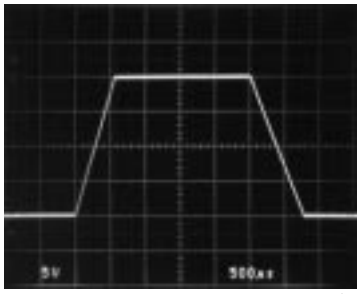


Overshoot vs Capacitive Load



TYPICAL PERFORMANCE CHARACTERISTICS

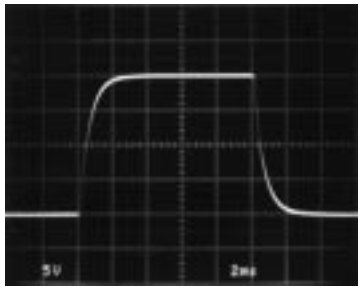
Large-Signal Transient Response



1789-1 G14

G = 1, 10, 100 500µs/DIV
V_S = ±15V
R_L = 20k
C_L = 50pF

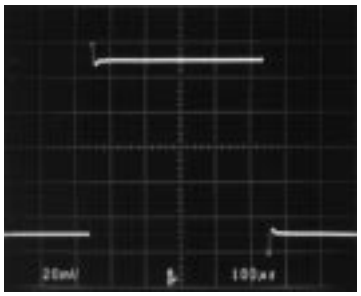
Large-Signal Transient Response



1789-1 G15

G = 1000 2ms/DIV
V_S = ±15V
R_L = 20k
C_L = 50pF

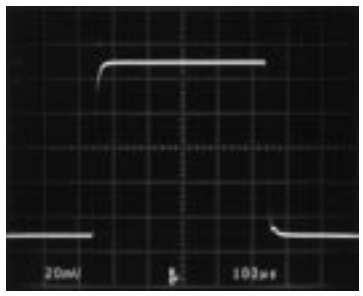
Small-Signal Transient Response



1789-1 G16

G = 1 100µs/DIV
V_S = 5V, 0V
V_{REF} = 2.5V
R_L = 20k
C_L = 50pF

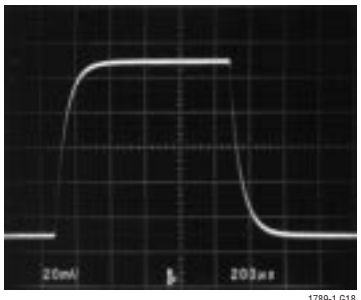
Small-Signal Transient Response



1789-1 G17

G = 10 100µs/DIV
V_S = 5V, 0V
V_{REF} = 2.5V
R_L = 20k
C_L = 50pF

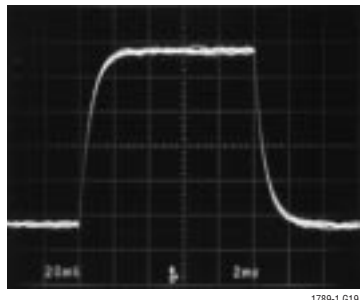
Small-Signal Transient Response



1789-1 G18

G = 100 200µs/DIV
V_S = 5V, 0V
V_{REF} = 2.5V
R_L = 20k
C_L = 50pF

Small-Signal Transient Response



1789-1 G19

G = 1000 2ms/DIV
V_S = 5V, 0V
V_{REF} = 2.5V
R_L = 20k
C_L = 50pF

BLOCK DIAGRAM

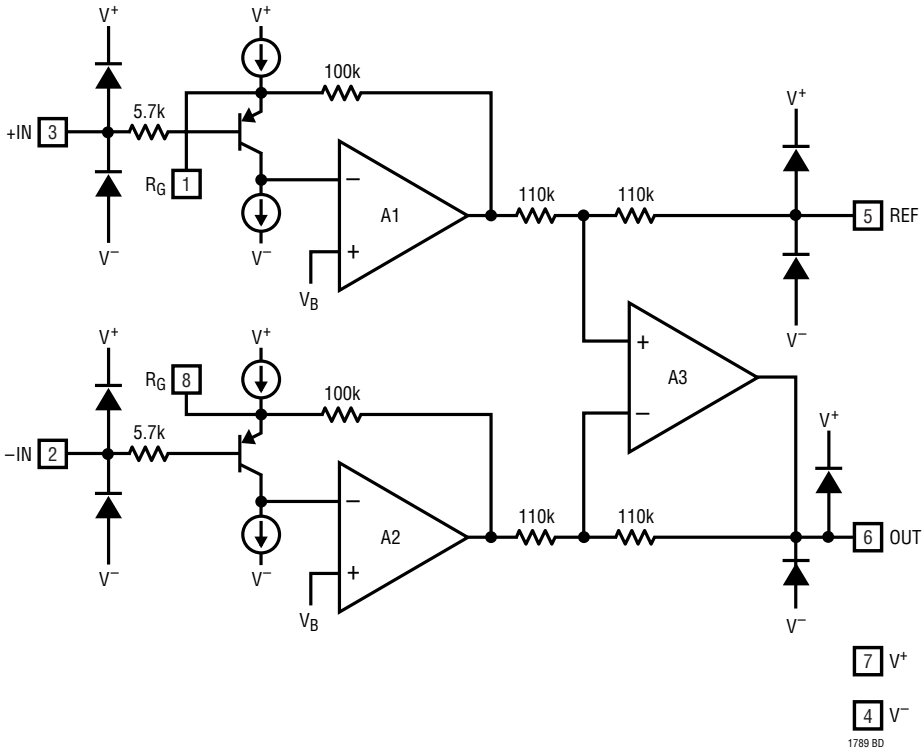


Figure 1. Block Diagram

APPLICATIONS INFORMATION

Input and Output Offset Voltage

The offset voltage of the LT1789-1 has two components: the output offset and the input offset. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain (G) and adding it to the input offset. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI)
= input offset + (output offset/G)

Total output offset voltage (RTO)
= (input offset • G) + output offset

Reference Terminal

The reference terminal is one end of one of the four 110k resistors around the difference amplifier. The output voltage of the LT1789-1 (Pin 6) is referenced to the voltage on the reference terminal (Pin 5). Resistance in series with the REF pin must be minimized for best common mode rejection. For example, a 22Ω resistance from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB.

Single Supply Operation

For single supply operation, the REF pin can be at the same potential as the negative supply (Pin 4) provided the output of the instrumentation amplifier remains inside the specified operating range.

Care must be taken to prevent the outputs of the input buffer amplifiers (A1, A2) from saturating. This problem can occur when the gain is greater than one and the inputs approach either the negative supply ($-V_S$) or the positive supply ($+V_S$). As the LT1789-1 Block Diagram (Figure 1)

APPLICATIONS INFORMATION

shows, the gain pins of A1 and A2 sit about 0.5V above their respective inputs. This translates to approximately 0.5V of output swing before saturation occurs when one of the inputs is at its common mode limit ($-V_S$ or $+V_S-1V$). The combinations of gain and input voltage that can cause output saturation are too many to enumerate. However, the maximum allowable differential input voltage for a valid output can be closely approximated by the following relationships:

For inputs operating near $-V_S$, the maximum differential input voltage can be found by adding 0.5V to the difference between $-V_S$ and the input closest to $-V_S$, and dividing this voltage by $100k\Omega/R_G$.

For example, with V_S = 5V, 0V; –IN = 1V; R_G = 22.2k (G = 10), $V_{REF} = -V_S$, the maximum differential input voltage will be equal to:

$(1V + 0.5V)/(100k\Omega/22.2k\Omega) = 0.333V$

Since the negative input (–IN) is equal to 1V, the output of A1 will saturate if the positive input (+IN) exceeds 1.333V.

For inputs operating near $+V_S$, 0.5V must be subtracted from the difference between $+V_S$ and the input closest to $+V_S$, and again dividing by $100k\Omega/RG$.

For example, with V_S = 5V,0V; +IN = 4V; R_G = 50k (G = 5), $V_{REF} = -V_S$, the maximum differential input voltage will be equal to:

$(1V – 0.5V)/(100k\Omega/50k\Omega) = 0.25V$

In this case, since the positive input is equal to 4V, the output of A2 will saturate if the negative input goes below 3.75V.

Output Offset Trimming

The LT1789-1 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset needs to be adjusted, the circuit in Figure 2 is an example of an optional offset adjust circuit. The op amp buffer provides a low impedance to the REF pin where resistance must be kept to a minimum for best CMRR and lowest gain error.

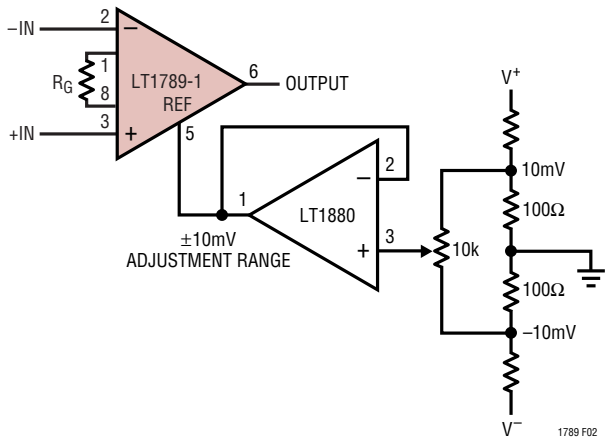


Figure 2. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The low input bias current of the LT1789-1 (19nA) and the high input impedance (1.6GΩ) allow the use of high impedance sources without introducing significant offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path the inputs will float high and exceed the input common mode range of the LT1789-1, resulting in a saturated input stage. Figure 3 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

APPLICATIONS INFORMATION

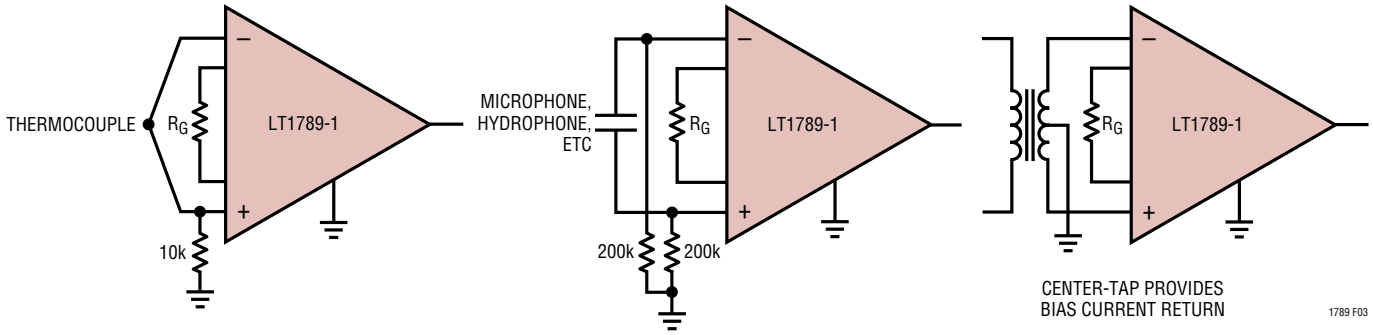
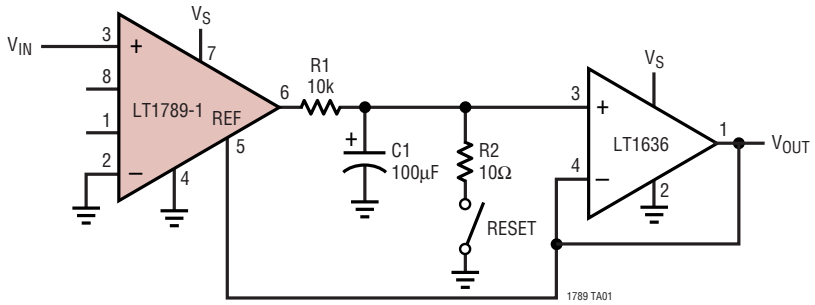


Figure 3. Providing an Input Common Mode Current Path

TYPICAL APPLICATION

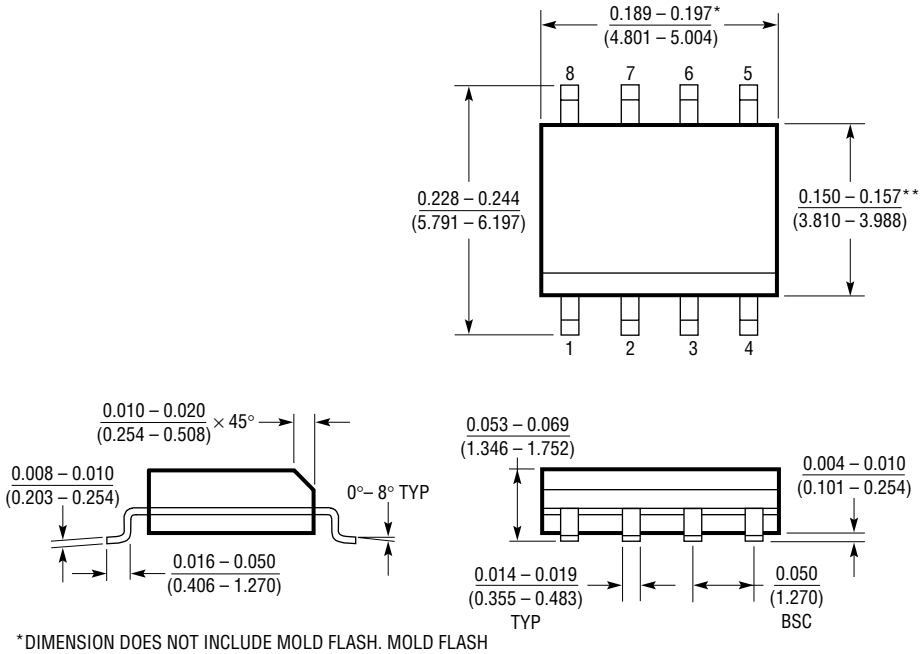
Single Supply Positive Integrator



V_S = 2.7V TO 32V
TIME CONSTANT = (R1)(C1) = 1 SECOND AS SHOWN

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



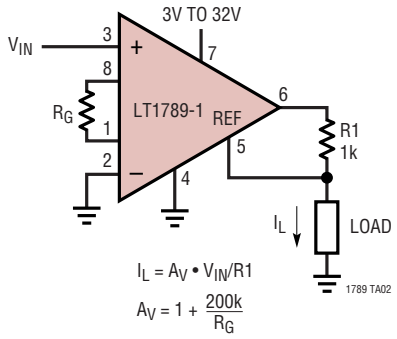
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

TYPICAL APPLICATION

Voltage Controlled Current Source



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1100	Precision Chopper-Stabilized Instrumentation Amplifier	Best DC Accuracy
LT1101	Precision, Micropower, Single Supply Instrumentation Amplifier	Fixed Gain of 10 or 100, I_S < 105µA
LT1102	High Speed, JFET Instrumentation Amplifier	Fixed Gain of 10 or 100, 30V/µs Slew Rate
LT1167	Single Resistor Gain Programmable, Precision Instrumentation Amplifier	Gain Error: 0.08% Max, Gain Nonlinearity: 10ppm Max, 60µV Max Input Offset Voltage, 90dB Min CMRR
LT1168	Low Power, Single Resistor Programmable Instrumentation Amplifier	I_{SUPPLY} = 530µA Max
LTC®1418	14-Bit, Low Power, 200ksps ADC with Serial and Parallel I/O	Single Supply 5V or ±5V Operation, ±1.5LSB INL and ±1LSB DNL Max
LT1460	Precision Series Reference	Micropower; 2.5V, 5V, 10V Versions; High Precision
LT1468	16-Bit Accurate Op Amp, Low Noise Fast Settling	16-Bit Accuracy at Low and High Frequencies, 90MHz GBW, 22V/µs, 900ns Settling
LTC1562	Active RC Filter	Lowpass, Bandpass, Highpass Responses; Low Noise, Low Distortion, Four 2nd Order Filter Sections
LTC1605	16-Bit, 100ksps, Sampling ADC	Single 5V Supply, Bipolar Input Range: ±10V, Power Dissipation: 55mW Typ

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