LTC1531

Self-Powered Isolated Comparator

October 1998

FEATURES

- **Self-Powered Across Isolation Barrier**
- **3000V_{RMS} Isolation**
- **2.5V Isolated Reference, I_{LOAD} = 5mA_{MAX}**
- UL Qualification Pending
- Zero-Cross Output for Line Power
- Dual Differential Input Comparator
- High Input Impedance Comparator

APPLICATIONS

- Self-Powered Isolated Sensing
- Isolated Temperature Control
- Isolated Voltage Monitor
- Isolated Switch Control

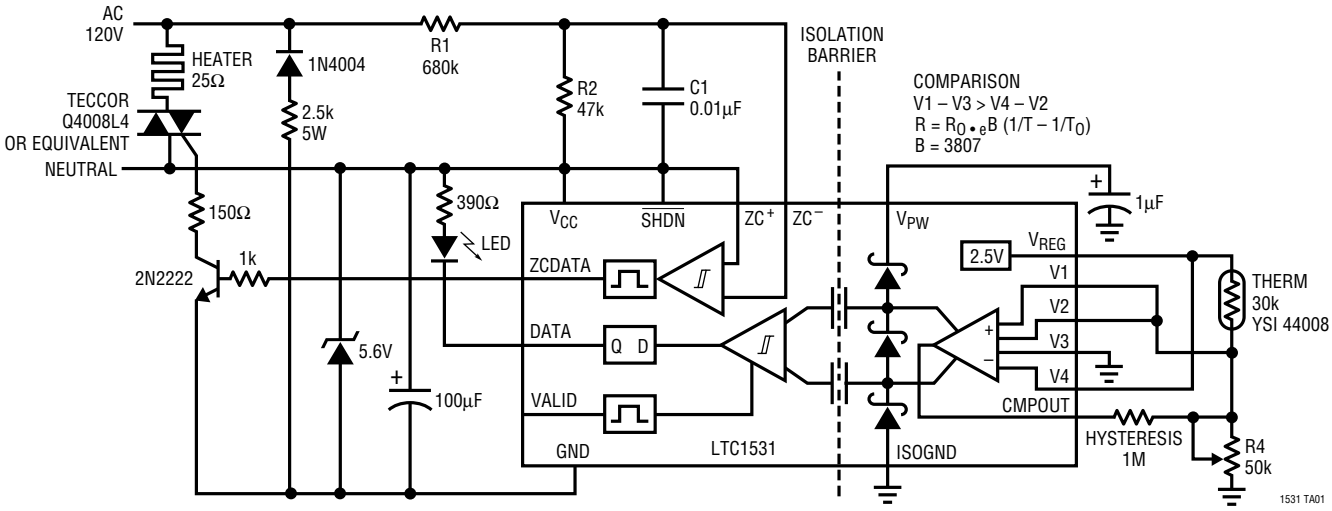
DESCRIPTION

The LTC®1531 is an isolated self-powered dual differential comparator. An internal capacitive isolation barrier provides 3000V_{RMS} of isolation between the comparator and its output. The part provides UL-rated isolated comparisons without the need for an isolated supply since both comparator power and output data are transmitted across the capacitive barrier. The comparator data is transferred differentially across the isolation barrier to provide high common mode voltage and noise immunity.

The isolated side can supply a 2.5V reference output to power external sensor circuits such as a thermistor bridge. The dual differential comparator inputs allow for comparison of two differential voltages as well as single-ended voltages. The powered side provides a latched data output as well as a pulsed zero-cross comparator output for controlling a triac. The part is available in a 28-lead SO package.

TYPICAL APPLICATION

Isolated Thermistor Temperature Controller

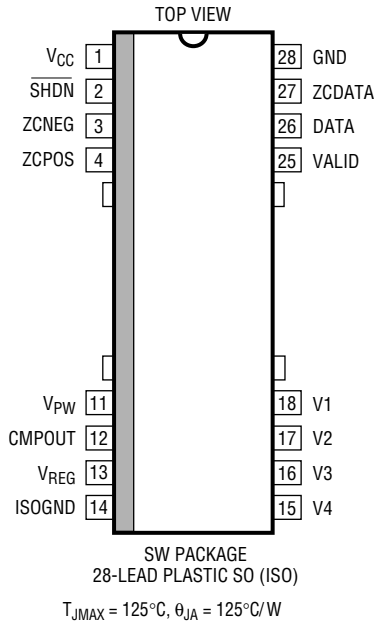


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND) 7V
Input Voltages
  Isolated Comparator
  (V1 to V4) ..... –0.3V to (V_{PW} + 0.3V)
  $\overline{SHDN}$, ZCPOS, ZCNEG ..... –0.3V to 12V
Current
  Input Pins ..... ±10mA
  ZCDATA, VALID, DATA ..... ±10mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
28-LEAD PLASTIC SO (ISO)

T_{JMAX} = 125°C, θ_{JA} = 125°C/W

ORDER PART NUMBER
LTC1531CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VCC}	Supply Current	$\overline{SHDN}$ = V_{CC}, No Load $\overline{SHDN}$ = 0V	● ●		10 0.2	14 10	mA µA
V_{ZCOS}	Zero-Cross Offset		●		±30	±120	mV
V_{HYS}	Zero-Cross Hysteresis	(Note 7)	●		200	800	mV
V_{CMR}	Zero-Cross Input Common Mode Range		●	(V_{CC}/2)+0.5		V_{CC}	V
f_{SAMPLE}	Isolated Comparator Sample Rate	V_{REG} Not Loaded (Note 2)			300		Hz
V_{OS}	Isolated Comparator Offset	V1 = V2, V3 = V4 V1 – V3 = 2V, V4 – V2 = 2V	● ●		2.0 2.0	4.0 4.0	mV mV
Q_{INJ}	Isolated Comparator Input Charge Injection	V1 = V3 = 2.5V, V2 = V4 = 0V (Note 3)			±4		pC
I_{VIN}	Isolated Comparator Input Current	V1 = V3 – 2.5V, V2 = V4 = 0V f_{SAMPLE} = 700Hz (Note 4)			±1		nA
V_{REG}	V_{REG}	2mA Load V_{PW} = 3V (Note 5)	●	2.40	2.50	2.55	V
R_{VREG}	V_{REG} Output Impedance	2mA to 5mA Load	●		4	15	Ω
I_{CMPOUT}	CMPOUT High Impedance Leakage Current	V_{CMPOUT} = 2.5V			1		nA
t_{VREG}	V_{REG} On-Time		●	90	105	130	µs
V_{PWH}	V_{PW}, Power Detect Enable Voltage				3.3		V
I_{VPW}	Current Transfer to V_{PW}	V_{PW} = 0V V_{PW} = 3.3V			45 30		µA µA
V_{ISO}	Isolation Voltage	1 Minute (Note 6) 1 Second	● ●	2500 3000			V_{RMS} V_{RMS}

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	$\overline{SHDN}$ Input High Voltage	V_{CC} = 4.5V	●	2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage	V_{CC} = 5.5V	●			0.8	V
V_{OH}	DATA, VALID, ZCDATA Output High Voltage	V_{CC} = 4.5V, I_O = 400µA	●	3.0	4.3		V
V_{OL}	DATA, VALID, ZCDATA Output Low Voltage	V_{CC} = 4.5V, I_O = 1.6mA	●		0.2	0.4	V
I_{INL}, I_{INH}	$\overline{SHDN}$ Low or High Level Input Current	V_{IN} = 5V, 0V	●			±1	µA
dV/dt	Continuous dV/dt Rejection	(Note 8)	●	50	70		V/µs

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The sample rate is not continuous, but depends on V_{PW} charging rate. See Applications Information.

Note 3: See Applications Information for further description of the comparator switched-capacitor input circuit.

Note 4: The sample rate, f_{SAMPLE}, varies with loading on V_{PW} and V_{REG}.

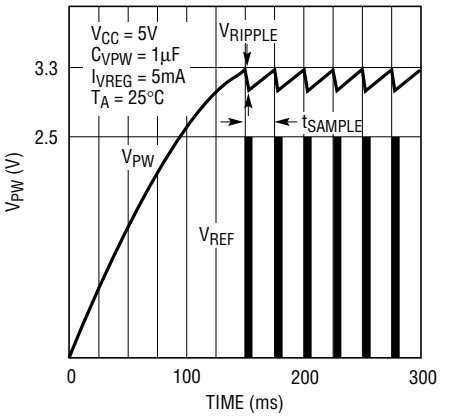
Note 5: Load on CMPOUT pulls current from V_{REG} when CMPOUT is high.

Note 6: Value derived from 1 second test.

Note 7: Zero-cross hysteresis is the minimum amount of signal amplitude above or below 0V differential to retrigger the zero-cross comparator.

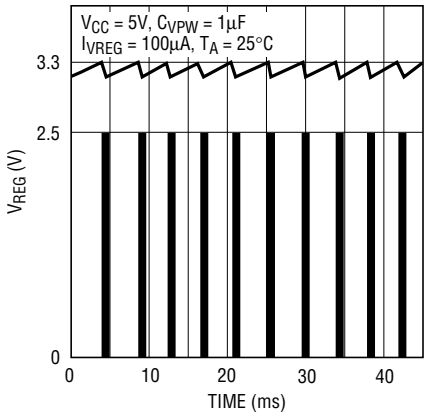
Note 8: Parameter not tested but guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS



NOTES: V_{RIPPLE} DEPENDS ON C_{VPW} AND I_{VPW} + I_{VREG}
t_{SAMPLE} DEPENDS ON I_{VPW} + I_{VREG}

Figure 1. V_{PW} Power-Up and V_{REG} Samples



NOTE: NONPERIODIC SAMPLES DUE TO DEPENDENCE ON V_{PW} > 3.3V AND THE POWER-LISTEN CYCLE SAMPLING

Figure 2. V_{REG} and V_{PW} with I_{VREG} = 100µA

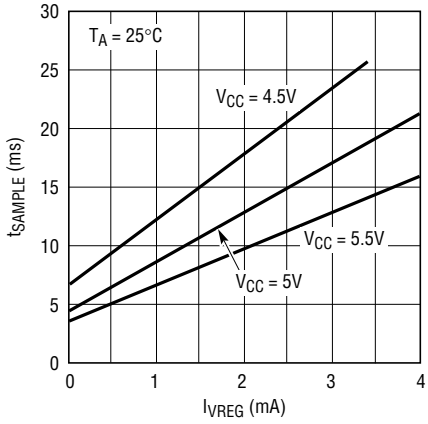


Figure 3. Average t_{SAMPLE} vs I_{VREG}

PIN FUNCTIONS

V_{CC} (Pin 1): Powered Side Power Supply.

$\overline{SHDN}$ (Pin 2): Active Low Chip Shutdown. A low signal causes the circuitry to power down. DATA logic output level will be reset to zero during power-down.

ZCNEG (Pin 3): Zero-Cross Comparator Negative Input.

ZCPOS (Pin 4): Zero-Cross Comparator Positive Input.

V_{PW} (Pin 11): Isolated Power Supply. Tied to an external storage capacitor.

CMPOUT (Pin 12): Isolated Latched Comparator Data. CMPOUT is active when V_{REG} is on. The CMPOUT output can be used on the isolated side for hysteresis (see applications). The output will contain the result of the previous comparison. When V_{REG} is low, the CMPOUT pin is Hi-Z.

V_{REG} (Pin 13): Isolated 2.5V Regulated Output. Pulsed on for 100µs with a maximum load current of 5mA. V_{REG} also supplies power to the CMPOUT output (Pin 12).

ISOGND (Pin 14): Isolated Side Power Ground.

V4 (Pin 15): Comparator Negative Input. The comparator inputs are summed together with the comparison output equal to (V1 + V2)/2 > (V3 + V4)/2 or equivalently (V1 – V3) > (V4 – V2).

V3 (Pin 16): Comparator Negative Input.

V2 (Pin 17): Comparator Positive Input.

V1 (Pin 18): Comparator Positive Input.

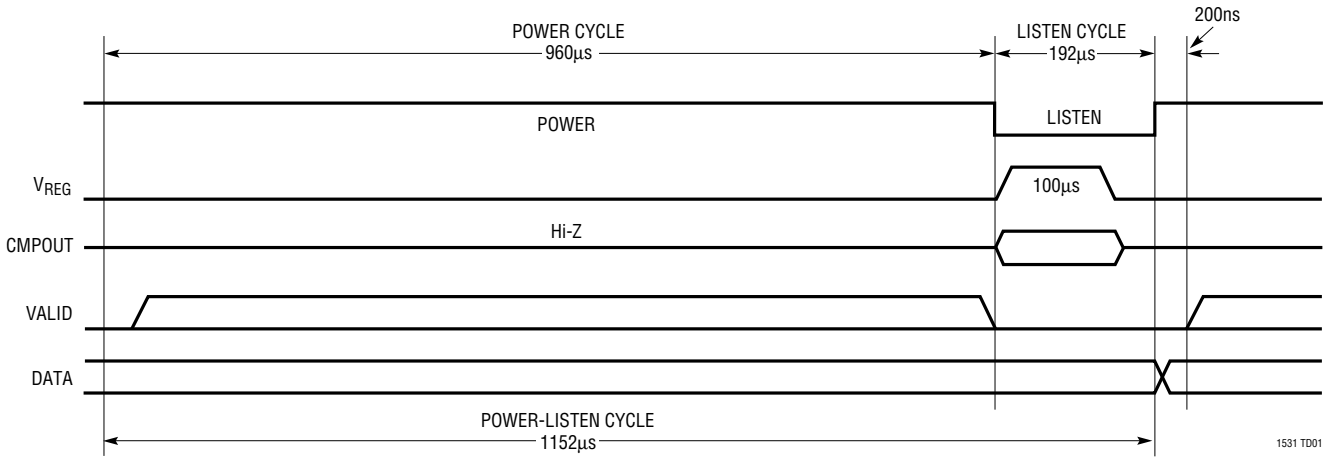
VALID (Pin 25): Pulsed Output. Indicates when valid data was received from the comparator. May be used to clock DATA to external circuitry.

DATA (Pin 26): Latched Comparator Result. DATA holds the value of the last valid comparison result. DATA changes only when a valid comparison was received from the isolated side.

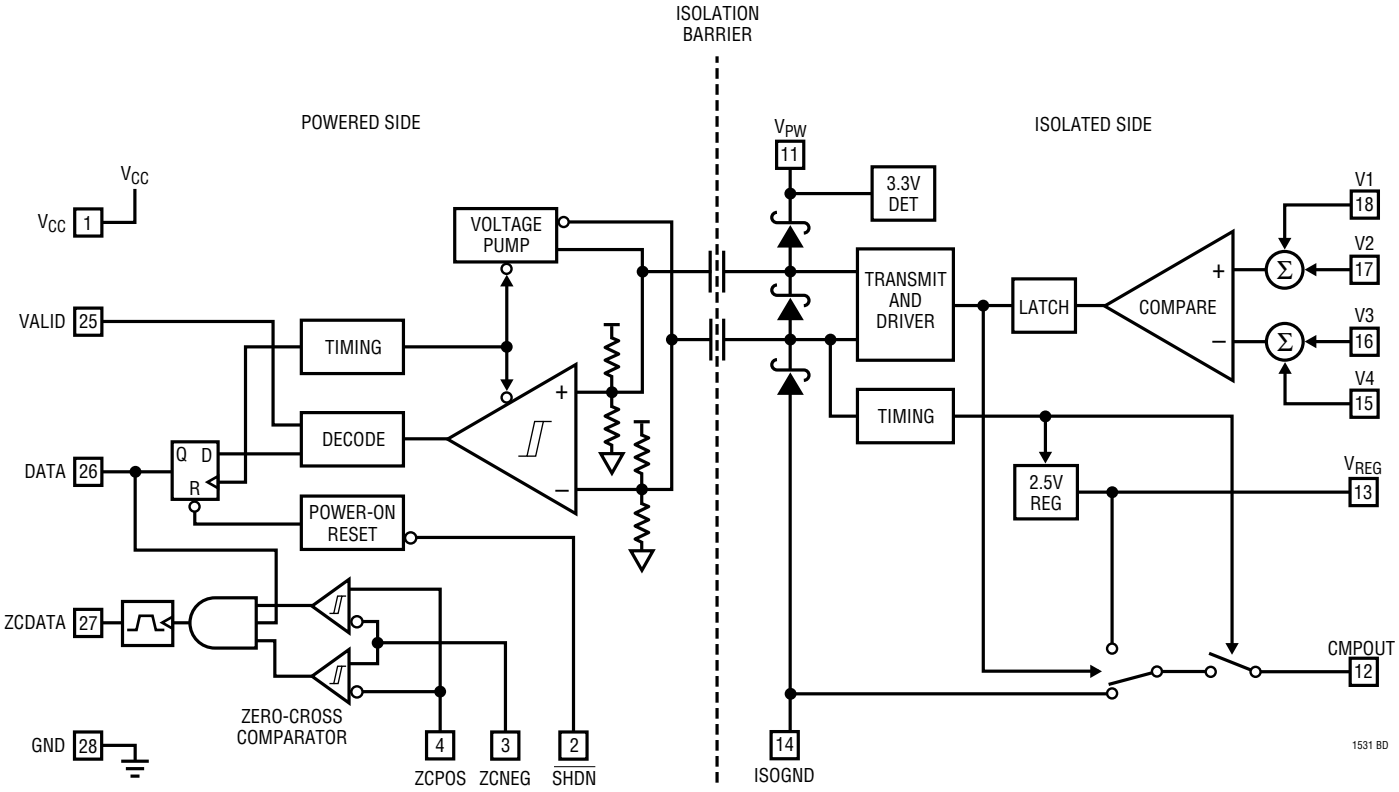
ZCDATA (Pin 27): A 24µs to 30µs Pulsed Output. The pulse occurs when the DATA output is high and the zero-cross comparator inputs (ZCPLS-ZCNEG) cross zero volts differential. Typically the zero-cross input signal is an RC phase shifted AC sine wave. This output is a TTL level pulse that can be used for firing an external triac.

GND (Pin 28): Power Supply Low Impedance Ground Connection.

TIMING DIAGRAM



BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1531 is an isolated self-powered dual differential comparator. It contains a switched-capacitor comparator that is self-powered through a capacitive isolation barrier. The capacitive isolation barrier provides $3000V_{RMS}$ of isolation. The isolated comparator duty cycles between storing power and performing comparisons. During the power delivery cycle, the nonisolated powered side delivers power through the internal isolation capacitors and rectifier onto an external storage capacitor. Periodically the isolated comparator makes a comparison if sufficient voltage has been stored on the external supply capacitor. See Timing and Block Diagrams.

During a comparison, the isolated side uses the energy stored on the external capacitor to deliver a regulated 2.5V power source for 100µs followed by a switched capacitor comparison. The result is transmitted back to the nonisolated powered side and latched, providing a logic level DATA output. A comparison will occur during the listen cycle if sufficient voltage (3.3V) has been stored on the external capacitor. New DATA is latched only if a comparison was actually done. A zero-crossing trigger pulse output, ZCDATA, for firing a triac is available to trigger a triac when the latched DATA output is high. A VALID data output pulse is provided after each power-listen cycle in which a comparison was done to indicate that DATA has been updated. The VALID data output can be used to clock external circuitry when a new comparator DATA value occurs.

Power-Listen Cycle

The LTC1531 comparator powered side toggles between delivering power to the isolated side and listening for a comparison result (see Timing Diagram). During the power cycle, AC power is delivered through the isolation capacitors to the isolated side. During the listen cycle, the powered side receives pulses from the isolated side and determines if a valid comparison occurred.

APPLICATIONS INFORMATION

V_{PW}, External Storage Capacitor and Sample Rate

The isolated side of the LTC1531 requires an external capacitor connected to V_{PW} whose value must be large enough to sustain less than a 300mV drop for 100µs with the given internal + external V_{REG} load current. Power is delivered to this external capacitor through the internal isolation capacitors and rectifiers during the power cycle. When this voltage reaches approximately 3.3V, the compare circuitry is enabled and a comparison will occur during the next listen cycle. This capacitive coupled isolated power source can be modeled as an equivalent 5V to 6.5V source with a 100kΩ source impedance. This pin will tend to self-regulate at 3.3V with a ripple determined by the discharge current supplied during the 100µs V_{REG} output pulse and the external capacitor value. The value of the capacitor affects the initial start-up time and the ripple voltage on V_{PW}, but it does not influence the sample rate of the comparator. Any excessive external DC loading on V_{PW} may prevent the capacitor voltage from reaching the required 3.3V enable voltage. Some continuous micropower loading on V_{PW} can be tolerated based on the 100k, 5.5V model of the power source (see Typical Applications for examples). The quiescent current of the isolated side is around 2µA to 3µA and the active internal load current is approximately 1mA.

The comparator sample rate depends on the charging rate through the isolated capacitors and the external + internal load current . The power-listen cycles at 700Hz to 900Hz, however, a comparison will only occur when V_{PW} exceeds the 3.3V enable voltage. Typical sample rate for light loading is 200Hz to 300Hz. The actual sampling is not uniform, but occurs during the listen period of the power cycle and when $V_{PW} \geq 3.3V$. Typical sample rates for various supply and load conditions are plotted in Figure 3 in Typical Performance Characteristics section. For maximum power transfer and maximum sample rates, etch copper away from the area shown in Figure 4.

Isolated Comparator Inputs and CMPOUT

The LTC1531 isolated switched-capacitor comparator has four inputs that allow various differential input sampling modes. All the comparator inputs sample simultaneously during the comparator autozero cycle, then switch to summing them together providing a dual differential comparison. The comparison performs:

$$(V1 + V2)/2 > (V3 + V4)/2$$

By rearranging the equation, for example, a dual differential comparison is performed:

$$(V1 - V4) > (V3 - V2) \text{ or } (V1 - V3) > (V4 - V2)$$

The switched-capacitor input samples at one time instance and has a rail-to-rail input and common mode voltage range of V_{PW}-ISOGND. The summing nature of the inputs allows midsupply referencing, for example, by connecting V3 to V_{REG} and V4 to ISOGND which sums together to provide $V_{REG}/2$ for the negative comparator input, as in the Isolated Switch application.

Charge injection occurs at the switched-capacitor comparator inputs. The amount depends on how the comparator is used. Minimum injection occurs with V1 = V2 and V3 = V4. A worst case would be with V1 = 3.3V, V2 = 0V, V3 = 3.3V, V4 = 0V, where the charge injection would be 7pC. Since the comparator is turned on only for the last 10µs of the 100µs V_{REG} period, the charge injection would occur at about the 90µs point.

The CMPOUT signal is typically used to provide hysteresis, as in the Isolated Temperature Control application. CMPOUT is the latched result of the previous comparison and is active during the following V_{REG}-on period. CMPOUT is powered by V_{REG}, the internal 2.5V regulated output, and is in high impedance except during the 100µs V_{REG}-on time. When active, CMPOUT is switched low to ISOGND or high to V_{REG} depending on the stored result of the previous comparison. The stored CMPOUT data is reset on power-up and is not necessarily reset by the powered side $\overline{SHDN}$ pin except when shutdown results in V_{PW} drooping low enough to trigger a power-on reset on the isolated side.

APPLICATIONS INFORMATION

DATA, VALID, ZCDATA

During a power cycle, the VALID signal goes high if a valid comparison was made during the previous listen cycle. VALID goes low at the beginning of the next listen cycle. The low-to-high transition of VALID can be used to clock DATA into external circuitry. In order for a comparison to occur, sufficient power must be stored on the isolated side storage capacitor.

The DATA output holds the last received compare result. DATA is reset to zero on power-up and shutdown. The VALID output is held high for one power cycle following a correctly received compare result. The received DATA value from the isolated side contains redundancy to improve noise immunity.

The ZCDATA is a 25µs output pulse triggered by the zero-cross comparator. In order for a pulse to occur, the DATA output must be at logic 1 and the ZCPOS-ZCNEG zero-cross comparator input crosses 0V after the input has exceeded the ±200mV to 800mV of hysteresis. The zero-cross comparator output is typically used to trigger a triac from a 60Hz RC phase shifted AC line signal.

The zero-cross comparator inputs, ZCPOS and ZCNEG, allow signal swings to exceed the supply rails. However, the ZCPOS and ZCNEG inputs contain ESD diode protection devices which will clamp input signals that go below GND. The current into the diode should be limited to less than 5mA. The Isolated Temperature Control shows an example phase shift network with attenuation that satisfies these conditons. In this example, with R1 >> R2, the phase shift θ is set by:

$$R2 \bullet C1 \cong \tan(\theta)/2\pi 60Hz$$

and the attenuation ≅ R2/R1. In this example, R1 = 1M, R2 = 47k and C1 = 0.01µF, provides a $7V_{PEAK}$ input signal referenced to the 5V V_{CC}, with 10° of phase lag. The positive input voltage should not exceed the 12V maximum rating or the 5mA input current to the ESD diode clamp.

Isolation dV/dt

The maximum continuous dV/dt across the isolation barrier that will still allow the isolated comparator to operate is 50V/µs. Rates of dV/dt greater than this cause the isolated side to not detect when its power cycle has stopped and a comparison should begin.

PC Board Layout

The PC board layout should not have copper near the lead frame isolation capacitors. The copper reduces the power coupling and power delivery to the isolated side.

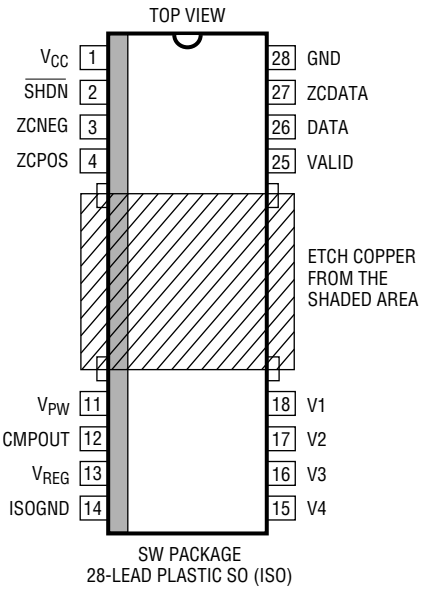
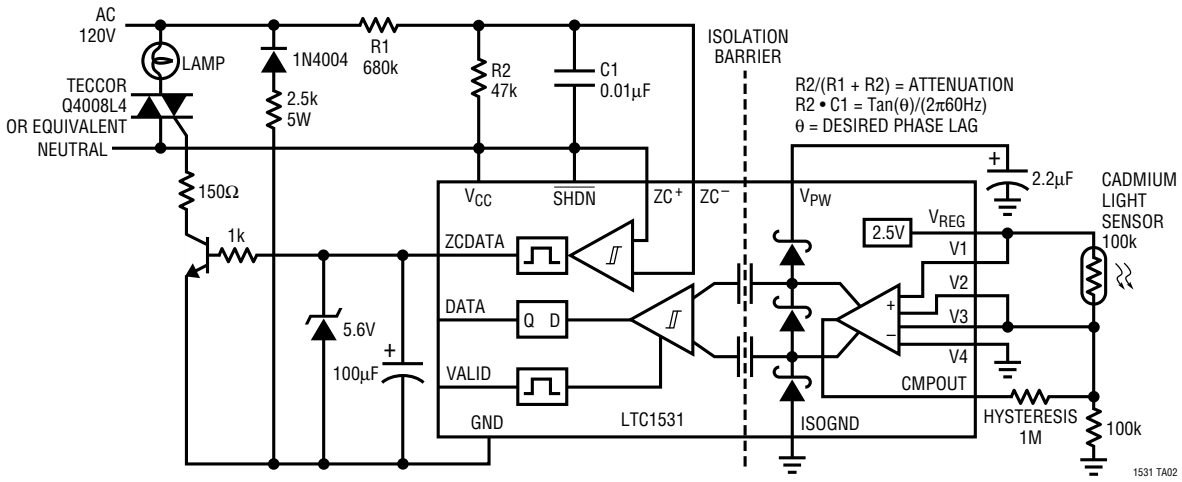


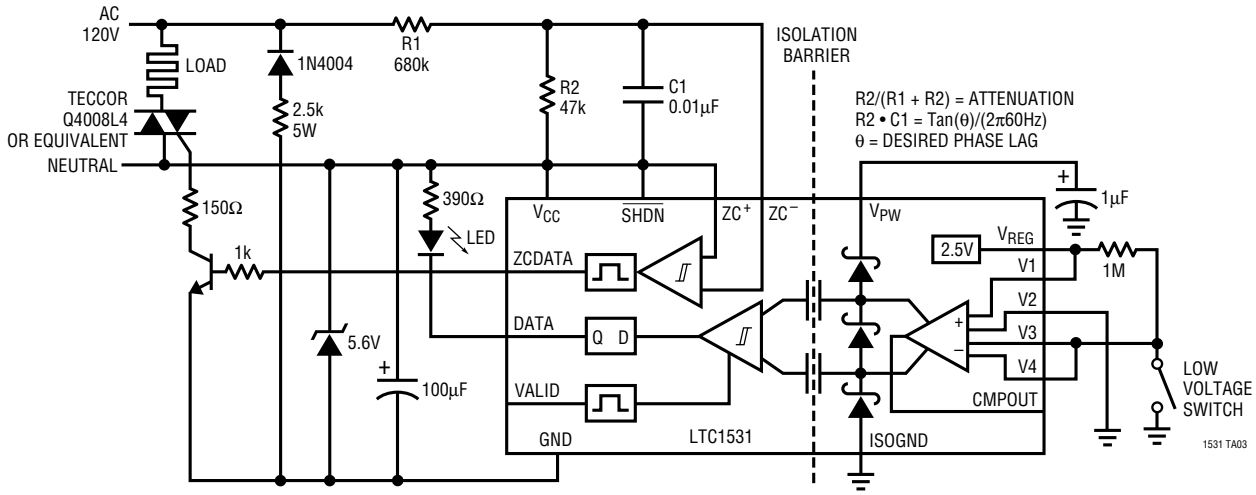
Figure 4. PC Board Layout Consideration

TYPICAL APPLICATIONS

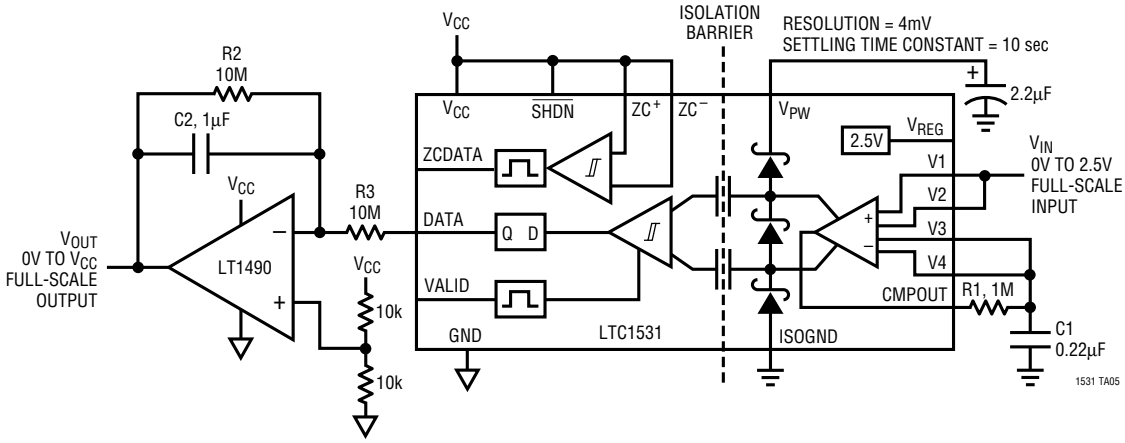
Remote Light-Controlled Switch



Isolated Switch Control

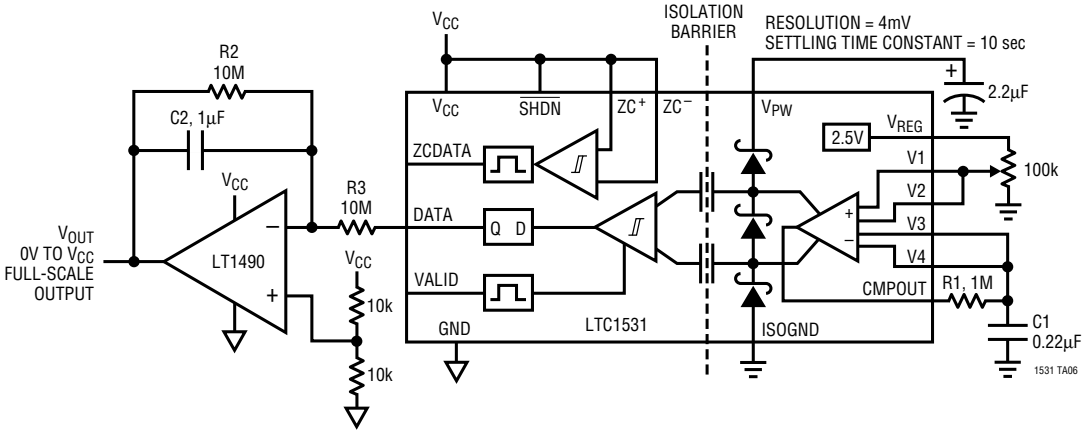


Isolated Voltage Sense

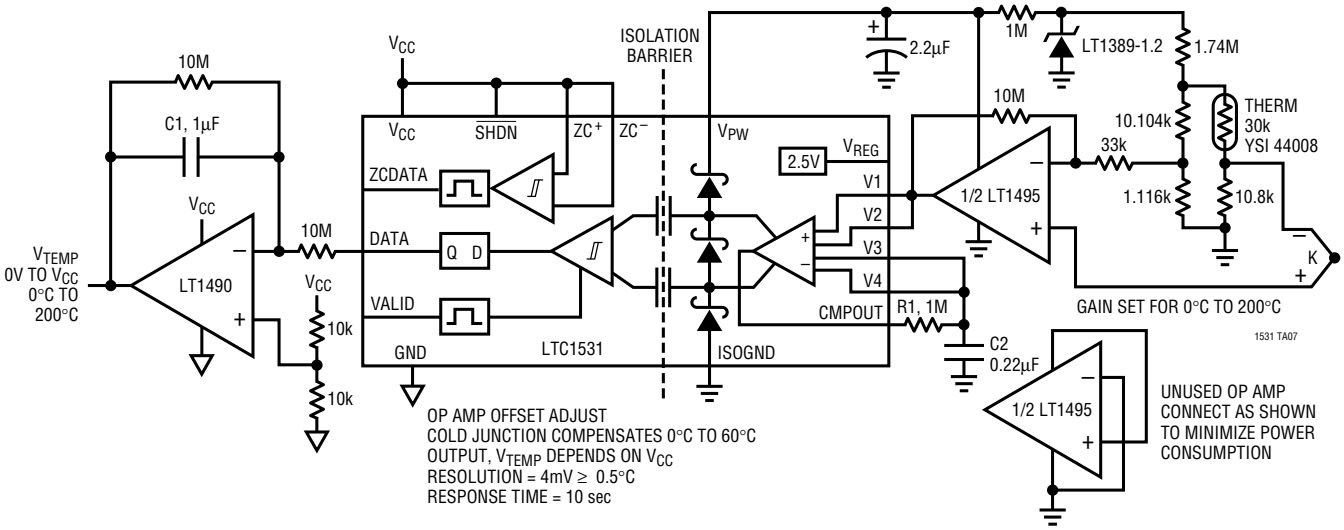


TYPICAL APPLICATIONS

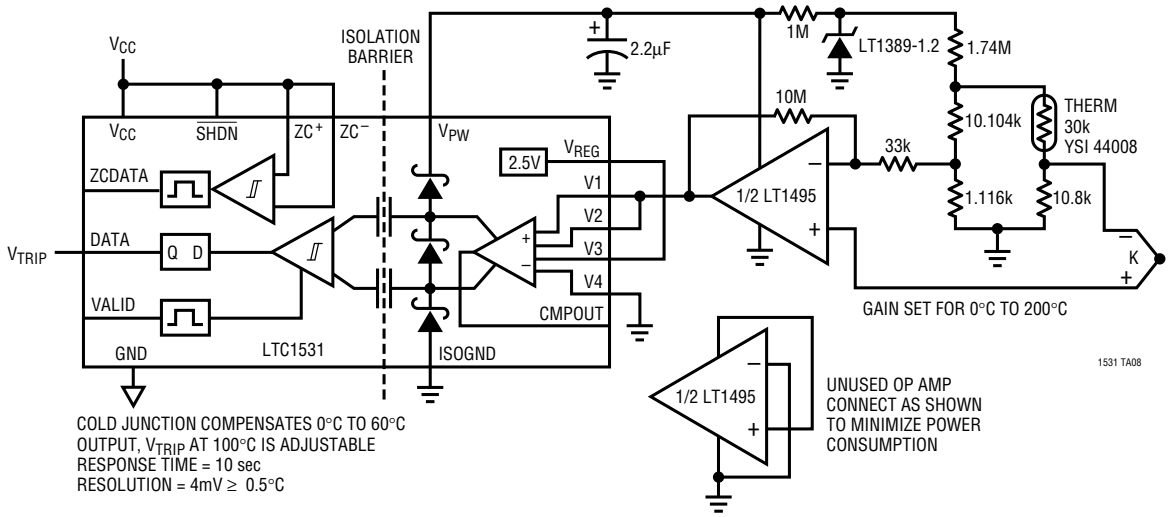
Isolated Potentiometer Transducer Sense



Isolated Thermocouple Voltage

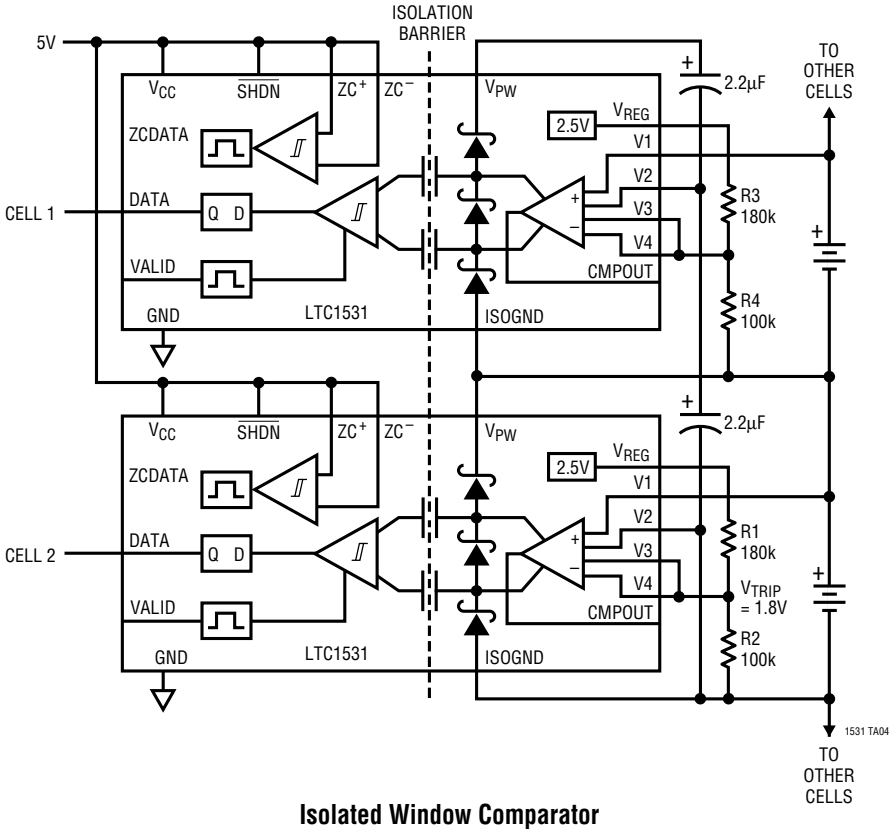


Over Temperature Detect

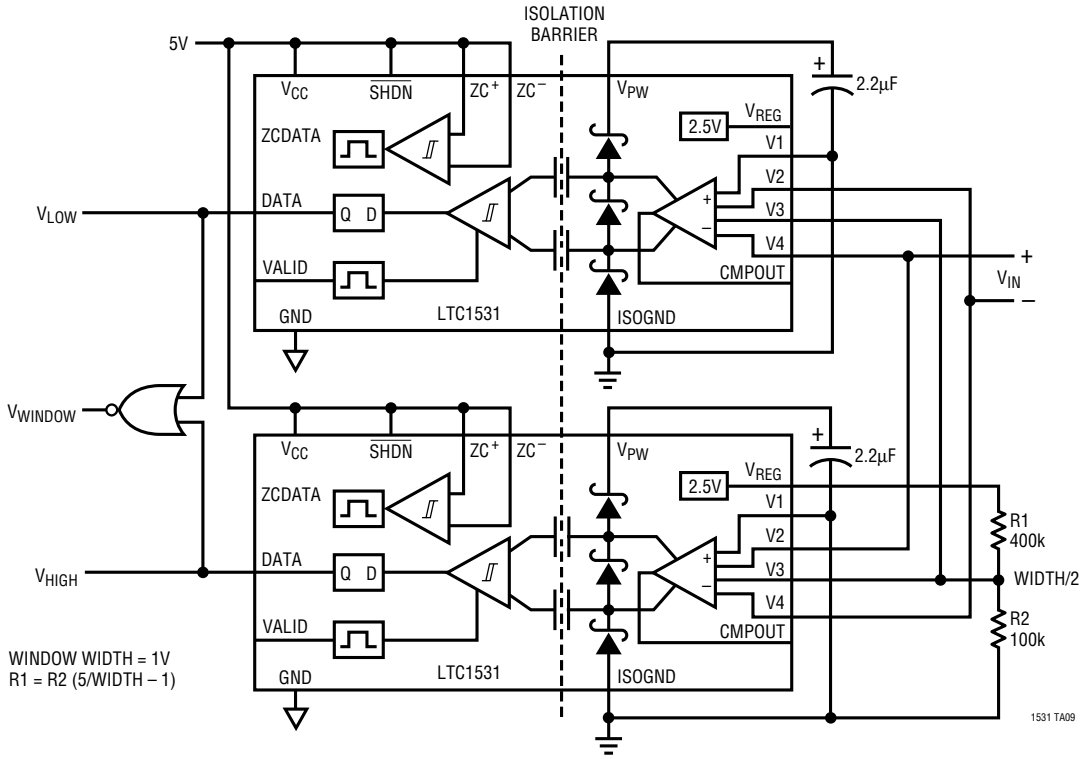


TYPICAL APPLICATIONS

Isolated Battery Cell Monitor



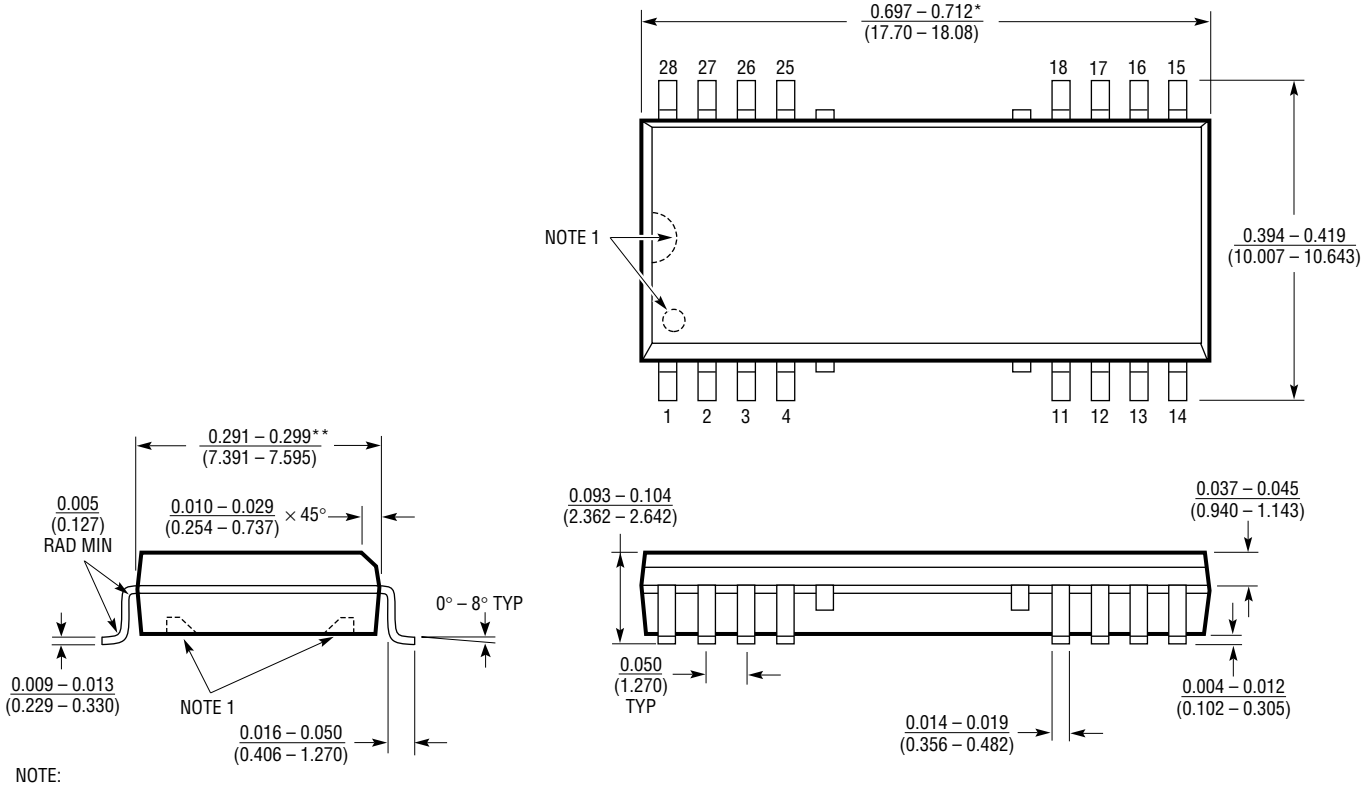
Isolated Window Comparator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
28-Lead Plastic Small Outline Isolation Barrier (Wide 0.300)
(LTC DWG # 05-08-1690)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

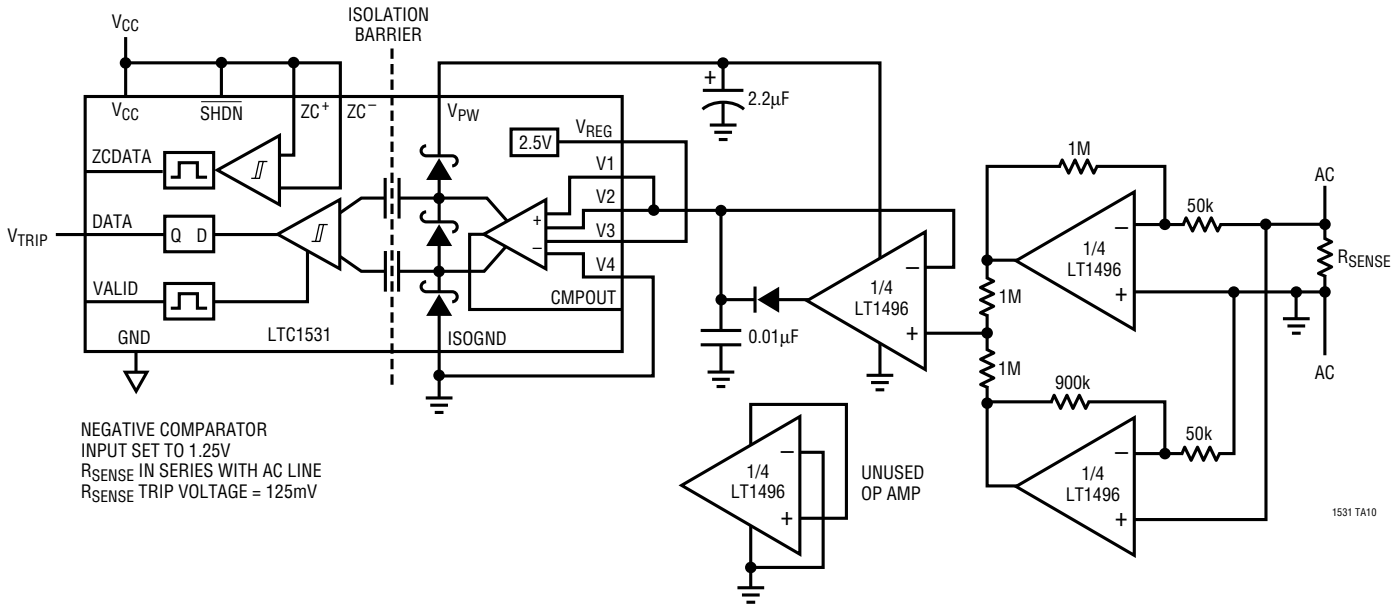
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW28 (ISO) 0695

TYPICAL APPLICATION

AC Line Overcurrent Detect



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1177	Isolated MOSFET Driver	No Secondary Power Supply, 2500V_{RMS} Isolation
LT1389	Nanopower Reference	800nA, 0.05% Accuracy, 10ppm/°C Max Drift
LTC1440/LTC1441 LTC1442	Ultralow Power Single/Dual Comparator with Reference	2.1µA Typ, 2V to 11V Supply, Adjustable Hysteresis
LT1495/LT1496	1.5µA Max, Dual/Quad Precision Rail-to-Rail Input and Output Op Amps	Low Offset 375µV_{MAX}, 2.2V to 36V Supply
LTC1540	Nanopower Comparator with Reference	0.3µA Typ, Adjustable Hysteresis, 2V to 11V Supply

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