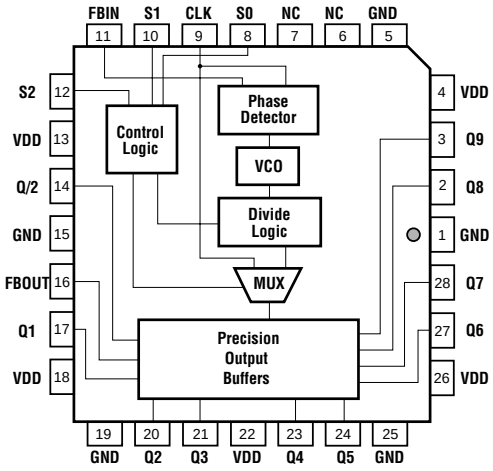
GA1086

11-Output Clock Buffer

Figure 1. Block Diagram



TriQuint's GA1086 operates from 30 MHz to 67 MHz. This TTL-level clock buffer chip supports the tight timing requirements of high-performance microprocessors, with near zero input-to-output delay and very low pin-to-pin skew. The device offers 10 usable outputs synchronized in phase and frequency to a periodic clock input signal. One of the ten outputs is a one-half clock output (CLK ÷ 2). With split termination, the GA1086 can be used to drive up to nineteen 15 pF loads, as shown in Figure 10.

The tight control over phase and frequency of the output clocks is achieved with a 400 MHz internal Phase-Locked Loop (PLL). By feeding back one of the output clocks to FBIN, the on-chip PLL continuously maintains synchronization between the input clock (CLK) and all ten outputs. Any drift or gradual variation in the system clock is matched and tracked at the ten outputs. The GA1086 output buffers are symmetric, each sourcing and sinking up to 30 mA of drive current. For diagnostic purposes, the device has a test mode which is used to test the device and associated logic by single-stepping through the control logic.

The GA1086 is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL compatibility. The output frequency makes this device ideal for clock generation and distribution in a wide range of high-performance microprocessor-based systems. Many other CISC- and RISC-based systems will also benefit from its tight control of skew and delay.

Features

- *Operates from 30 MHz to 67MHz*
- *Pin-to-pin output skew of 250 ps (max)*
- *Period-to-period jitter: 75 ps (typ)*
- *Near-zero propagation delay: –350 ps ± 500 ps or –350 ps ± 1000 ps*
- *10 symmetric, TTL-compatible outputs with 30 mA drive and rise and fall times of 1.4 ns(max)*
- *28-pin J-lead surface-mount package*
- *Special test mode*
- *Meets or exceeds Pentium™ processor timing requirements*
- *Typical applications include low-skew clock distribution for:*
  - *RISC- or CISC-based systems*
  - *Multi-processor systems*
  - *High-speed backplanes*

SYSTEM TIMING PRODUCTS

Functional Description

The GA1086 generates 10 outputs (Q1 – Q9 and FBOUT) which have the same frequency and zero phase delay relative to the reference clock input. In addition, there is one output (Q/2) that has $^1/_2$ the frequency of the reference clock. The GA1086 maintains frequency and zero phase delay using a Phase Detector to compare the output clock with the reference clock input. Phase deviations between the output clock and reference clock are continuously corrected by the PLL. Figure 1 shows a block diagram of the PLL, which consists of a Phase Detector, Voltage Controlled Oscillator (VCO), Divide Logic, Mux and Control Logic.

The Phase Detector monitors the phase difference between FBIN which is connected to FBOUT, and the reference clock (CLK). The Phase Detector adjusts the VCO such that FBIN aligns with CLK. The VCO has an operating range of 360 MHz to 402 MHz. The output clocks (Qn, FBOUT, and Q/2) are generated by dividing the VCO output.

The desired operating frequency determines the proper divide mode. There are 4 divide modes; ÷12, ÷10, ÷8 and ÷6. In each mode, the GA1086 operates across the frequency range listed in the Divide Mode Selection Table. The operating frequency is equivalent to the VCO frequency divided by the mode number.

Table 1 shows the input clock frequency (CLK), output clock frequency (Qn), $^1/_2$ output clock frequency (Q/2), control bit settings, divide mode and VCO range. FBOUT is fed back to FBIN and has the same frequency as the Qn outputs.

The GA1086 has a test mode that allows for single stepping of the clock input for testing purposes. With S2 HIGH, S1 LOW and S0 HIGH, the signal at the CLK input goes directly to the outputs, bypassing the PLL circuitry.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the GA1086 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

The GA1086-MC500 and GA1086-MC1000 are identical except for the propagation delay specification (see AC Characteristics table).

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. As long as the signal at FBIN is derived directly from the FBOUT pin and maintains its frequency, additional delays can be accommodated. The internal phase-locked loop will adjust the output clocks on the GA1086 to ensure zero phase delay between the FBIN and CLK signals.

Note: the signal at FBIN must be continuous, i.e. not a gated or conditional signal.

Table 1. Divide Mode Selection Table

CLK	*Qn*	*Q/2*	*Control S2*	*S1*	*S0*	*Divide Mode*
30 – 33 MHz	30 – 33 MHz	15 – 16.5 MHz	1	1	1	÷12
36 – 40 MHz	36 – 40 MHz	18 – 20 MHz	1	1	0	÷10
45 – 50 MHz	45 – 50 MHz	22.5 – 25 MHz	1	0	0	÷8
60 – 67 MHz	60 – 67 MHz	30 – 33.5 MHz	0	1	1	÷6
TSTCLK	TSTCLK	TSTCLK/2	1	0	1	—

Power-Up/Reset Synchronization

The GA1086 utilizes on-chip phase-locked loop (PLL) technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLK) is reset, the phase-locked loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required for synchronization is 500 ms.

Typical Applications

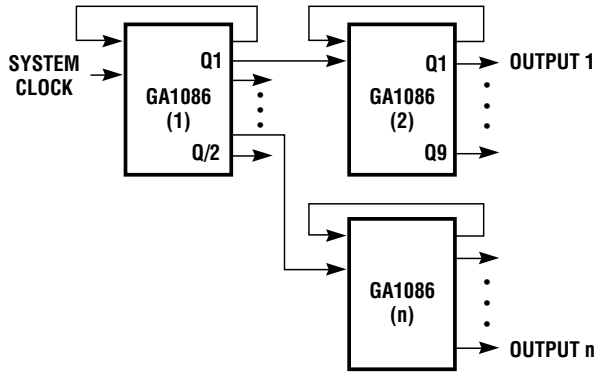
The GA1086 is designed to satisfy a wide range of system clocking requirements. Following are two of the most common clocking bottlenecks which can be solved using the GA1086.

1) Low-Skew Clock Distribution / Clock Trees

The most basic bottleneck to clocking high-performance systems is generating multiple copies of a system clock, while maintaining low skew throughout the system.

- *The GA1086 guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all outputs. In Figure 2, the worst-case skew from Output 1 to Output n, with reference to the system clock, is obtained by summing the various skews. The skew between the outputs of the GA1086 (1) which drive the GA1086 (2) and the GA1086 (n) is summed with the propagation delay of the GA1086 (2 or n), the skew between the outputs of the GA1086 (2), and the skew between the outputs of the GA1086 (n). This results in a total skew of 1.75 ns (250 ps + 1000 ps + 250 ps + 250 ps).*

Figure 2. Low-Skew Clock Distribution

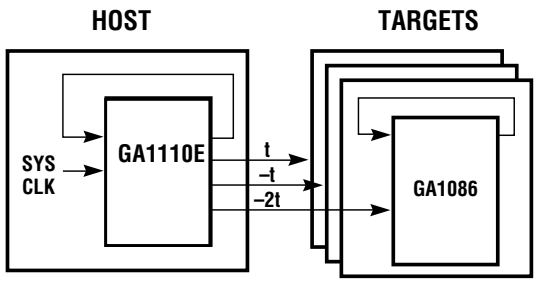


2) Board-to-Board Synchronization

Many computing systems today consist of multiple boards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

- *The edge placement feature of TriQuint's configurable custom clock generator (GA1110E) operating at 33 MHz, coupled with the tightly controlled input/output delay of the GA1086, ensures all boards in the system are running synchronously.*

Figure 3. Board-to-Board Synchronization



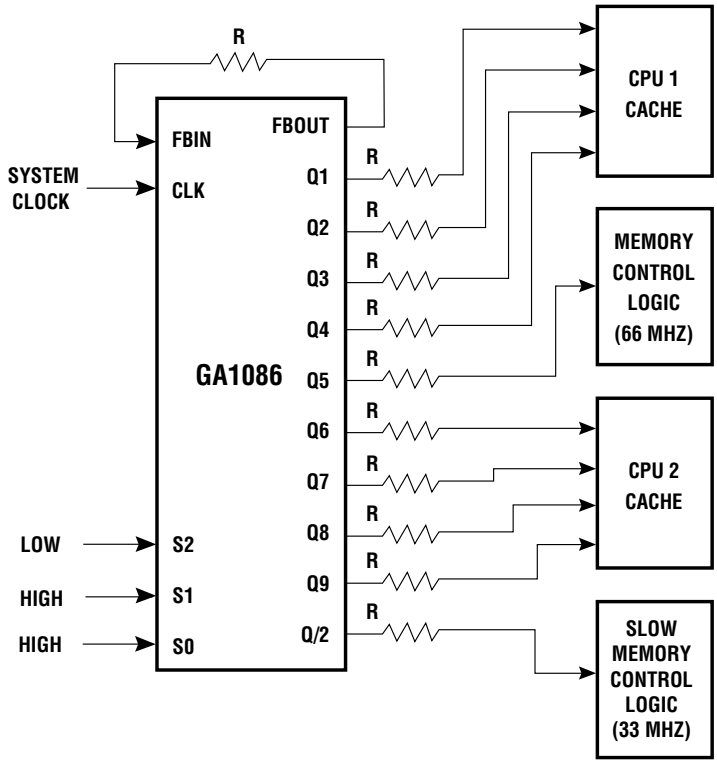
SYSTEM TIMING PRODUCTS

Multi-Processor Systems

The GA1086 can be effectively used to distribute clocks in RISC- or CISC-processor-based systems. Its 10 outputs support both single- and multi-processor systems. Following are three representative configurations which show how the 10 outputs can be used to synchronize the operation of CPU cache and memory banks operating at different speeds.

Figure 4 depicts a 2-CPU system in which the processors and associated peripherals are operating at 66 MHz. Each of the nine outputs operating at 66 MHz are fully utilized to drive the appropriate CPU, cache, and memory control logic. The 33 MHz output is used to synchronize the operation of the slower memory bank to the rest of the system.

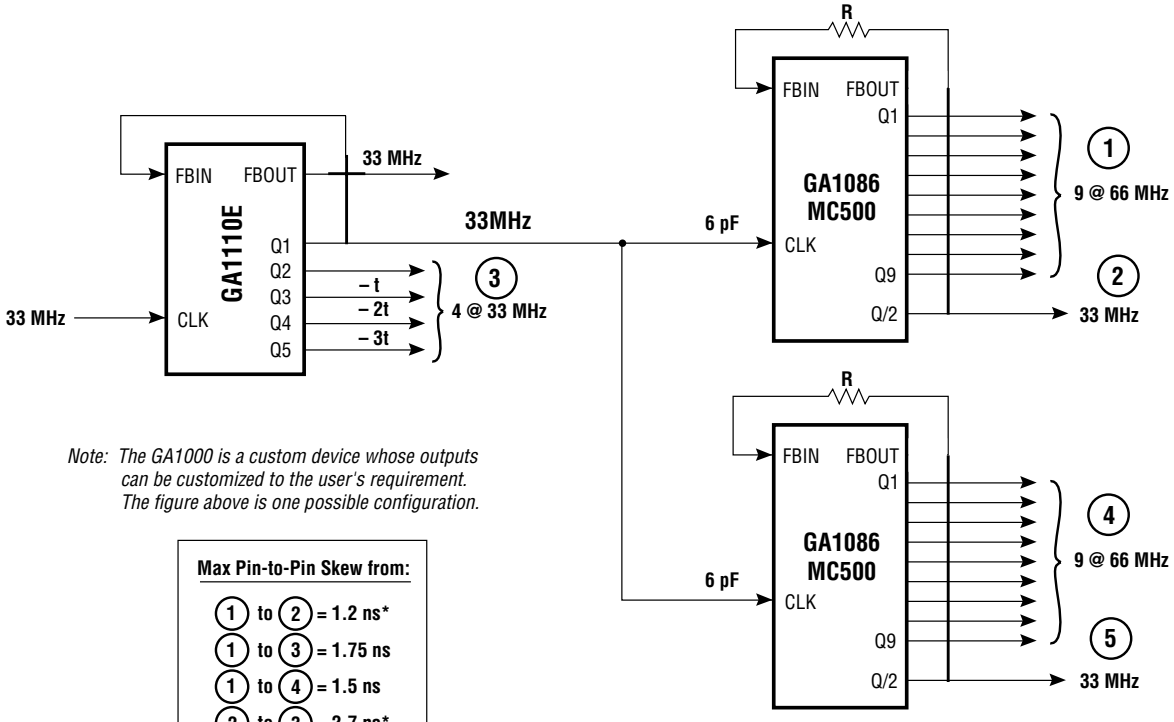
Figure 4. Clocking a Dual-CPU System



Multi-Processor Systems (cont.)

Figure 5 shows a 4-processor system with various 33 MHz memory banks synchronized to the 66 MHz CPUs. The GA1110E, a custom device whose six outputs can be individually configured, (see GA1110E data sheet), is used as the clock source for the GA1086 devices. This configuration gives the user 18 copies of the 66 MHz clock and 7 copies of the 33 MHz clock. By using the configurability of the GA1110E, the user can also specify and control the placement of the edges of the outputs of the GA1110E.

Figure 5. Generating Multiple Outputs



Note: The GA1000 is a custom device whose outputs can be customized to the user's requirement. The figure above is one possible configuration.

Max Pin-to-Pin Skew from:

1 to 2	= 1.2 ns*
1 to 3	= 1.75 ns
1 to 4	= 1.5 ns
2 to 3	= 2.7 ns*
2 to 5	= 3.2 ns*
3 to 4	= 1.75 ns
3 to 5	= 2.7 ns*
4 to 5	= 1.2 ns*

** Assumes maximum skew between Q9 and Q/2 is 1.2 ns. See AC specifications.*

SYSTEM TIMING PRODUCTS

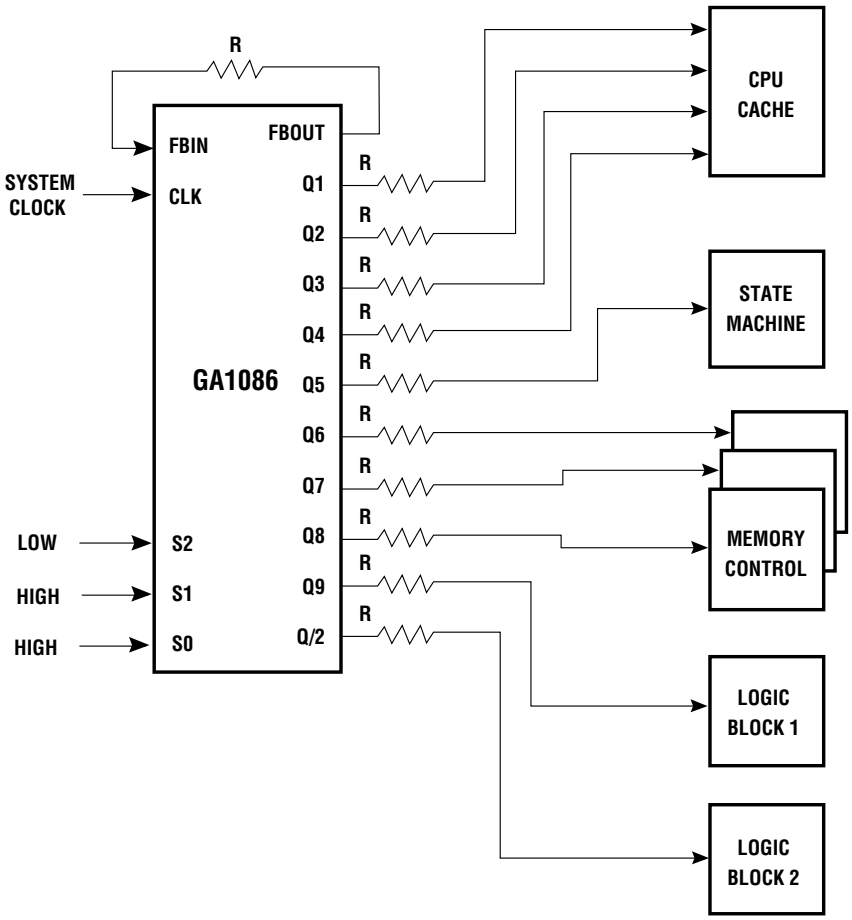
Single-Processor Systems

Figure 6 is an example of a single-CPU system. The nine 66MHz outputs of the GA1086 are used to drive the CPU and its related cache, the state machine, memory banks, and other general-purpose logic.

The table in Figure 5 also specifies the maximum pin-to-pin skew of various sets of outputs from the three clocking devices.

Please note that the GA1086s are series-terminated and that the feedback trace lengths for the two devices should be equal.

Figure 6. Clocking a Single-CPU System

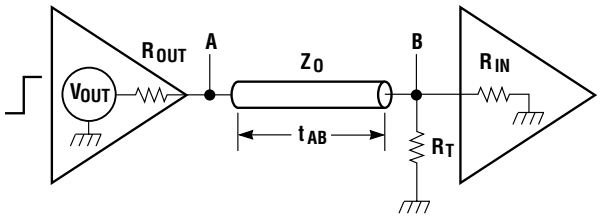


Parallel Termination of Outputs

The GA1086 can be terminated either in parallel or in series. If power dissipation is not of primary concern, then parallel termination can be the most effective mode of termination for the GA1086. An example of this termination is shown in Figure 7, along with the waveforms at an output pin and at the load. Note that the Thevenin equivalent using two resistors and +5 V supply can replace the 65 ohms to 1.5 V.

Unused outputs must be terminated.

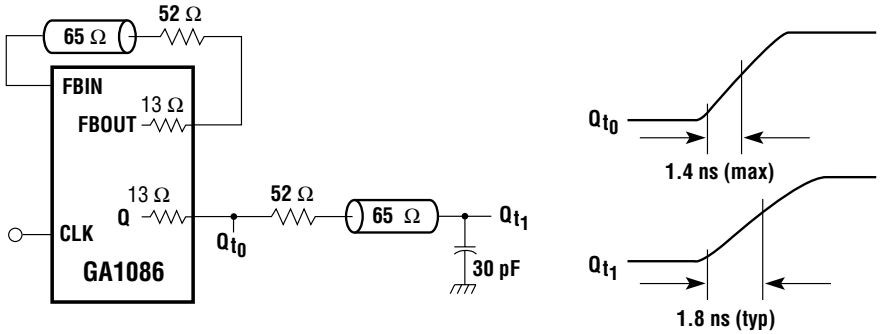
Figure 7. Parallel Termination



Series Termination of Outputs

The alternative to parallel termination is series termination. For applications where overshoots and undershoots of the clock signal are a concern, it is best to use balanced termination as shown in Figure 8. This could, however, slow the rise time of the pulses arriving at the destination.

Figure 8. Balanced Termination



If rise times are critical and if overshoots and undershoots can be tolerated, then unbalanced termination may be used. Reflections due to unbalanced termination can cause ringing at the load. The transmission line lengths, therefore, must be long enough to cause the ringing to occur only after the waveform has completely switched to either the LOW or the HIGH state, (the round trip). The propagation time of the output signals should be greater than the switching time for LOW to HIGH or HIGH to LOW.

To double the number of loads (devices) driven by the GA1086, split termination may be used. Examples of three types of series termination and the resulting waveforms, measured between 0.8 V and 2.0 V, are shown in Figures 9 and 10 for one of the outputs. Unused outputs must be terminated.

Figure 9. Unbalanced Termination

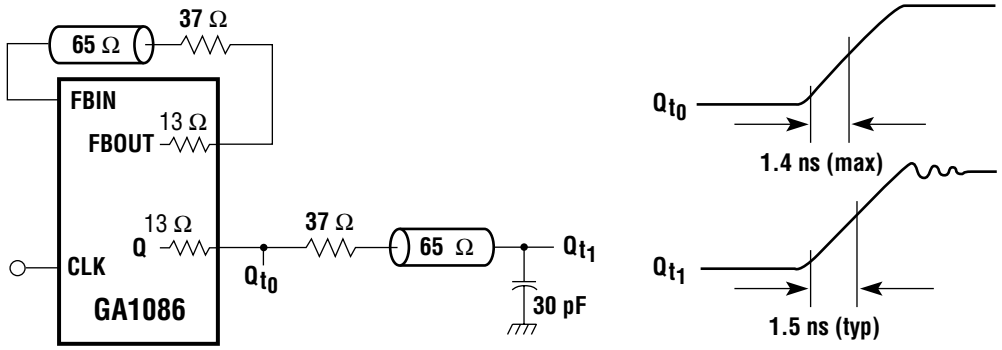
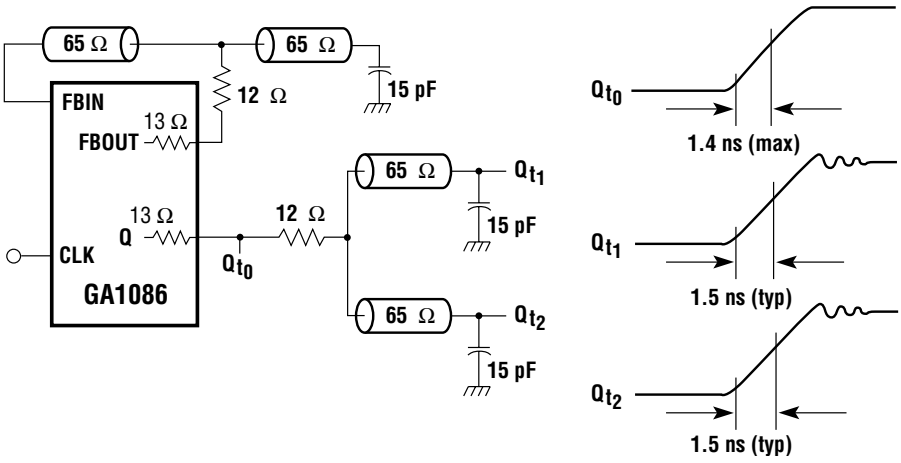


Figure 10. Split Unbalanced Termination



Note: Rise time at Q_{t1} is measured between 0.8 V and 2.0 V.

Absolute Maximum Ratings

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +100 °C
Supply voltage to ground potential	–0.5 V to +7.0 V
DC input voltage	–0.5 V to +(V_{DD} + 0.5)
DC input current	–30 mA to +5 mA

Caution: *Damage to the device may occur if an output is shorted to ground or V_{DD}.*

DC Characteristics

(Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C) [1]

Symbol	*Description*	*Test Conditions*	*Limits* [2] *Min*	*Typ*	*Max*	*Unit*
V_{OH}	Output HIGH voltage	V_{DD} = Min I_{OH}= –30 mA V_{IN}= V_{IH} or V_{IL}	2.4	3.6		V
V_{OL}	Output LOW voltage	V_{DD} = Min I_{OL} = 30 mA V_{IN}= V_{IH} or V_{IL}		0.2	0.5	V
V_{IH}[3]	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}[3]	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I_{IL}	Input LOW current	V_{DD} = Max V_{IN} = 0.40 V		–166	–400	µA
I_{IH}	Input HIGH current	V_{DD} = Max V_{IN} = 2.7 V		0	25	µA
I_I	Input HIGH current	V_{DD} = Max V_{IN} = 5.5 V		2	1000	µA
I_{DD}[4]	Power supply current	V_{DD} = Max			115	160 mA
V_I	Input clamp voltage	V_{DD} = Min I_{IN} = –18 mA		–0.62	–1.2	V

Capacitance [1,5]

Symbol	*Description*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
C_{IN}		Input capacitance	V_{IN} = 2.0 V at f = 1 MHz		6	pF

Notes: 1. These values apply to both the GA1086-MC500 and GA1086-MC1000.
2. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. I_{DD} is measured with outputs LOW and unloaded.
5. These parameters are not 100% tested, but are periodically sampled.

AC Specifications

(Supply voltage: +5 V ± 5%, Ambient temp: 0°C to +70°C)

	Input Clocks	*Min*	*Typ*	*Max*	*Unit*
F_{IN}	CLK frequency	30	—	67	MHz
t_{CP}	CLK period	14.9	—	33	ns
t_{CPW}	CLK pulse width	3.0	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)	—	—	2.0	ns

	Output Clocks	*Min*	*Typ*	*Max*	*Unit*
t_{OR}	Output rise time (0.8 V – 2.0 V)	0.15	—	1.4	ns
t_{OF}	Output fall time (0.8 V – 2.0 V)	0.15	—	1.4	ns
t_{PD1} [1]	CLK Î to FBIN Î (MC500)	–850	–350	+150	ps
t_{PD2} [1,2]	CLK Î to FBIN Î (MC1000)	–1350	–350	+650	ps
t_{SKEW1} [2,3]	Q1–Q9 and FBOUT (0.8V)	–125	—	+125	ps
t_{SKEW1} [2,3]	Q1–Q9 and FBOUT (1.5V)	–125	—	+125	ps
t_{SKEW1} [2,3]	Q1–Q9 and FBOUT (2.0V)	–125	—	+125	ps
t_{SKEW2} [2,3]	Q/2 Output skew	—	0.6	1.2	ns
t_W [4]	Output window	—	100	250	ps
t_{CYC} [5]	Duty-cycle variation	—	1.0	—	ns
t_{SYNC} [6]	Synchronization time	—	200	500	µs
t_{JIT} [7]	Period-to-period jitter	—	75	—	ps

Figure 11. Switching Waveforms

Buffer Configuration (FBIN = FBOUT)

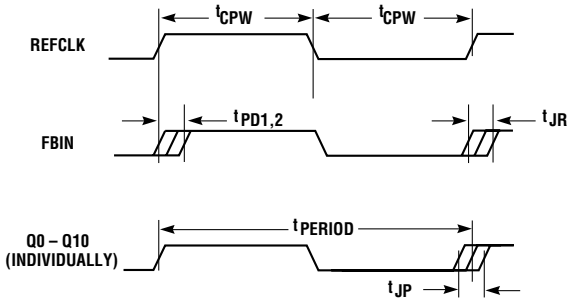
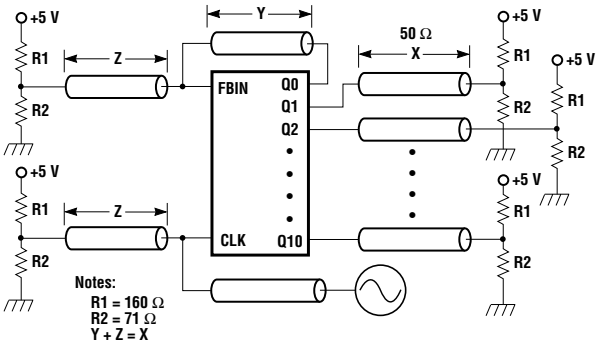


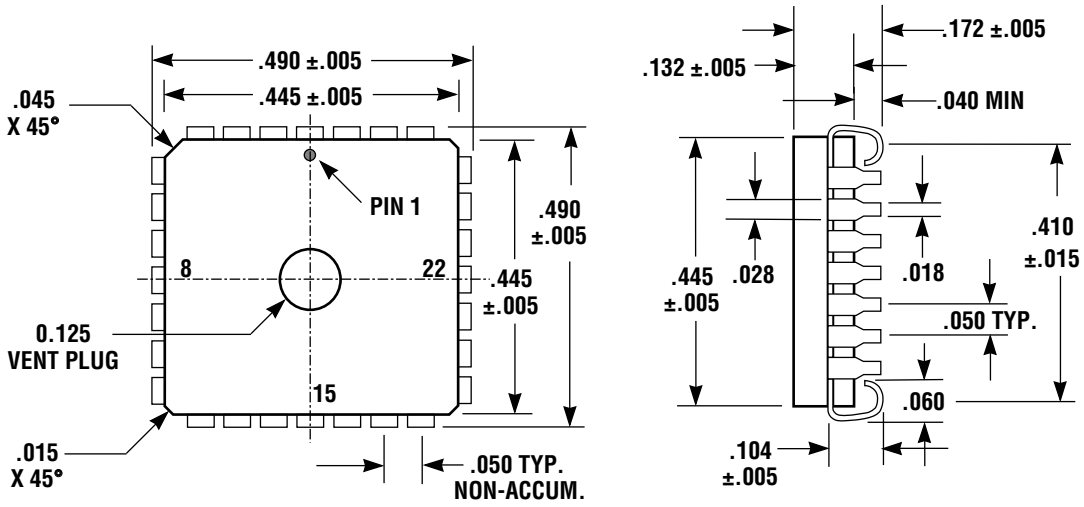
Figure 12. AC Test Circuit



Notes:
1. *The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.*
2. *t_{PD} and t_{SKEW} are tested with an input clock having a rise time of 0.5 ns (0.8 V to 2.0 V).*
3. *The output skew is measured from the middle of the output window, t_W. The maximum skew is guaranteed across all voltages and temperatures.*
4. *t_W specifies the width of the window in which outputs Q1–Q9 switch.*
5. *This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.*
6. *t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.*
7. *Jitter is specified as a peak-to-peak value.*

28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	*Pin Name*	*Description*	*I/O*
1	GND	Ground	–
2	Q8	Output Clock 8	O
3	Q9	Output Clock 9	O
4	VDD	+5 V	–
5	GND	Ground	–
6	N/C	No Connect	–
7	N/C	No Connect	–
8	S0	Select 0	I
9	CLK	Reference Clock	I
10	S1	Select 1	I
11	FBIN	Feedback In	I
12	S2	Select 2	I
13	VDD	+5 V	–
14	Q/2	Half-Clock Out	O

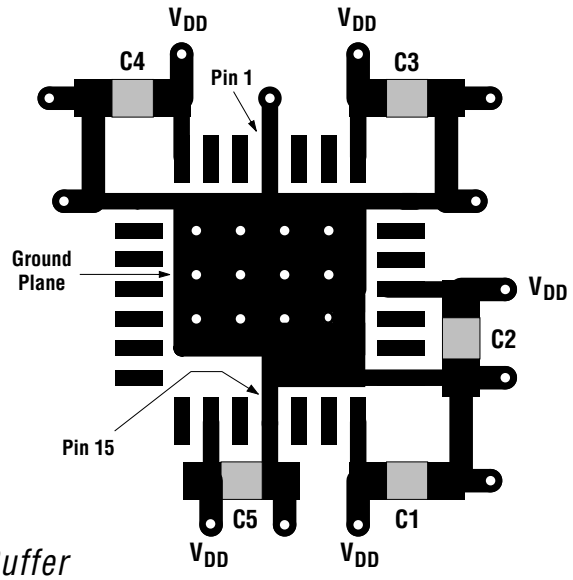
Pin #	*Pin Name*	*Description*	*I/O*
15	GND	Ground	–
16	FBOUT	Feedback Clock	O
17	Q1	Output Clock 1	O
18	VDD	+5 V	–
19	GND	Ground	–
20	Q2	Output Clock 2	O
21	Q3	Output Clock 3	O
22	VDD	+5 V	–
23	Q4	Output Clock 4	O
24	Q5	Output Clock 5	O
25	GND	Ground	–
26	VDD	+5 V	–
27	Q6	Output Clock 6	O
28	Q7	Output Clock 7	O

Layout Guidelines

Multiple ground and power pins on the GA1086 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 13 shows the recommended power layout for the GA1086. The bypass capacitors should be located on the same side of the board as the GA1086. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through-holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 13. Top Layer Layout of Power Pins
(Approx. 3.3x)



Ordering Information

To order, please specify as shown below:

GA1086-MC n...n *11-Output Clock Buffer*

Propagation delay skew:

500	–350 ps ± 500 ps
1000	–350 ps ± 1000 ps

Temperature range:
0 °C to 70 °C (Commercial)

Package: MQuad

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: sales@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

Email: applications@tqs.com

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