MH89625C

OPS/DID PCM SLIC

Preliminary Information

ISSUE 4 May 1995

Features

- Input impedance variants:
  - 600Ω
  - 200Ω + 680Ω // 0.1µF
  - 200Ω + 560Ω // 0.1µF
- Operates with a wide range of battery voltages
- Constant current battery feed with constant voltage fallback for long loop drive capabilities
- Overvoltage and short circuit protection
- Off-hook detection and LED indicator drive
- Dial pulse detection
- Ring trip filter with auto ring trip
- Ring relay driver plus three more uncommitted relay drivers
- Transformerless 2W to 4W conversion
- A/D and D/A conversion
- Conforms to A-Law PCM
- Analog and digital loopback
- Conforms to CCITT k.20 overvoltage surge requirements with external primary protection circuitry

Applications

- Off premise digital PBX line cards
- DID (Direct Inward Dial) line cards
- PABX, Key Systems, Central Office Equipment

Ordering Information

MH89625C	600Ω
MH89625C- 5	200Ω + 680Ω // 0.1µF
MH89625C- 6	200Ω + 560Ω // 0.1µF

40 Pin DIL Package

Description

The Mitel MH89625C SLIC (Subscriber Line Interface Circuit) provides a complete interface between an off-premise telephone line and a digital switching system. All BORSCHT functions of Battery Feed, Overvoltage Protection, Ringing Feed, Line Supervision, Codec, 2-4 Wire Hybrid and Test are provided requiring only a few external components. The input impedance conforms with Chinese standard requirements. The device is fabricated using thick film hybrid technology which incorporates various technologies for high voltage capability, optimum circuit design and very high reliability.

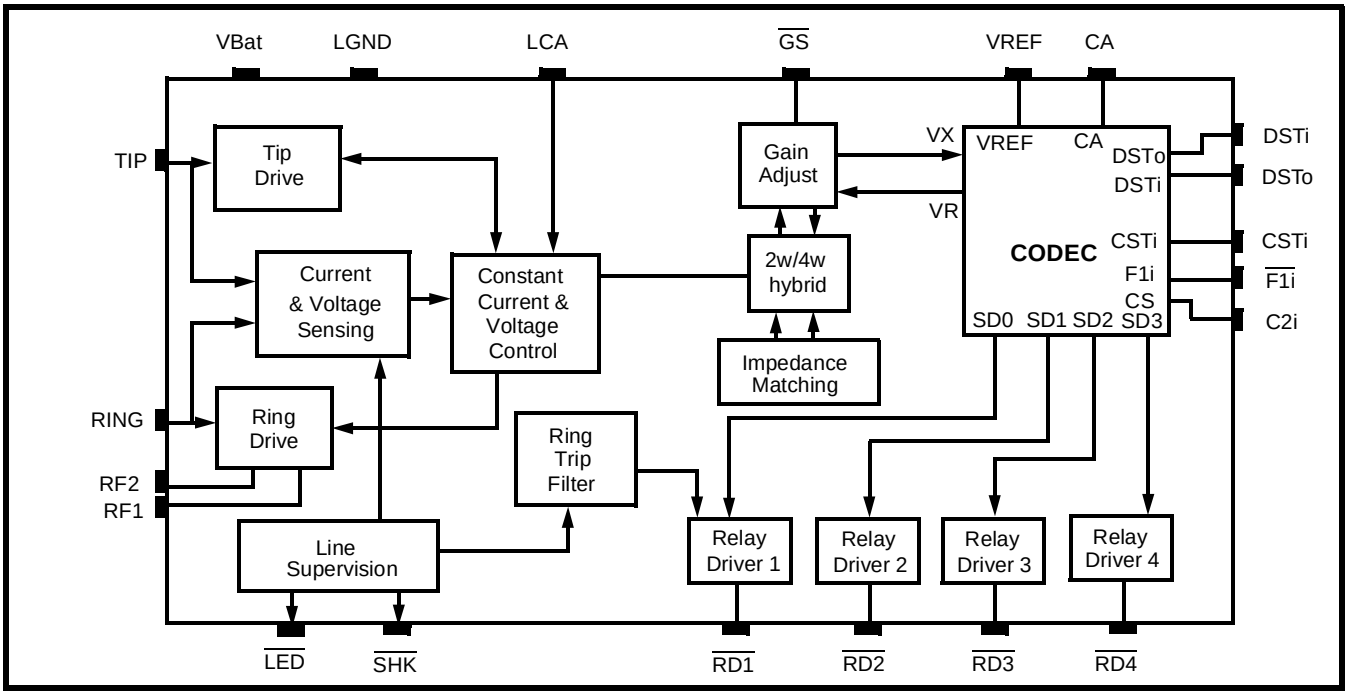


Figure 1 - Functional Block Diagram

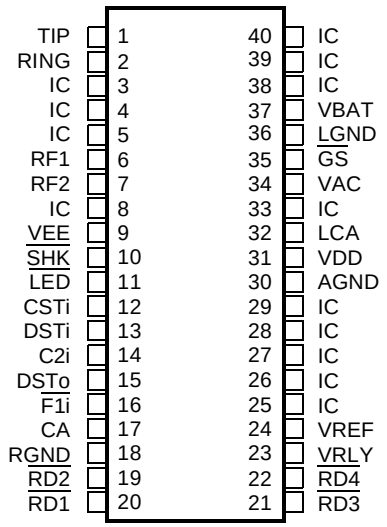


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TIP	**Tip Lead.** Connects to the “Tip” lead of the telephone line.
2	RING	**Ring Lead.** Connects to the “Ring” lead of the telephone line.
3	IC	**Internal Connection:** This pin is internally connected.
4	IC	**Internal Connection:** This pin is internally connected.
5	IC	**Internal Connection:** This pin is internally connected.
6	RF1	**Ring Feed 1:** For OPS operation, connects to the external battery backed ringing generator, see Figure 2.
7	RF2	**Ring Feed 2:** For OPS operation, connects to RING through a normally closed relay contact (K1), see Figure 2.
8	IC	**Internal Connection.** This pin is internally connected.
9	V_{EE}	**Negative Supply Voltage:** (-5V)
10	$\overline{SHK}$	**Switch Hook Detect (Output):** A logic low indicates an off-hook condition.
11	$\overline{LED}$	**LED Drive (Output):** Drives an LED directly through an internal 2.2kΩ resistor. A logic low indicates an off-hook condition.
12	CSTi	**Control ST-BUS in (Input):** A TTL compatible digital input used to control the function of the filter/codec. Three modes of operation may be affected by applying to this input logic high, logic low or an 8-bit serial word, depending on the logic states of CA and F1i. Functions controlled are: power down, filter gain adjust, loopback, chip testing, and the SD outputs which control the relay drivers, ring trip circuitry and impedance selection.
13	DSTi	**Data ST-BUS in (Input):** A TTL compatible digital input which accepts the 8-bit PCM word from the incoming PCM bus.
14	C2i	**Clock Input (Input):** A TTL compatible digital input which accepts the 2048 kHz clock.
15	DSTo	**Data ST-BUS Out (Output).** A three stage TTL compatible digital output which drives the 8-bit PCM word to the outgoing PCM bus.
16	F1i	**Synchronization Input (Input):** A TTL compatible active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the clock, C2i, and provides frame and channel synchronization.

Pin Description (Continued)

Pin #	Name	Description
17	CA	**Control Address (Input):** A three-level digital input which enables PCM input and output, and determines into which control register (A or B) the serial data, presented to CSTi, is stored.
18	RGND	**Relay Ground:** Return path for relay supply voltage.
19	$\overline{RD2}$	**Relay Driver 2:** Connects to a user provided external relay coil. A logic high at the SD1 output of the internal MT8967 codec activates this driver. An internal clamp diode from VRLY to $\overline{RD2}$ is provided. This relay is typically used for DID reversals.
20	$\overline{RD1}$	**Relay Driver 1.** Connects to a user provided external relay coil. A logic high at the SD0 output of the internal MT8967 codec activates this driver. An internal clamp diode from VRLY to $\overline{RD1}$ is provided. This relay is typically used for ringing.
21	$\overline{RD3}$	**Relay Driver 3.** Connects to a user provided external relay coil. A logic high at the SD2 output of the internal MT8967 codec activates this driver. An internal clamp diode from VRLY to $\overline{RD3}$ is provided. This relay is typically used for in-test.
22	$\overline{RD4}$	**Relay Driver 4:** Connects to a user provided external relay coil. A logic high at the SD3 output of the internal MT8967 codec activates this driver. An internal clamp diode from VRLY to $\overline{RD4}$ is provided. This relay is typically used for out-test.
23	V_{RLY}	**Relay Positive Supply Voltage:** Normally +5V. Connects to the relay coil and the relay supply voltage.
24	V_{Ref}	**Voltage Reference (Input):** +2.50V for the internal codec.
25	IC	**Internal Connection**: This pin is internally connected.
26	IC	**Internal Connection**: This pin is internally connected
27	IC	**Internal Connection**: This pin is internally connected
28	IC	**Internal Connection**: This pin is internally connected
29	IC	**Internal Connection**: This pin is internally connected
30	AGND	**Analog Ground**. Analog and Digital Ground. Connects to System Ground.
31	V_{DD}	**Positive Supply Voltage** (+5V)
32	LCA	**Loop Current Adjust (Input).** The maximum constant loop current is a function of the resistance connected from this pin to V_{EE}. Normally left open
33	IC	**Internal Connection.** This pin is internally connected.
34	VAC	**Battery AC Component (Input).** AC noise present in the V_{BAT} supply, isolated from the DC component, can be applied to this pin to reduce longitudinal noise on TIP and RING. To implement this feature, connect a 0.1µF 100V capacitor from V_{BAT} to VAC, and a 1kΩ resistor from VAC to AGND. This pin must be tied to AGND when not used.
35	GS	**Gain Setting (Input**). A logic low at this input adds an additional -0.5dB gain in the receive direction (DSTi to Tip-Ring). This gain is in addition to the gain set by the Codec. A logic high adds 0dB gain.
36	LGND	**Loop Ground.** Return path for the battery (V_{BAT}) supply voltage. Connects to System Ground.
37	V_{Bat}	**Battery Supply Voltage.** Normally -48V.
38	IC	**Internal Connection**: This pin is internally connected
39	IC	**Internal Connection**: This pin is internally connected
40	IC	**Internal Connection**: This pin is internally connected

Functional Description

The Mitel MH89625C OPS SLIC (Off-Premise Subscriber Line Interface Circuit) provides a complete interface between an off-premise telephone line and an digital switching system. All BORSCHT functions are provided requiring only a few external components. The input impedance conforms with Chinese standard requirements.

All functions of the SLIC are controlled by the system Drive (SD) outputs of the internal Mitel A-Law Codec MT8967. The SD outputs are controlled by the serial data input stream at CSTi.

The BORSCHT Functions

The MH89625C performs all of the BORSCHT functions of Battery Feed, Overvoltage Protection, Ringing, Supervision, Codec, Hybrid and Test.

Battery Feed

The MH89625C powers the telephone set with constant DC loop current for short lines and automatically reverts to constant voltage for long lines. The constant loop current is a function of the resistance connected from the LCA pin to $V_{EE.}$

$$R = \frac{147.2 - I_{Loop}}{(0.0001176 \times I_{Loop}) - 0.002586}$$

Where I_{Loop} is the desired constant loop current in mA, and R is the resistance from pin LCA to pin V_{EE} in ohms.

R (kΩ)	open	348k	200k	80k	50k	30k
I_{Loop} (mA)	22.0	25.0	27.1	34.0	40.2	49.7

Overvoltage Protection

The MH89625C is protected from short term (20ms) transients (±250V) between TIP and RING, TIP and ground, and RING and ground. However, additional protection circuitry may be needed depending on the requirements which must be met. Normally simple external shunt protection as shown in Figure 4 is all that is required.

Ringing

The ringing insertion circuit has the capability to provide ringing voltage to a telephone set by simply adding an external relay, ring generator and a transient protector. The internal relay driver switches ringing voltage onto the line via the external ring relay. A clamp diode is included which suppresses voltage transients during relay switching caused by the relay coil. The serial data input at CSTi controls the internal Codec's SDo output which activates the ring driver. Refer to Table 1 for control of SLIC functions.

Supervision

The loop detection circuit determines whether a low enough resistance is across Tip and Ring to be recognized as an off-hook condition. When an off-hook condition occurs, the SHK and LED (the LED output can drive an LED directly) outputs toggle to a low level. These outputs also toggle with incoming dial pulses.

During applied ringing (ring relay driver activated), the loop detection circuit engages a ringing filter. This filter prevents false off-hook detection due to the current associated with the AC ringing voltage as well as current transients that occur when the ringing voltage is switched in and out. The ring trip detection circuitry deactivates the ring relay driver after an off-hook condition is detected.

Codec

The Codec function of the SLIC is implemented using the Mitel MT8967 A-Law Codec. This device provides the conversion interface between the voiceband analog signals of a telephone subscriber loop and the digital signals required in a digital PCM (pulse code modulation) system. Eight-bit PCM encoded digital data enters and leaves the chip serially on DSTi and DSTo pins, respectively.

For detailed information on the CODEC portion of the MH89625C, refer to the MT8967 integrated PCM Filer/Codec data sheet (Microelectronics Digital Communications Handbook, Mitel Semiconductor Issue 9).

Absolute Maximum Ratings* - All voltages are with respect to AGND unless otherwise specified.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{DD} V_{EE}	-0.3 0.3	7 -7	V
2	DC Battery Voltage ①	V_{BAT}	0.3	-65	V
3	DC Ring Relay Voltage	V_{RLY}	-0.3	7	V
4	DC Reference Voltage	V_{REF}	-0.3	V_{DD}	V
5	AC Ring Generator Voltage			150	V_{RMS}
6	DC Digital Input Voltage	$\overline{GS}$, CSTi DSTi, C2i $\overline{F1i}$	-0.3	V_{DD}	V
7	DC Digital (3-level) Input voltage	CA	V_{EE}	V_{DD}	V
8	Storage Temperature	TS	-40	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
① LGND is connected to AGND

Recommended Operating Conditions

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Supply Voltages	V_{DD} V_{EE}	4.75 -4.75	5.0 -5.0	5.25 -5.25	V V	
2	DC Battery Voltage ①	V_{BAT}	-39.8	-48	-60	V	
3	DC Ring Relay Voltage	V_{RLY}		5.0	7	V	
4	DC Reference Voltage ②	V_{REF}	2.488	2.500	2.512	V	
5	AC Ringing Generator Voltage Ringing Generator Frequency		22	90 25	130 28	V_{RMS} Hz	
6	Operating Temperature	T_{OP}	0	25	70	°C	

① LGND is connected to AGND.
② Temperature coefficient of V_{REF} should be better than 100ppm/C.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply and Battery Current ①						LCA = Open
			I_{DD}		8.7	15	mA	
			I_{EE}		8.4	15	mA	
		Short Loop	I_{BAT}		23.5	28	mA	R_{Loop} = 0Ω
		Open Loop	I_{BAT}		1.5	2	mA	R_{Loop} = Open
2		Power Consumption ①	PC					LCA = Open
		On-Hook (V_{BAT})				100	mW	R_{Loop} =Open
		Powerdown (V_{DD} and V_{EE})				150	mW	
		Off-Hook (V_{DD},V_{EE},V_{BAT})				1500	mW	R_{Loop} = 0Ω
3	$\overline{REF}$	DC Reference Voltage			2		µA	
		Mean Current						
4	$\overline{SHK}$	Low Level Output Voltage	V_{OL}	-0.3		0.5	V	I_{OL} = 2mA
		High level Output Voltage	V_{OH}	3.7		5.25	V	I_{OH} = 2mA
5	$\overline{LED}$	Low Level Output Voltage ②	V_{OL}			3.0	V	I_{OL} = 1.1mA
		High Level Output Voltage	V_{OH}	2.0			V	I_{OH} = 0.7mA
6	$\overline{RD1}$ $\overline{RD2}$ $\overline{RD3}$ $\overline{RD4}$	Sink Current, Relay to V_{DD}	I_{OL}	65			mA	V_{OL} = 1.0V
		Clamp Diode Current	I_{CD}	100			mA	
7	$\overline{GS}$	Low Level Input Voltage	V_{IL}			0.8	V	
		High Level Input Voltage	V_{IH}	2.0			V	
8		Low Level Input Current	I_{IL}			1	µA	V_{IL} = 0V
		High Level Input Current	I_{IH}			1	µA	V_{IH} = 5.0V
9	CA	Low Level Input Voltage	V_{IL}			-3.5	V	
		Intermediate Input Voltage	V_{IM}	0.0		0.8	V	
		High Level Input Voltage	V_{IH}	2.4			V	
10	$\overline{RD}$	Low Level Input Current	I_{IL}			10	µA	V_{IL} = 5.0V
		High Level Input Current	I_{IM}			10	µA	V_{IM} = 0.5V
		High Level Input Current	I_{IH}			10		V_{IH} = 5.0V
11	DSTo	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
		High Level Input Voltage	V_{OH}	4.0			V	I_{OH} = 0.1mA
		Tri-State Leakage Current	I_{OZ}		0.1		mA	
12	CSTi DSTi	Low Level Input Voltage	V_{IL}			0.8	V	
		High Level Input Voltage	V_{IH}	2.4			V	
13	C2i F1i	Low Level Input Current	I_{IL}			10	µA	V_{IL} = 0V
		High Level Input Current	I_{IH}			10	µA	V_{IH} = 5.0V

† DC Electrical Characteristics are over Recommended Operating Conditions with V_{DD} at +5.0V ± 5% and V_{EE} at -5.0V ±5% unless otherwise stated.

‡ Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only.

① Supply current and power consumption characteristics are over Recommended Operating Conditions with V_{DD} at 5.0V, V_{EE} at -5.0V and V_{BAT} at -48.0V

② The LED output consists of a 2.2kΩ resistor in series with the $\overline{SHK}$ HCT output.

NOTE 1: Powerdown mode is activated through the CSTi input data stream. Refer to Table 2.

Loop Electrical Characteristics† -

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Maximum AC Ringing ① Current Rejection		33			mA	25Hz, V_{BAT} = -48V
2	Ring Trip Detect Time ②			100		ms	
3	Hook Switch Detect Time: Off-Hook to On-Hook On-Hook to Off-Hook				 20 20	 ms ms	
4	Operating Loop Currents Maximum Operating Loop Current	I_{IP}	18	22 50	26 1850	mA	LCA= Open LCA= 30k to V_{EE}
5	Operating Loop Resistance	R_{IP}	0 0		 2300	Ω Ω	V_{BAT}= -40V V_{BAT}=-48V
6	Loop Current at Off-Hook ③ Detect Threshold	I_{SH}	7	10	13	mA	

† Loop Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

① The SLIC can be loaded with an AC impedance as low as 4000Ω without generating a false $\overline{SHK}$ output. Since each REN represents 8kΩ, the SLIC can drive a REN of 2 without generating a false $\overline{SHK}$ output.

② This parameter is over Recommended Operating Conditions as well as the specified Operating Loop Resistance.

③ Off-Hook Detect ($\overline{SHK}$) will be detected for loop lengths of 2900Ω or less.

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	2-wire Input Impedance ① 600R (Magnitude) 560 Network (Magnitude) 680 Network	Z_{in}		 600 720 813		 Ω Ω Ω	1020 Hz
2	Return Loss at 2-Wire ②		14 18 14	23 24 35		dB dB dB	300 Hz 500-2000 Hz 3400 Hz
3	Longitudinal to Metallic Balance		40 46	54 51		dB dB	300-600 Hz 600-3400 Hz
4	Transhybrid Loss ②		16 20 16	52 41 52		dB dB dB	300 Hz 500-2500 Hz 3400 Hz
5	Power Supply Rejection Ratio at 2-Wire and DSTo: V_{DD} V_{EE} V_{BAT}	PSRR	 20 20 20	 40 30 40		 dB dB dB	Ripple 50mV 1020 Hz

† AC Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only.

① Three impedance selections of Z_{in} = 600Ω, Z_{in}=200Ω + 560 // 0.1µF, and Z_{in}=200Ω + 680 // 0.1µF are available.

② Values apply for all three impedances selections; in all three cases Z_{in} = Reference Impedance.

Note 1: All of the above test conditions use 200Hz to 3400 Hz unless otherwise stated.

Note 2: The transmit codec gain is set to 0dB, the receive codec gain is set to 0dB, and the receive gain adjustment is set to 0dB ($\overline{GS}$=5V), unless otherwise specified.

Note 3: With the transmit and receive gains set to 0dB; 0dBmO at the DSTi input will appear as 0dBm at the Tip-Ring output; 0dBm at the Tip-Ring input will appear as 0dBmO at the DSTo output.

Note 4 All dBm is referenced to 600Ω.

AC Electrical Characteristics† - Transmit (A/D) Path

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Absolute Gain Default (Codec 0dB)		-0.5	0	0.5	dB	Input -6dBm 1020 Hz
2	Gain Programmable Range ①		0		7	dB	1020 Hz
3	Loss Distortion with Frequency (relative to level at 1020Hz with codec at 0dB)		0.0 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3		- - 1.0 0.75 0.35 0.55 1.5	dB dB dB dB dB dB dB	0-200 Hz 200-300 Hz 300-400 Hz 400-600 Hz 600-2400 Hz 2400-3000 Hz 3000-3400 Hz
4	Gain Variation with Input Level (relative to gain at 1020Hz with -6dBm input)		 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB	Input 1020 Hz 0 to + 3dBm -40 to 0dBm -50 to -40dBm -55 to-50dBm
5	Signal input Overload Level at 2-Wire		3.14			dBm	THD $\leq$ 5% Input 1020 Hz
6	Signal Output Overload Level at DSTo		3.14			dBm0	THD $\leq$ 5% Input 1020 Hz
7	Signal to Total Distortion Ratio at DSTo		 35 33.8 28.8 19.5 14.5			 dB dB dB dB dB	Input at 2-Wire 0 to -10dBm -20dBm -30dBm -40dBm -50dBm
8	Out-of-Band Discrimination at DSTo: Signals in 4.6 -72 kHz band Signals in 300 -3400 Hz band other than 1020Hz Signals in 4.6 -72 kHz band				 -50 -40 -25	 dBm0 dBm0 dBm0	Input at 2-Wire -25dBm, 4.6 -72kHz 0dB, 1020 Hz 0dBm, 300-3400 Hz
9	Harmonic Distortion (2nd or 3rd Harmonic) at DSTo				-41	dB	
10	Idle Channel Noise at DSTo			-72	-64	dBm0p	

† AC Gain Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only.

① Codec provides adjustment in 1 dB steps.

Note 1: With the transmit gain set to 0dB; 0dBm at the Tip-Ring input will appear as 0dBmO at the DSTo output.

Note 2: The transmit codec gain is set to 0dB unless otherwise specified.

Note 3: All dBm is referenced to 600Ω.

Note 4: Refer to table 2 for control of SLIC gain.

Note 5: Loss Distortion with Frequency is equivalent to the negative of Frequency Response Gain.

AC Electrical Characteristics† - Receive (D/A) Path

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Absolute Gain Default 1 (Codec 0dB, $\overline{GS}$ = 5V) Default 2 (Codec 0dB, $\overline{GS}$ =oV)		 -0.5 -1.0	 0.0 -0.5	 0.5 0.0	 dB dB	Input -10dBm0 1020 Hz 1020 Hz
2	Gain Programmable Range $\overline{GS}$ = 5V ① $\overline{GS}$ = 0V ①		 -7 -7.5		 -0 -0.5	 dB dB	Input -10dBm0 1020 Hz 1020 Hz
3	Loss Distortion with Frequency (relative to level at 1020 Hz) with Codec at 0dB and $\overline{GS}$ =5V)		 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3		 - - 1.0 0.75 0.35 0.55 1.5	 dB dB dB dB dB dB dB	Input -10dBm0 0-200 Hz 200-300 Hz 300-400 Hz 400-600 Hz 600-2400 Hz 2400-3000 Hz 3000-3400 Hz
4	Gain Variation with Input Level (relative to gain to 1020 Hz with -10dBm0 input)		 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB	Input 1020 Hz 0 to +3dBm -40 to 0dBm -50 to -40dBm -55 to -50dBm
5	Signal Input Overload Level at DSTi		3.14			dBm	THD ≤ 5% Input 1020 Hz
6	Signal Output Overload Level at 2-Wire		3.14			dBm0	THD ≤ 5% Input 1020 Hz
7	Signal Output to Total Distortion Ratio at 2-Wire		 35 32.9 24.9 19.9			 dB dB dB dB	Input at 2-Wire 0 to -20dBm -30dBm -40dBm -50dBm
8	Out-of-Band Discrimination at 2-wire Signals in 4.6 -72kHz band Signals in 300-3400 Hz band other than 1020 Hz Signals in 4.6 -72 kHz band				 -50 -40 -25	 dBm dBm dBm	Input at DSTi -25dBm0, 4.6 -72 kHz 0dBm0, 1020 Hz 0dBm0, 300 -3400 Hz
9	Harmonic Distortion (2nd or 3rd Harmonic) at 2-Wire				-41	dB	
10	Idle Channel Noise at 2-Wire			 -73 -73	 -67 -67	 dBmp dBmp	Gain Setting: -3.5dB -7dB

† AC Gain Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only.

① Codec provides adjustment in 1 dB steps

Note 1: With the transmit gain set it 0dB; 0dBm0 at the DSTi input will appear as 0dBm at the Tip-Ring output.

Note 2: The receive codec gain is set to 0dB; and the receive gain adjustment is set to 0dB ($\overline{GS}$ =5V), unless otherwise specified.

Note 3: All dBm is referenced to 600Ω

Note 4: Refer to Table 2 for control of SLIC gain.

Note 5: Loss Distortion with Frequency is equivalent to the negative of Frequency Response Gain.

Table 1- Control of SLIC Functions through Codec 8 bit Register B

Bit	Codec Name (SLIC Name)	Description
7, 6	CODEC TESTING CONTROL	Codec Testing Controls. Set bits to 0 for normal operation. For details of testing functions, see the MT8967 integrated PCM Filter/Codec data sheet.
3	SD3 (RD4)	When logic '0', SD3 goes to the open state which deactivates the internal relay driver 4, RD4 output goes to the open state.
2	SD2 (RD3)	When logic '0' SD2 goes to AGND which deactivates the internal relay driver 3, RD3 output goes to the open state.
1	SD1 (RD2)	A logic '0', SD1 goes to AGND which deactivates the internal relay driver 2, $\overline{RD2}$ output goes to the open state. A logic '1', SD1 goes to V_{DD} which activates the internal relay driver 2, $\overline{RD2}$ output goes to RGND.
0	SD0 (RD1)	A logic '0', SD0 goes to AGND which deactivates the internal relay driver 1, $\overline{RD1}$ output goes to the open state. A logic '1', SD0 goes to V_{DD} which activates the internal driver 1, $\overline{RD1}$ output goes to RGND.

Table 2 - Modified Analog Gain* - Which when combined with CODEC gives 0dBm

Variant	Input Impedance	Transmit (A/D) Path	Receive (D/A) Path	Units
MH89625C	600R	4.02	-4.02	dB
MH89625C-5	200R + 680R // 0.1µF	2.72	-2.72	dB
MH89625C-6	200R + 560R // 0.1µF	3.26	-3.26	dB

* All with GS = High and A-Law CODEC (Mitel)

Table 3- Control of SLIC Functions through $\overline{GS}$ and Codec 8 Bit Register A

Bit 7	Bit 6	Special Function Control		
0	0	Normal Operation		
0	1	Digital Loopback		
1	0	Analog Loopback		
1	1	Powerdown		
Bit 5	**Bit 4**	**Bit 3**	**Receive (D/A) Gain (dB)**	
			With GS =0	**With GA = 1**
0	0	0	0	-0.5
0	0	1	-1	-1.5
0	1	0	-2	-2.5
0	1	1	-3	-3.5
1	0	0	-4	-4.5
1	0	1	-5	-5.5
1	1	0	-6	-6.5
1	1	1	-7	-7.5
Bit 2	**Bit 1**	**Bit 0**	**Transmit (A/D) Gain (dB)**	
0	0	0	0	
0	0	1	+1	
0	1	0	+2	
0	1	1	+3	
1	0	0	+4	
1	0	1	+5	
1	1	0	+6	
1	1	1	+7	

Note: A transmit gain of 0dB indicates that an analog input signal of 0dBm at Tip-Ring will appear as 0dBmO at the DSTo output. A receive gain of 0dB indicates that an input signal of 0dBmO will appear as 0dBm at the Tip-Ring output.

Hybrid

The 2-4 Wire hybrid circuit separate the 2-wire balanced full duplex signal at Tip and Ring of the telephone line into 4-wire receive and transmit ground referenced analog signals internal to the SLIC. These analog signals are internally connected to the MT8967 Filter/Codec which translates the analog signals to digital PCM. The hybrid also includes cancellation circuitry which prevents the input PCM signal at DSTi from appearing at DSTo. The degree to which the Hybrid minimizes the contribution of the input signal at DSTi from appearing at the DSTo output is specified as transhybrid loss. See the Network Balance section for maximizing transhybrid loss.

Return Loss

To maximize return loss, the impedance at Tip-Ring should match the SLIC's input impedance (Z_{in}).

Network Balance

Transhybrid loss is maximized when the line termination impedance and the SLIC's network balance are matched. The MH89625C's network balance impedance is automatically internally set to match the SLIC's input impedance (Z_{in}). Therefore, the SLIC's transhybrid loss is maximized when the line termination impedance and the SLIC's input impedance (Z_{in}) are matched.

Tip-Ring Drive Circuit

The PCM input ground referenced signal at DSTi is converted to a balanced output signal at Tip and Ring. The Tip-Ring Drive Circuit is optimized for good 2-wire longitudinal balance.

Tip-Ring Receive Gain

The differential audio signal at Tip and Ring is converted to a ground referenced PCM signal at the DSTo output.

Transmit Gain

Transmit Gain (Tip-Ring to DSTo) and Receive Gain (DSTi to Tip-Ring) are programmed in 1dB steps by writing to the Codec's Control Register A via the CSTi serial data stream. In addition, a Receive Gain adjustment is provided which when activated provides an additional -0.5dB gain. Refer to control of SLIC gain.

Short Circuit Protection

The MH89625C is protected from long term (infinite) short circuit conditions occurring between Tip and Ring, Tip and AGND, and Ring and AGND.

Protection Circuit Design

The high voltage protection circuit is the MH80625C which can be used in conjunction with the MH89625C to meet the CCITT K.20 specification. See Figures 3 and 4. The protection circuit consists of 1 MOSFET Transistor (BUZ 22) per 16 lines and 4 voltage clamping diodes (IN4004) per line circuit. This protection circuit will dissipate the lightning and AC power energy to protect the line circuit. The Energy Dump Ground (EDG) is tied to the chassis of the system ground. The PCB E.D.G. track to the MOSFET must be run separately. The width of the ground track should be greater than 0.050 thou and the resistance should be kept as low as possible, less than 1 ohm. The MOSFET requires a heat sink of 9°C/W to dissipate the heat generated by the overvoltages

Mechanical Data

See Figure 6.

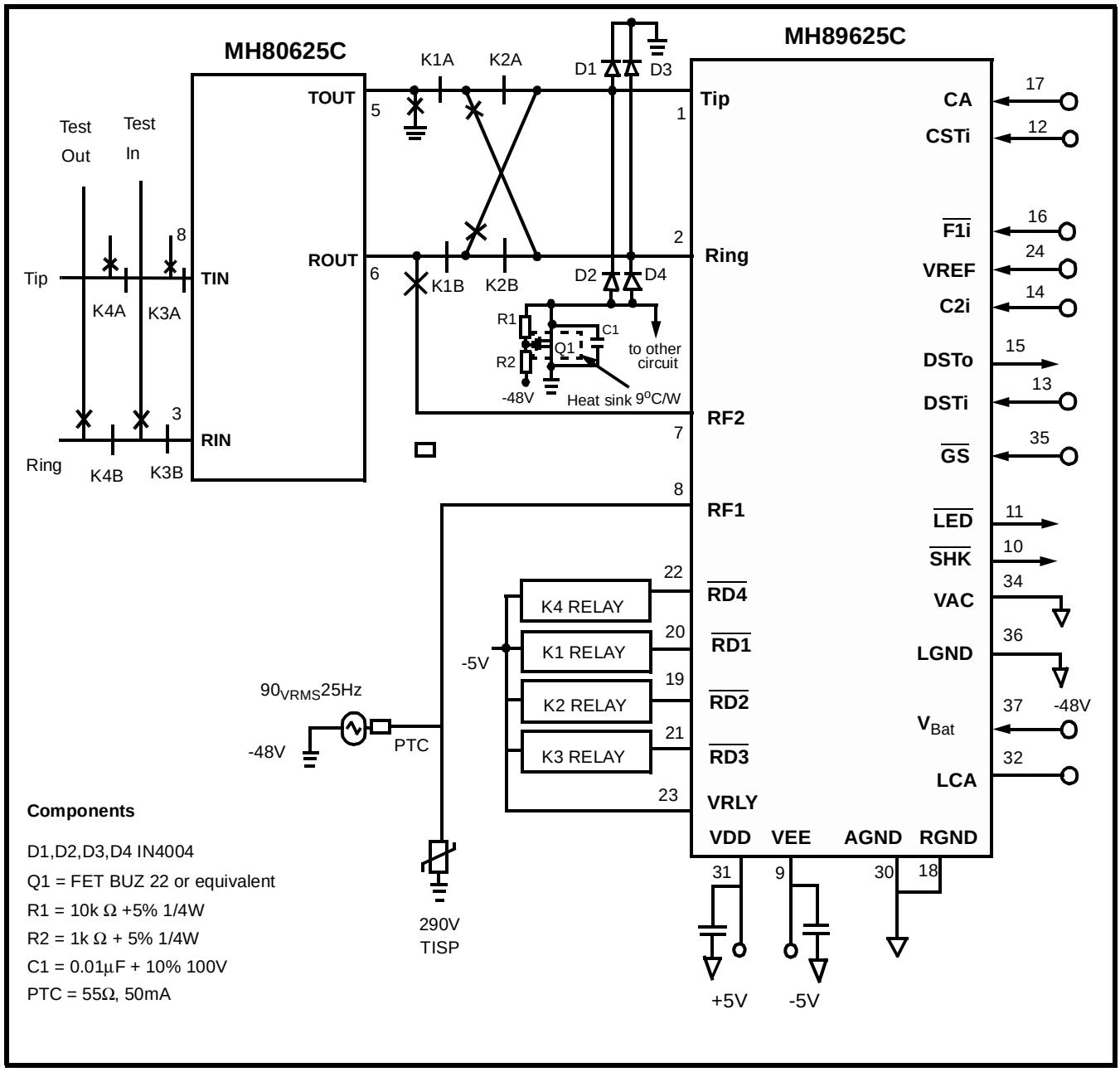


Figure 3 - Typical Line Card Application

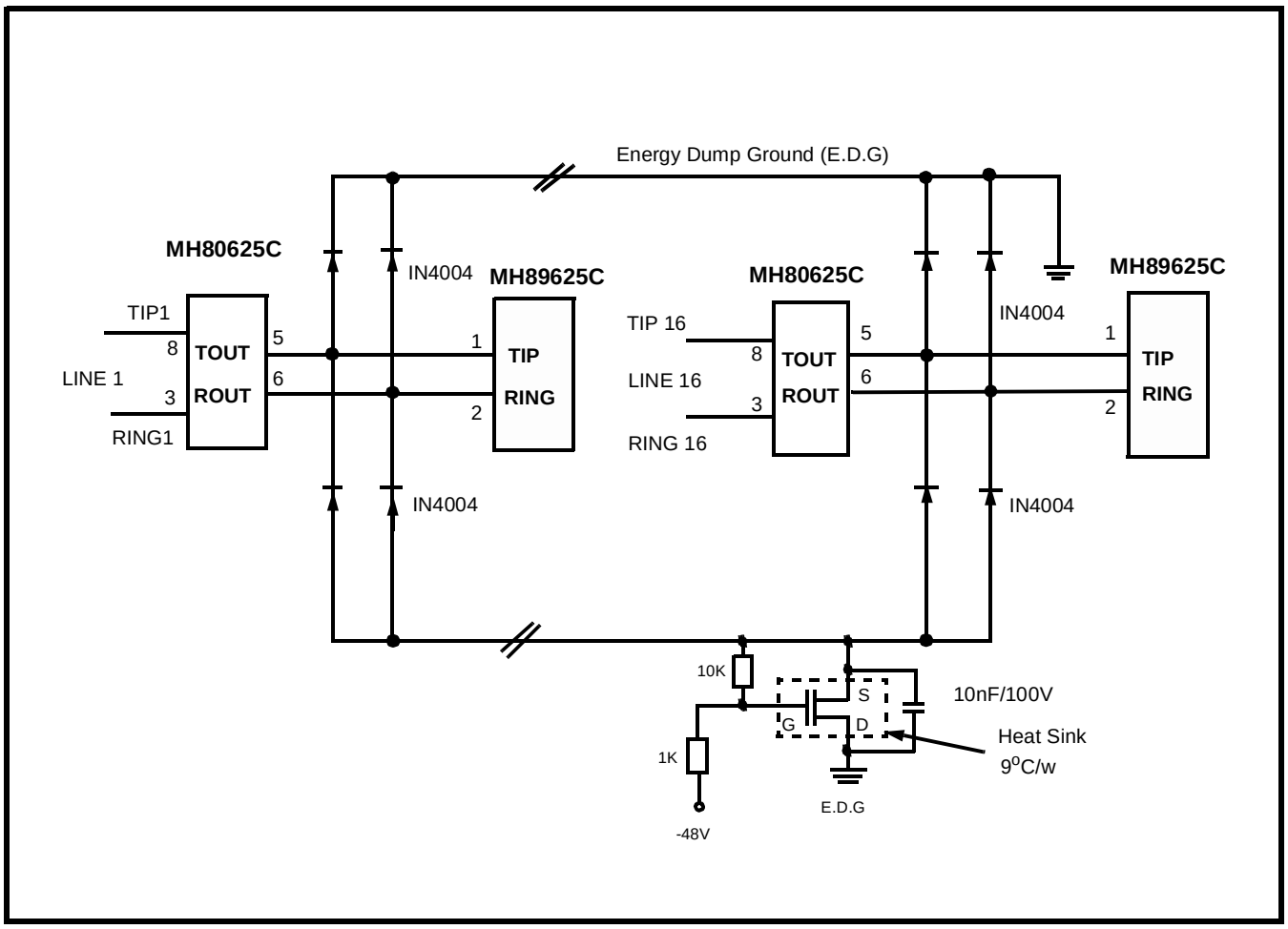
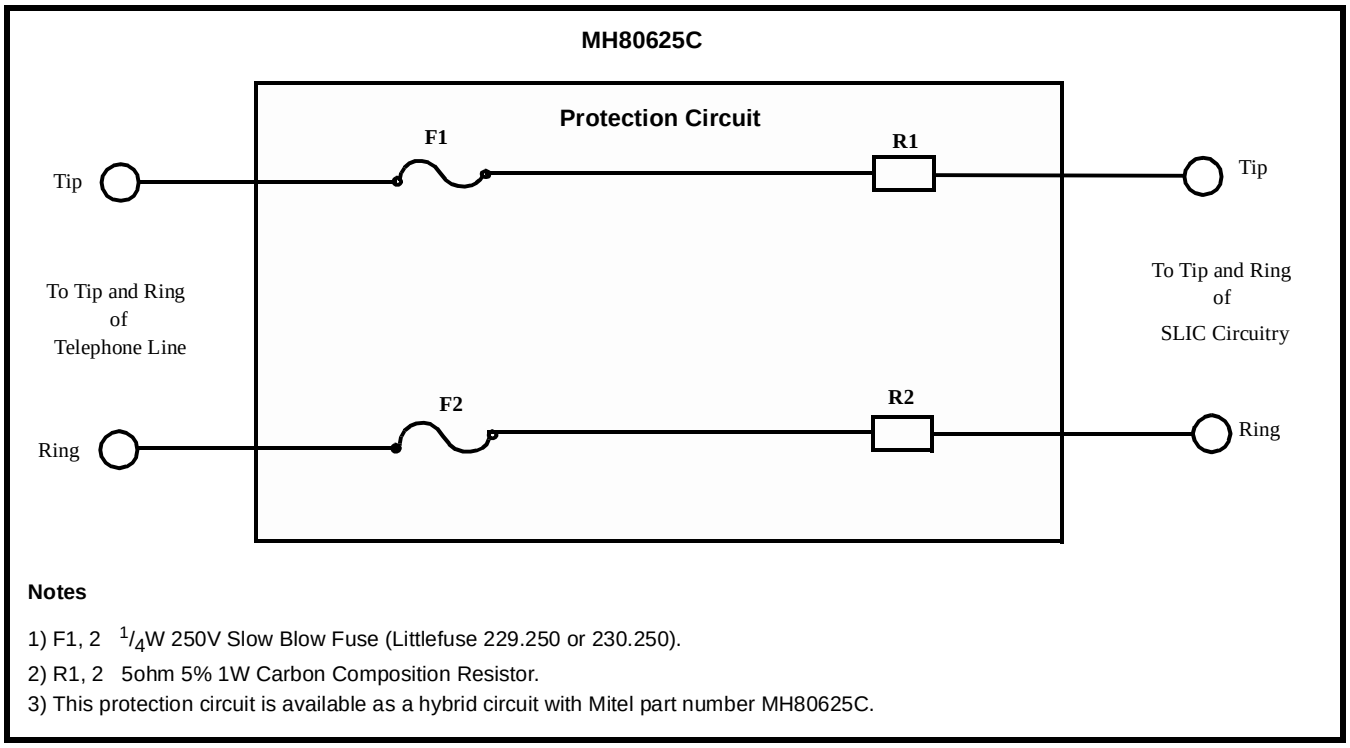


Figure 4 - 16 Lines Circuit Configuration



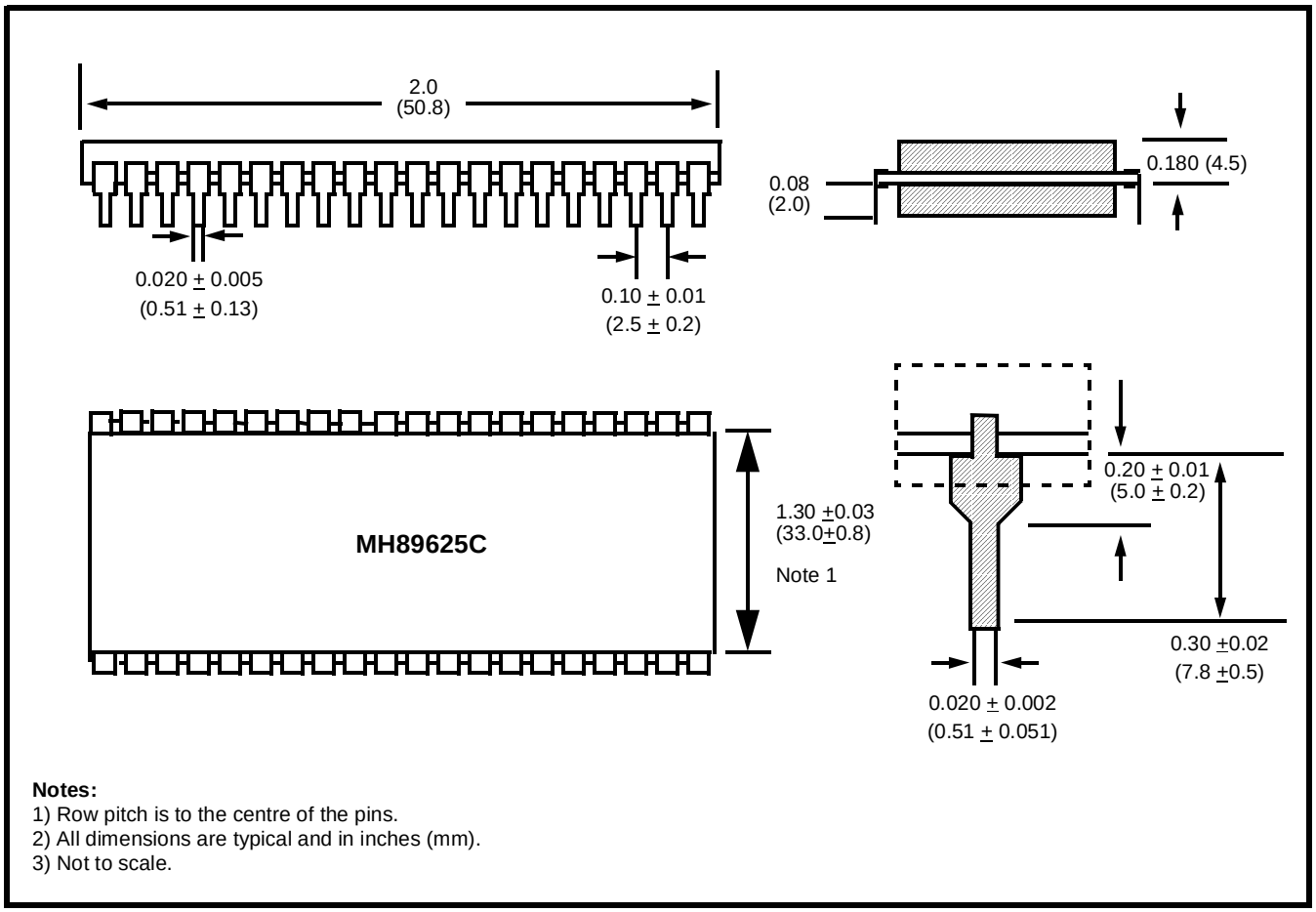
Notes

1) F1, 2 $^1/_4$W 250V Slow Blow Fuse (Littlefuse 229.250 or 230.250).

2) R1, 2 5ohm 5% 1W Carbon Composition Resistor.

3) This protection circuit is available as a hybrid circuit with Mitel part number MH80625C.

Figure 5 - Solid State External Protection Application Circuit



Notes:
1) Row pitch is to the centre of the pins.
2) All dimensions are typical and in inches (mm).
3) Not to scale.

Figure 6 - Mechanical Data

Notes: