Data Sheet December 2001

3A, 55V, 0.070 Ohm, N-Channel UltraFET Power MOSFET

This N-Channel power MOSFET is manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery operated products.

Formerly developmental type TA75309.

Ordering Information

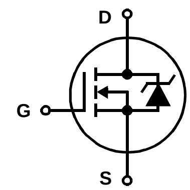
PART NUMBER	PACKAGE	BRAND
HUF75309T3ST	SOT-223	5309

NOTE: HUF75309T3ST is available only in tape and reel.

Features

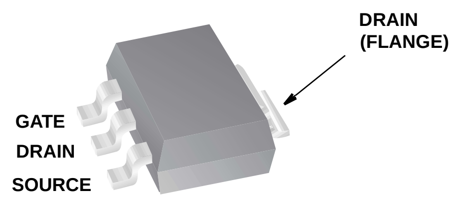
- 3A, 55V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.070\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

SOT-223



Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		HUF75309T3ST	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20V	V
Drain Current			
Continuous (Note 2) (Figure 2)	I_D	3	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation (Note 2)	P_D	1.1	W
Derate Above 25^{o}C		9.09	mW/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 45V, V_{GS} = 0V, $T_A = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 3A, V_{GS} = 10V (Figure 9)		-	0.057	0.070	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D ≅ 3A, R_L = 10Ω, V_{GS} = 10V, R_{GS} = 28Ω		-	-	45	ns
Turn-On Delay Time	$t_{d(ON)}$			-	8	-	ns
Rise Time	t_r			-	20	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	12	-	ns
Fall Time	t_f			-	28	-	ns
Turn-Off Time	t_{OFF}			-	-	65	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 30V, I_D ≅ 3A, R_L = 10Ω, $I_{g(REF)}$ = 1.0mA (Figure 13)	-	19	23	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	10.7	13	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	0.71	0.85	nC
Gate to Source Gate Charge	Q_{gs}			-	1.40	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	4.80	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	352	-	pF
Output Capacitance	C_{OSS}			-	146	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	30	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.164 in^2 (See note 2)		-	-	110	^{o}C/W
		Pad Area = 0.068 in^2 (See TB377)		-	-	126	^{o}C/W
		Pad Area = 0.026 in^2 (See TB377)		-	-	143	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 3A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3A, dI_{SD}/dt = 100A/μs	-	-	41	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 3A, dI_{SD}/dt = 100A/μs	-	-	59	nC

NOTE:

2. 110^{o}C/W measured using FR-4 board with 0.164 in^2 footprint for 1000 seconds.

Typical Performance Curves

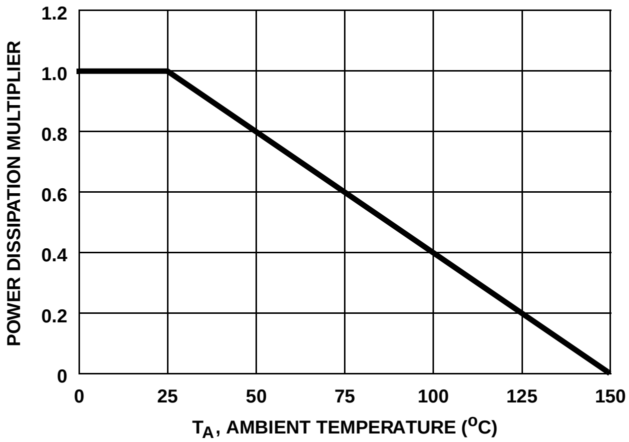


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

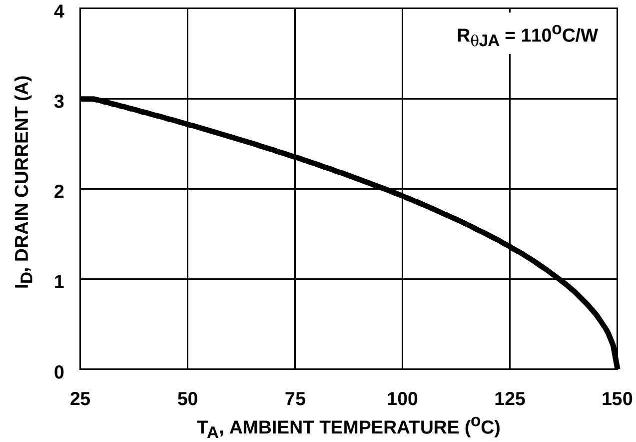


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

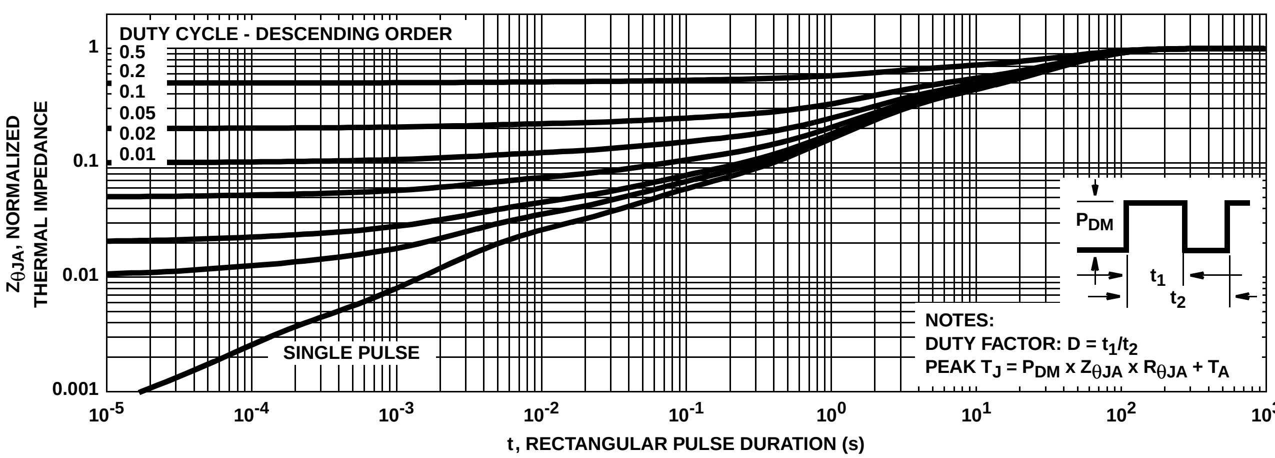


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

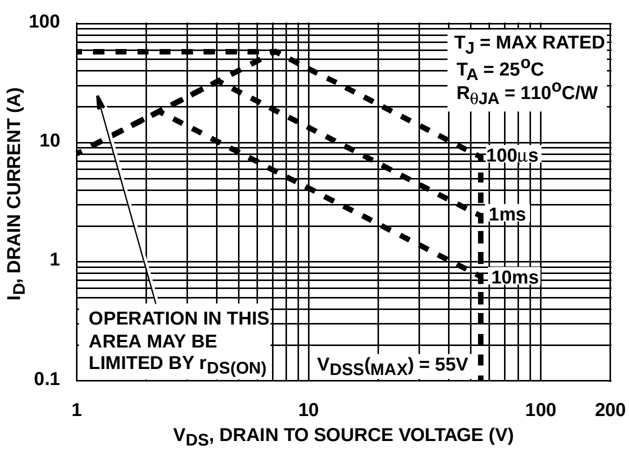


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

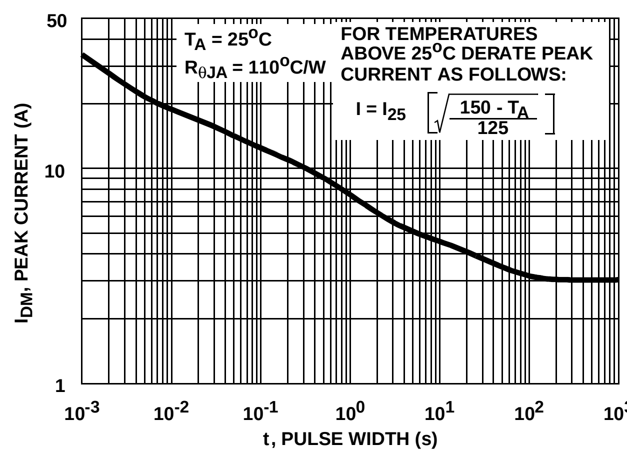
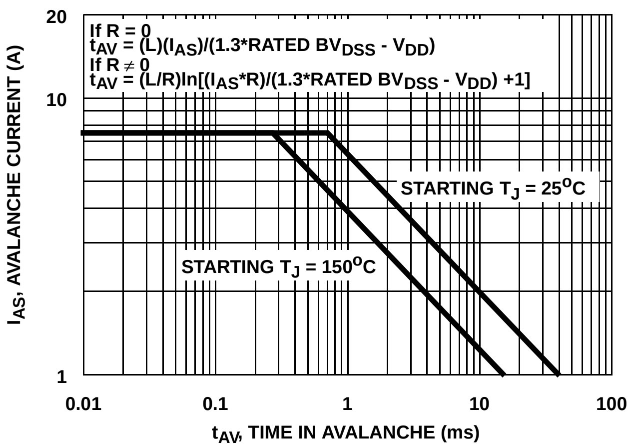


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

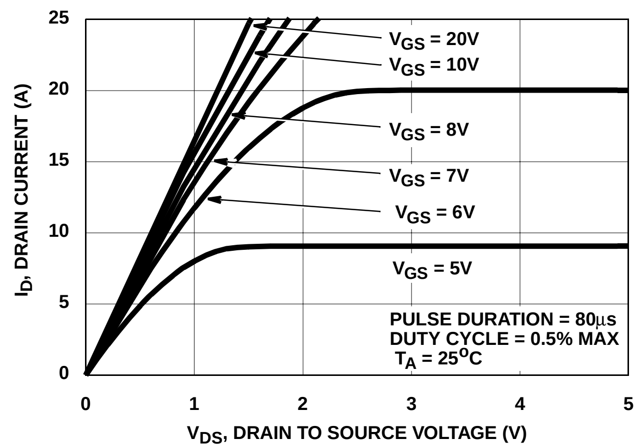


FIGURE 7. SATURATION CHARACTERISTICS

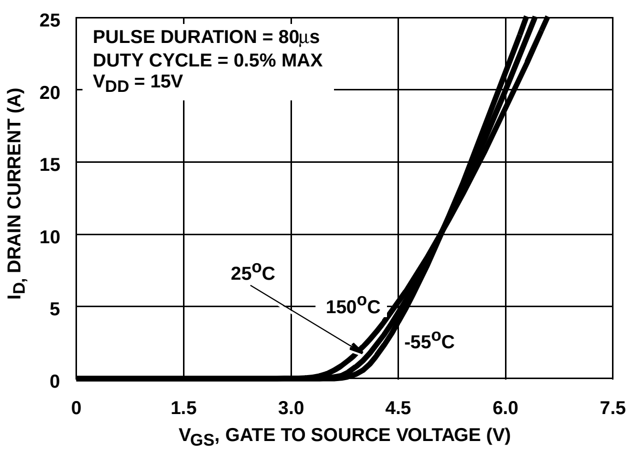


FIGURE 8. TRANSFER CHARACTERISTICS

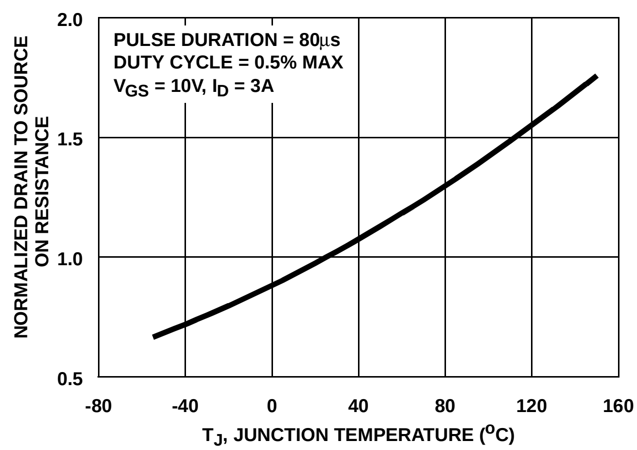


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

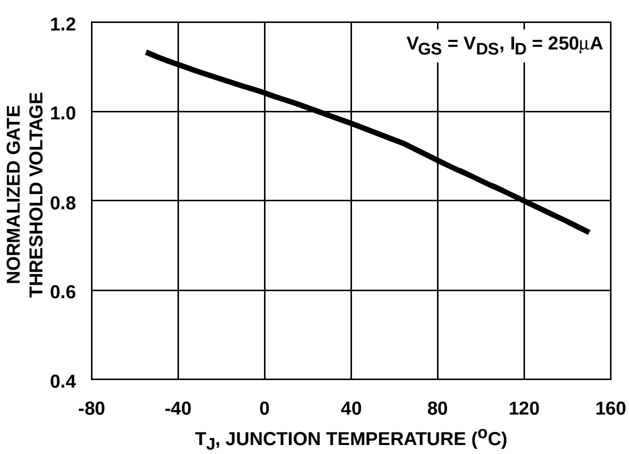


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

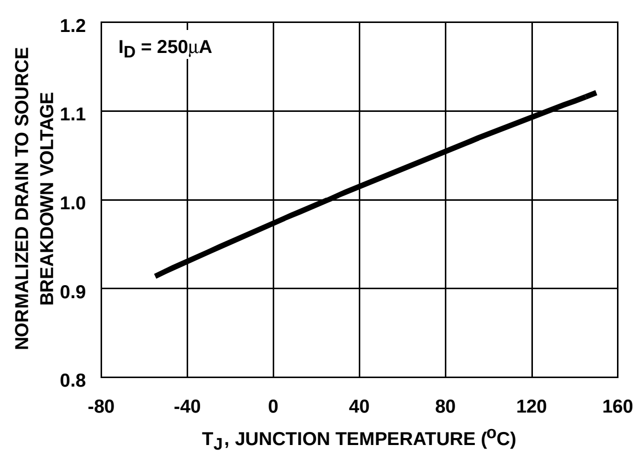


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

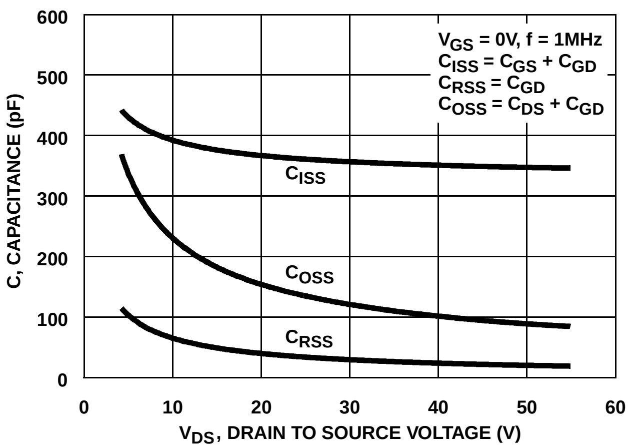
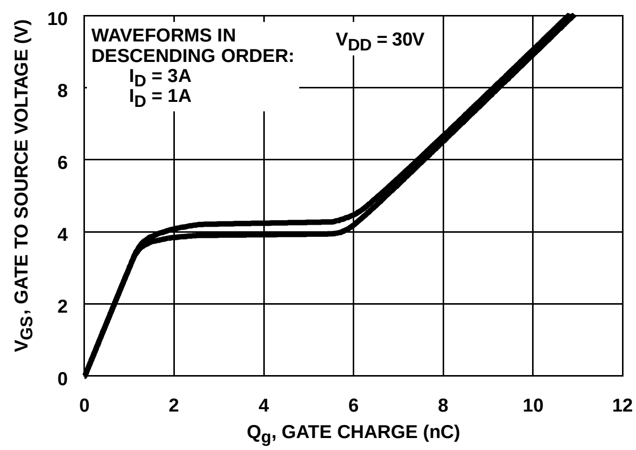


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

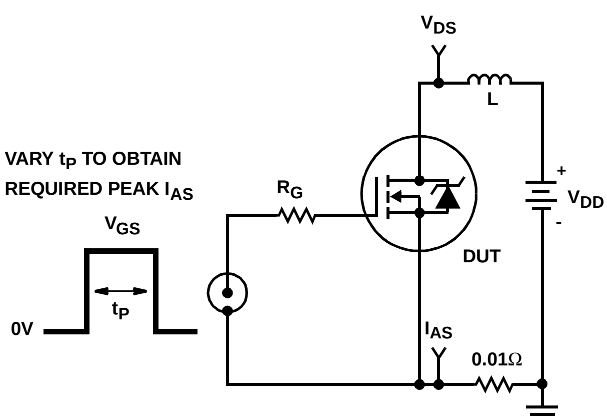


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

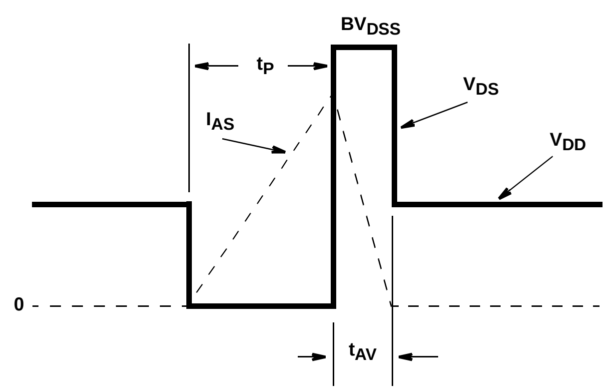


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

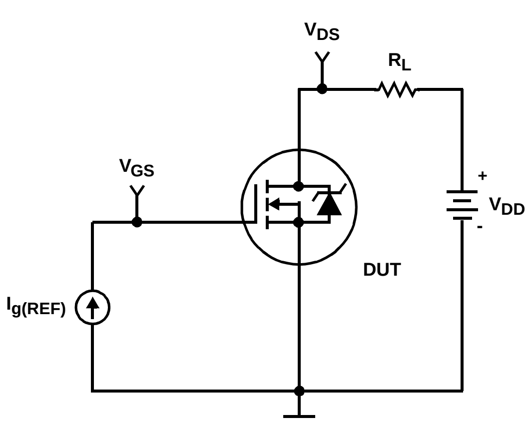


FIGURE 16. GATE CHARGE TEST CIRCUIT

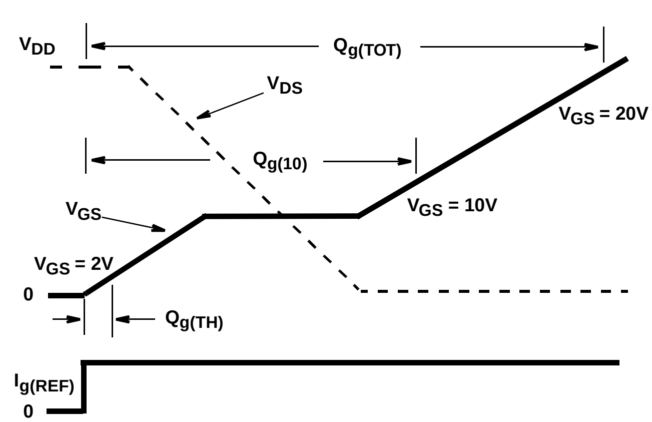


FIGURE 17. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

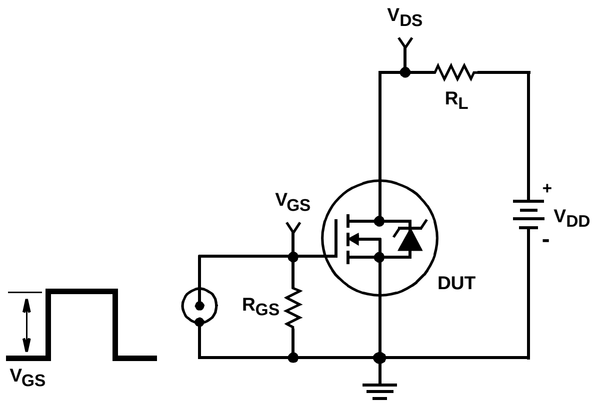


FIGURE 18. SWITCHING TIME TEST CIRCUIT

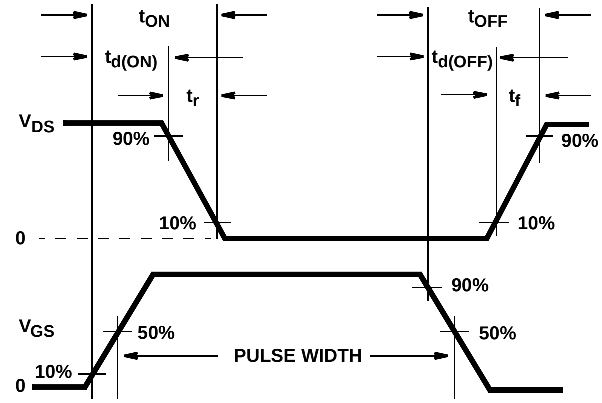


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, $T_{J(MAX)}$, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, $P_{D(MAX)}$, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal impedance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that $T_{J(MAX)}$ is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the SOT-223 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of the $P_{D(MAX)}$ is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow.This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchildl device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

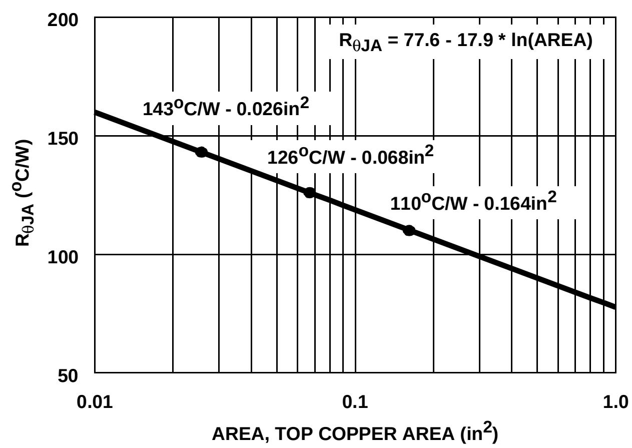


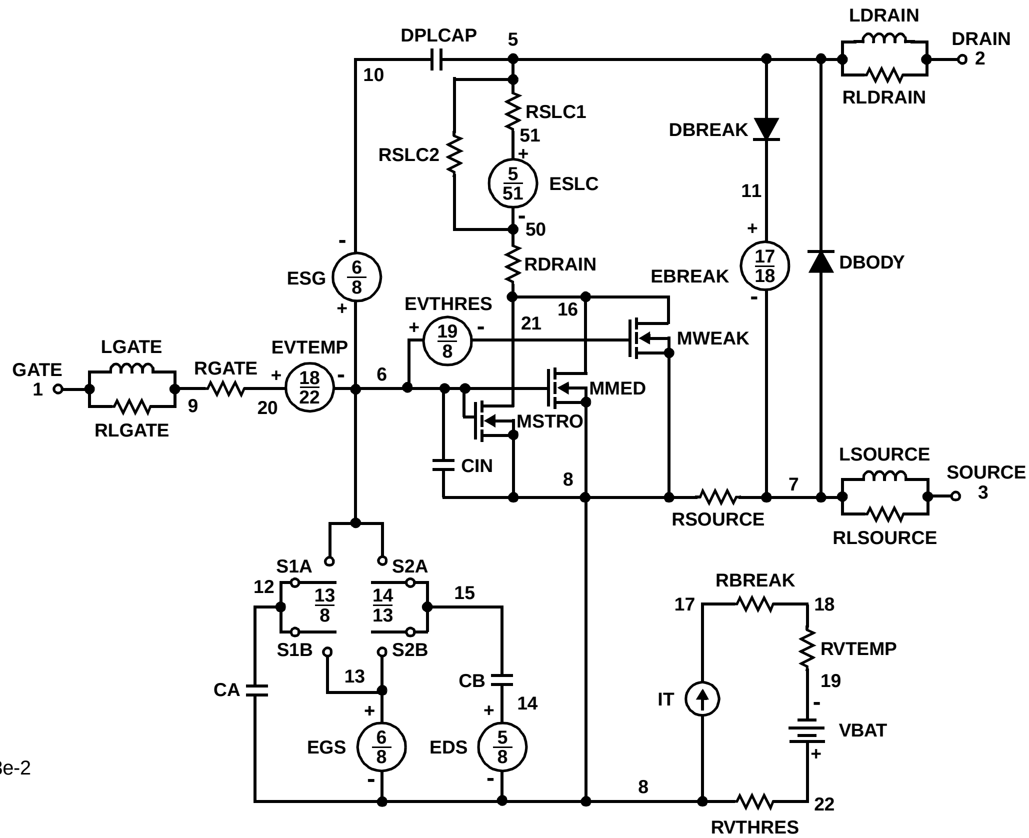
FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD AREA

Displayed on the curve are the three $R_{\theta JA}$ values listed in the Electrical Specifications table. The three points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, $P_{D(MAX)}$. Thermal resistances corresponding to other component side copper areas can be obtained from Figure 20 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 77.6 - 17.9 \times \ln(\text{Area}) \quad \text{(EQ. 2)}$$

PSPICE Electrical Model

.SUBCKT HUF75309T3ST 2 1 3 ;   REV December 97




```
CA  12 8 5.0e-10
CB  15  14 5.0e-10
CIN  6  8 3.27e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 58.46
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1e-9
LGATE 1  9 2.71e-9
LSOURCE  3  7 5.6e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 5e-3
RGATE  9  20 2.2
RLDRAIN 2 5 10
RLGATE 1 9 27.1
RLSOURCE 3 7 5.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 4.8e-2
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*50),3))}

.MODEL DBODYMOD D (IS = 3.4e-13  RS = 2.3e-2   TRS1 = 2.2e-3  TRS2 = 1.03e-6  CJO = 6.55e-10  TT = 3.6e-8 M = 0.57)
.MODEL DBREAKMOD D (RS = 2.8e-  1TRS1 = 1e-  4TRS2 = 2.25e-5)
.MODEL DPLCAPMOD D (CJO = 4e-1  0IS = 1e-3  0N = 10 M = 0.75)
.MODEL MMEDMOD NMOS (VTO = 3.35 KP = 3 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.2)
.MODEL MSTROMOD NMOS (VTO = 3.65 KP = 16 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.97 KP = 0.125 LAMBDA = 1e-3 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 22 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.07e-  3TC2 = -5.2e-7)
.MODEL RDRAINMOD RES (TC1 = 5.25e-2  TC2 = 1.08e-4)
.MODEL RSLCMOD RES (TC1 = 3.3e-3 TC2 = 1.03e-7)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -3.15e-3 TC2 = -9.41e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.61e-  3TC2 = 1.37e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -7.25  VOFF= -4.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.25  VOFF= -7.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0  VOFF= 2.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.5  VOFF= 0)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

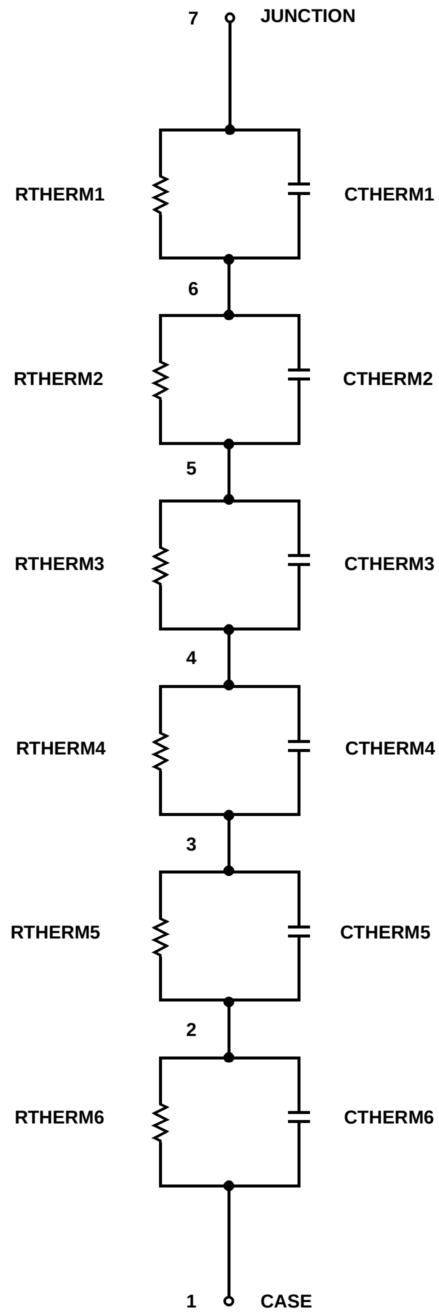
SPICE Thermal Model

REV December 97

HUF75309T3ST

CTHERM1 7 6 7.5e-5
CTHERM2 6 5 4.0e-4
CTHERM3 5 4 1.7e-3
CTHERM4 4 3 1.5e-2
CTHERM5 3 2 7.1e-2
CTHERM6 2 1 5.9e-1

RTHERM1 7 6 7.0e-2
RTHERM2 6 5 2.7e-1
RTHERM3 5 4 2.0
RTHERM4 4 3 3.5
RTHERM5 3 2 30
RTHERM6 2 1 80



PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.