FAIRCHILD

SEMICONDUCTOR ™

April 2000

QFET™

FQP140N03L

30V LOGIC N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters, high efficiency switching for power management in portable and battery operated products.

Features

- 140A, 30V, $R_{DS(on)}$ = 0.0045Ω @V_{GS} = 10 V
- Low gate charge (typical 73 nC)
- Low Crss (typical 580 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating

TO-220
FQP Series

G
D
S

D

G

S
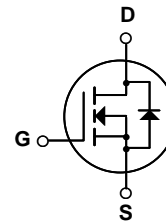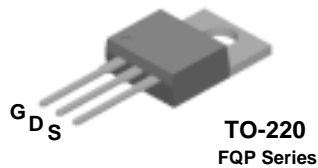
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FQP140N03L	Units
V_{DSS}	Drain-Source Voltage			30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	(Note 6)	140	A
		- Continuous (T_C = 100°C)	(Note 6)	99	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	490	A
V_{GSS}	Gate-Source Voltage			± 20	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	710	mJ
I_{AR}	Avalanche Current		(Note 1)	140	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	18	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)			180	W
	- Derate above 25°C			1.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.84	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	30	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C	--	0.03	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30$ V, $V_{GS} = 0$ V	--	--	1	µA
		$V_{DS} = 24$ V, $T_C = 150°C$	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 70$ A	--	0.0038	0.0045	Ω
		$V_{GS} = 5$ V, $I_D = 70$ A	--	0.005	0.006	
g_{FS}	Forward Transconductance	$V_{DS} = 15$ V, $I_D = 70$ A (Note 4)	--	85	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	3400	4420	pF
C_{oss}	Output Capacitance		--	2090	2720	pF
C_{rss}	Reverse Transfer Capacitance		--	580	755	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 70$ A, $R_G = 25$ Ω	--	60	130	ns
t_r	Turn-On Rise Time		--	770	1500	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	250	510	ns
Q_g	Total Gate Charge	$V_{DS} = 24$ V, $I_D = 140$ A, $V_{GS} = 5$ V	--	73	95	nC
Q_{gs}	Gate-Source Charge		--	29.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	38.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	140	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	490	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 140$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 140$ A, $dI_F / dt = 100$ A/µs (Note 4)	--	70	--	ns
Q_{rr}	Reverse Recovery Charge		--	105	--	nC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 36µH, $I_{AS} = 140$A, $V_{DD} = 15$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 140$A, di/dt ≤ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature
6. Continuous Drain Current Calculated by Maximum Junction Temperature : Limited by Package
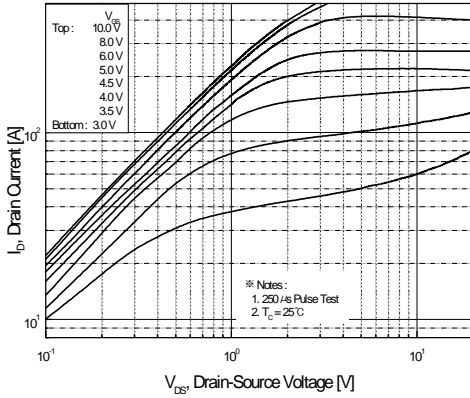
Typical Characteristics

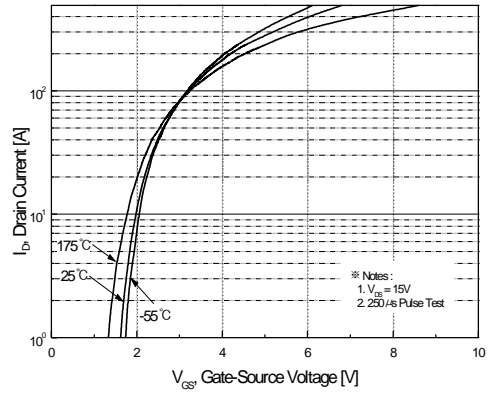**Figure 1. On-Region Characteristics**
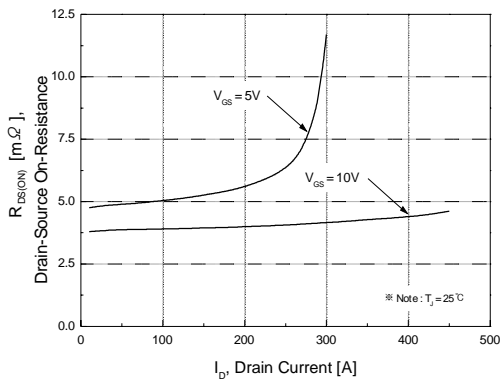

Figure 2. Transfer Characteristics

**Figure 3. On-Resistance Variation vs.
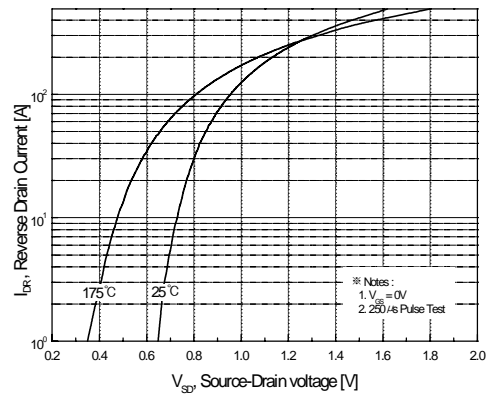Drain Current and Gate Voltage**

**Figure 4. Body Diode Forward Voltage
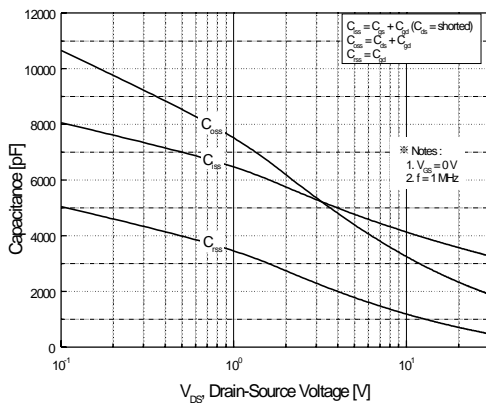Variation vs. Source Current
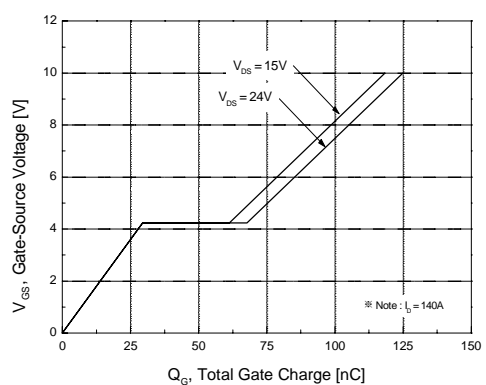and Temperature**

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

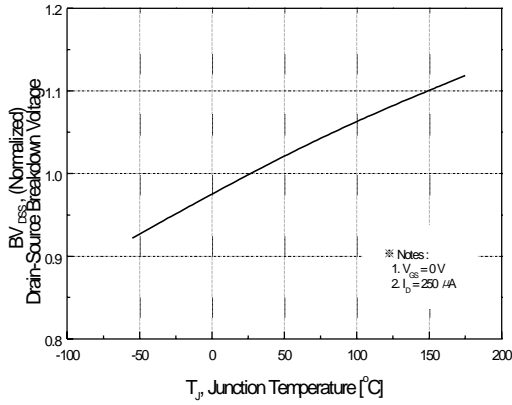## Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature
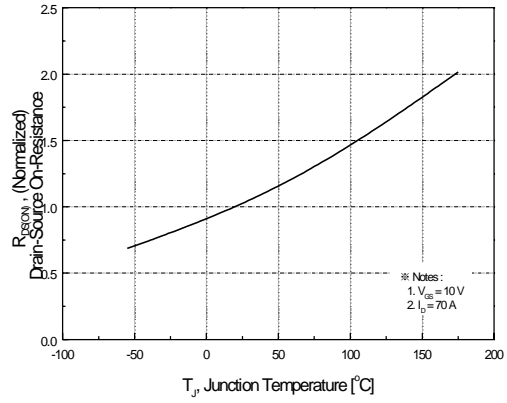

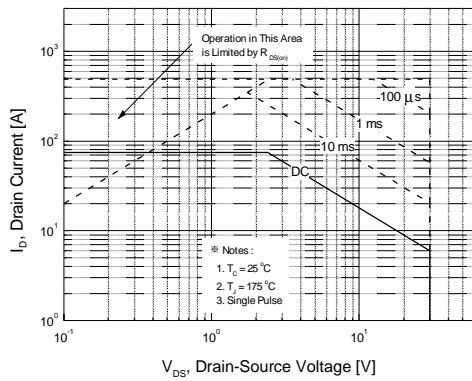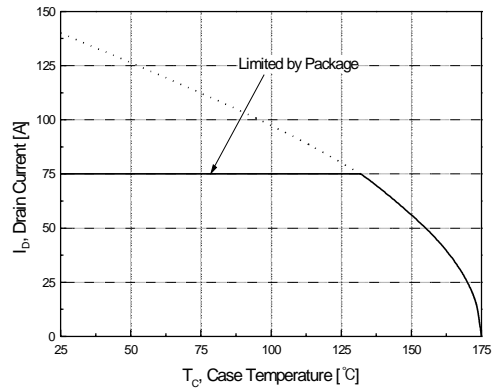**Figure 8. On-Resistance Variation vs. Temperature**

Figure 9. Maximum Safe Operating Area
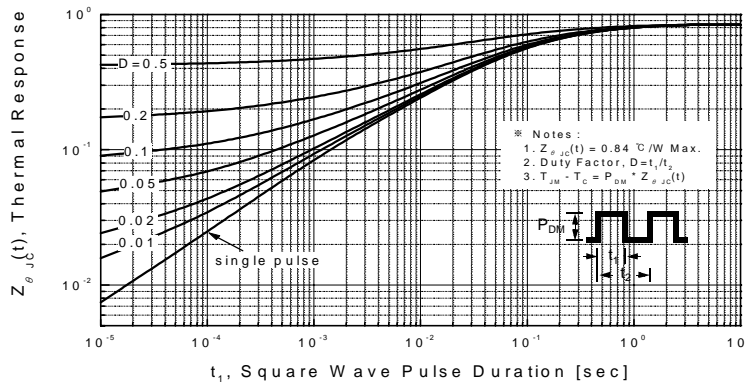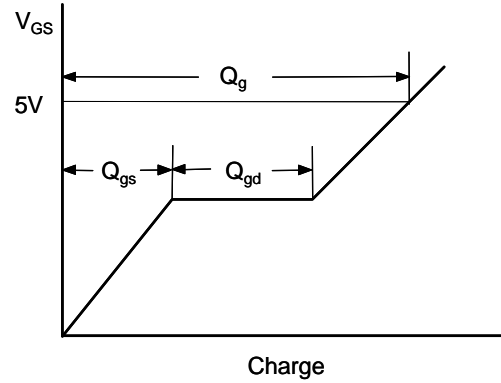

Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Same Type
as DUT

12V

200nF

50KΩ

300nF

V_{GS}

DUT

3mA

V_{DS}

V_{GS}

5V

Q_g

Q_{gs}

Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{DS}

R_L

V_{DD}

R_G

V_{GS}

5V

DUT

V_{DS}

90%

V_{GS}

10%

$t_{d(on)}$

t_r

t_{on}

$t_{d(off)}$

t_f

t_{off}
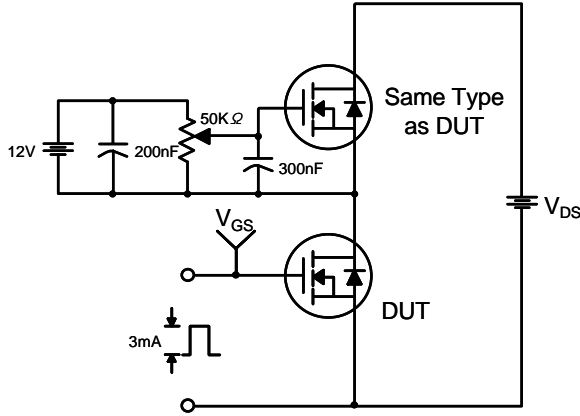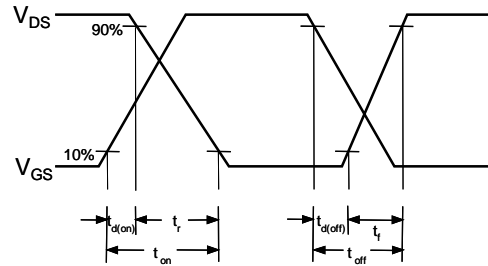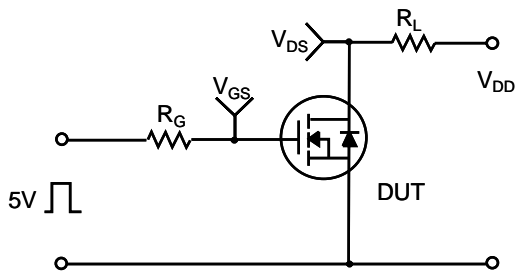
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS}

L

I_D

R_G

V_{DD}

10V

DUT

t_p

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p

Time
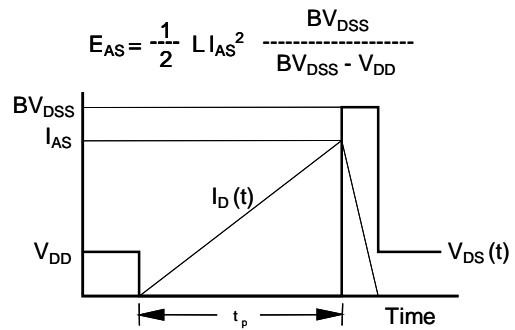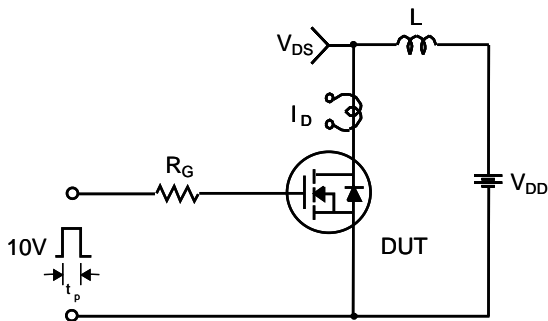
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

−

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

TO-220
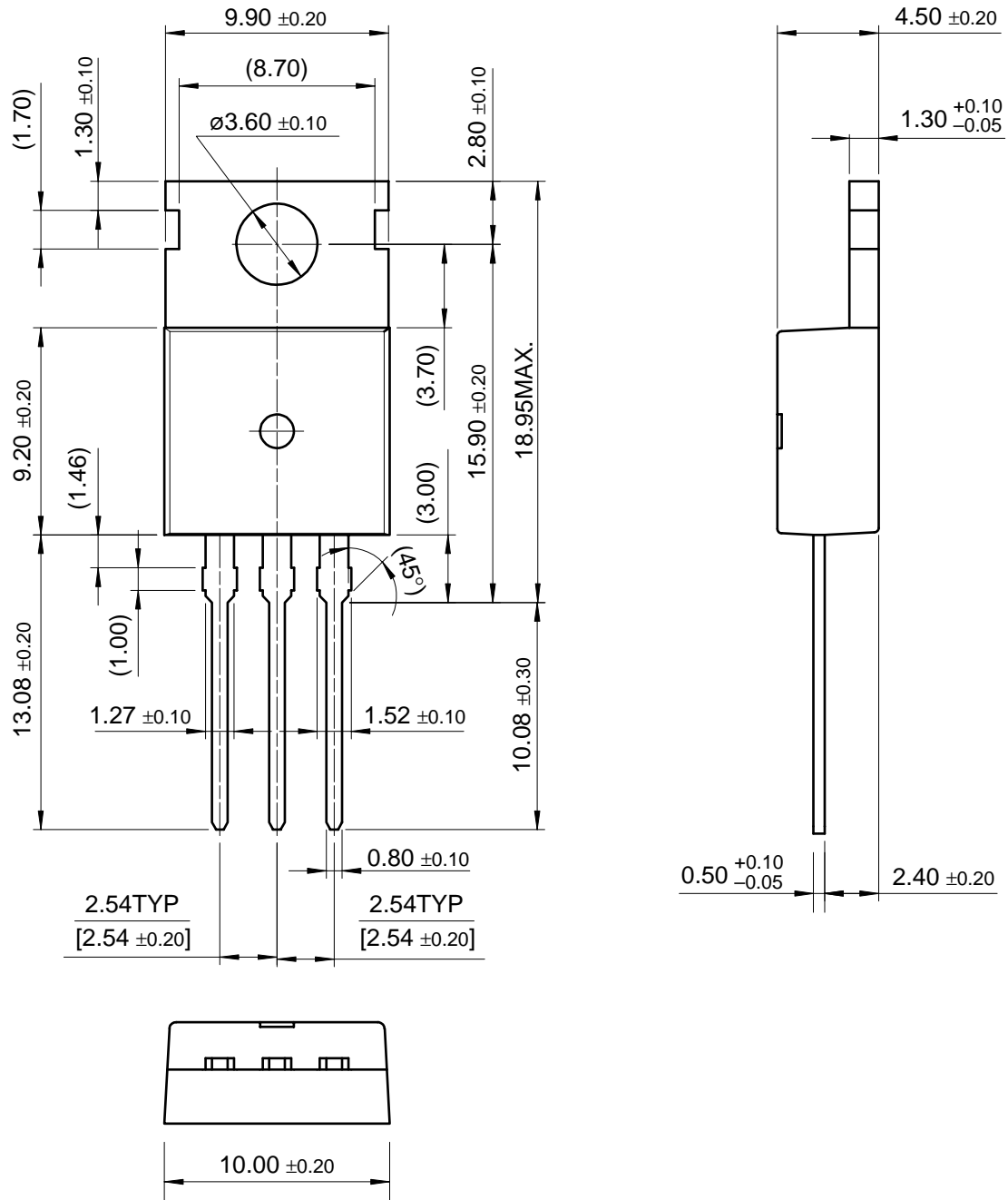
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FAST$^®$	Quiet Series™	
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