EXAR

March 1998-3

FEATURES

- 3 MHz Sampling Rate
- Non-Linearity +1/4 LSB (typ) with S/H
- Low Power CMOS - 100mW (typ)
- Requires NO SAMPLE AND HOLD for signals less than 100 kHz
- Single Supply Voltage (+4 V to +6 V)
- Latch-Up Free
- Monotonic. No Missing Codes

APPLICATIONS

- High Speed Low Power A/D Conversion
- Satellite Operations
- High Energy Physics Research
- Portable Products
- Radar Pulse Analysis
- μP Data Acquisition Systems

GENERAL DESCRIPTION

The MP7683 is a monolithic CMOS 8-bit two step flash Analog-to-Digital Converter designed for applications which demand Low Power Consumption and High Speed digitization (2 MHz sampling rate, 100mW power dissipation). The linearity error is 1/4 LSB (typical), with clock frequency of 2 MHz at a supply voltage of 5 volts.

The MP7683 conversion is done in two segments. The first segment converts the 3 MSBs and consists of eight (8) auto–balanced comparators, latches, an encoder, and four buffer storage registers. The second segment converts the five (5) LSBs and consists of 32 auto-balanced comparators, latches, an encoder, and five buffer storage registers. The MP7683 operates over a wide, full-scale input voltage range from 2.0 volts up to VDD, full-scale.

The overflow bit makes it possible to achieve 9-bit resolution by connecting two MP7683's in series. See Figure 1.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7683 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Shrunk Small Outline (SSOP) and Surface Mount (SOIC) packages.
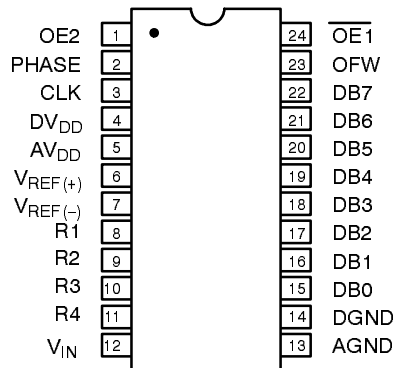
SIMPLIFIED BLOCK DIAGRAM
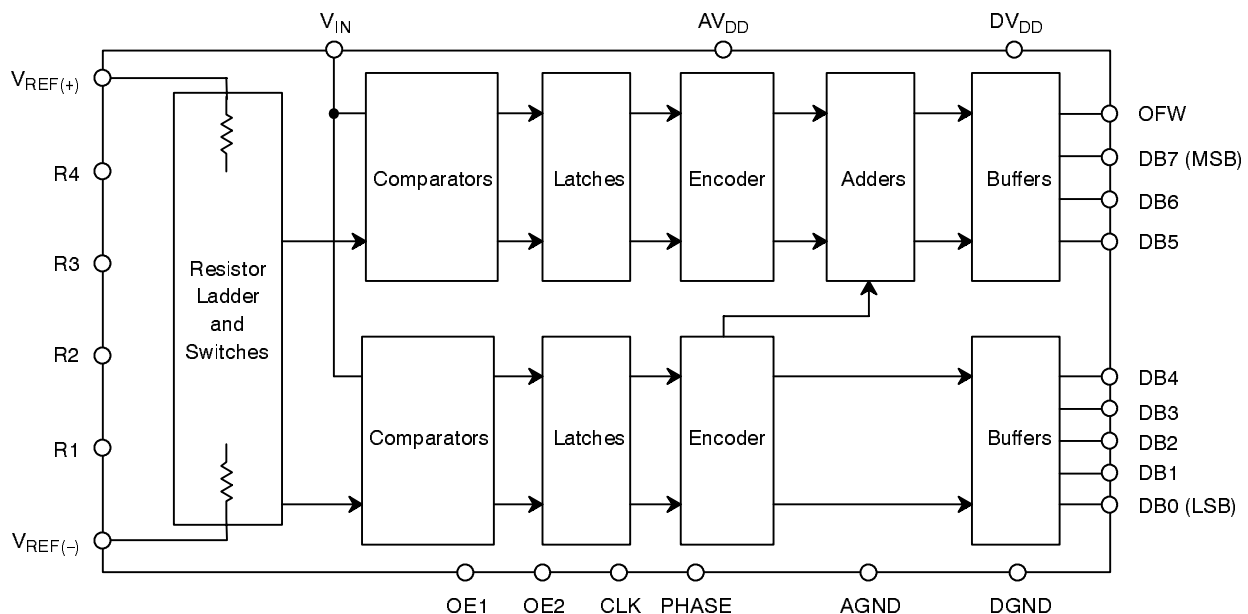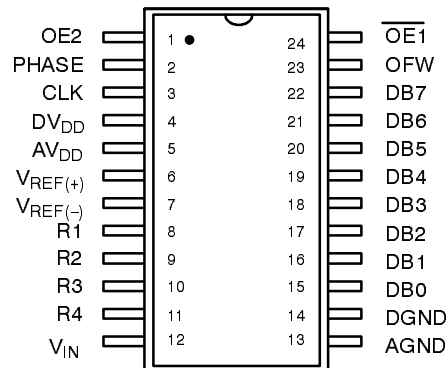
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	−40 to +85°C	MP7683JN	±1 1/4	1 1/4
Plastic Dip	−40 to +85°C	MP7683KN	±3/4	3/4
SOIC	−40 to +85°C	MP7683JS	±1 1/4	1 1/4
SOIC	−40 to +85°C	MP7683KS	±3/4	3/4
SSOP	−40 to +85°C	MP7683JQ	±1 1/4	1 1/4
SSOP	−40 to +85°C	MP7683KQ	±3/4	3/4
Ceramic Dip	−55 to +125°C	MP7683SD*	±1 1/4	1 1/4

*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

	24 Pin CDIP, PDIP (0.600")		24 Pin SOIC (EIAJ, 0.335") / 24 Pin SSOP

Left (CDIP/PDIP):
OE2 — 1, PHASE — 2, CLK — 3, DV$_{DD}$ — 4, AV$_{DD}$ — 5, V$_{REF(+)}$ — 6, V$_{REF(-)}$ — 7, R1 — 8, R2 — 9, R3 — 10, R4 — 11, V$_{IN}$ — 12
24 — $\overline{OE1}$, 23 — OFW, 22 — DB7, 21 — DB6, 20 — DB5, 19 — DB4, 18 — DB3, 17 — DB2, 16 — DB1, 15 — DB0, 14 — DGND, 13 — AGND

24 Pin CDIP, PDIP (0.600")

24 Pin SOIC (EIAJ, 0.335") / 24 Pin SSOP

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	OE2	Output Enable Control 2
2	PHASE	Sampling Clock Phase Control
3	CLK	Clock Input
4	DV$_{DD}$	Power Supply
5	AV$_{DD}$	Power Supply for Analog Circuit
6	V$_{REF(+)}$	Reference Voltage (+) Input
7	V$_{REF(-)}$	Reference Voltage (−) Input
8	R1	1/16th Point of Ladder R Matrix
9	R2	5/16th Point of Ladder R Matrix
10	R3	9/16th Point of Ladder R Matrix
11	R4	13/16th Point of Ladder R Matrix
12	V$_{IN}$	Analog Input

PIN NO.	NAME	DESCRIPTION
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DB0	Data Output Bit 0 (LSB)
16	DB1	Data Output Bit 1
17	DB2	Data Output Bit 2
18	DB3	Data Output Bit 3
19	DB4	Data Output Bit 4
20	DB5	Data Output Bit 5
21	DB6	Data Output Bit 6
22	DB7	Data Output Bit 7 (MSB)
23	OFW	Digital Output Overflow
24	$\overline{OE1}$	Output Enable Control 1

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S = 3$ MHz (50% Duty Cycle), $V_{REF(+)} = 4.1$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Maximum Sampling Rate	F_S	3			3		MHz	For specified accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±1		±1 1/4	LSB	
Integral Non-Linearity	INL			1		1 1/4	LSB	Best Fit Line (Max INL – Min INL) / 2
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±3/4	LSB	
Integral Non-Linearity	INL			1/2		3/4	LSB	Best Fit Line
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	2	4.1	AV_{DD}	2	AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Differential Ref. Voltage[2]	V_{REF}	2		AV_{DD}-AGND	2	AV_{DD}-AGND	V	For specified accuracy
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					2000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance[2]	Z_{IN}		10				MΩ	
Input Capacitance[4]	C_{INA}		50				pF	
Aperture Delay[2]	t_{AP}		55				ns	
Aperture Uncertainty (Jitter)[2]	t_{AJ}		200				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents[5]								V_{IN} = DGND to DV_{DD}
CLK	I_{IN}			±50		±50	µA	
Input Capacitance[2]	C_{IND}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	333					ns	
"High" Time	t_h	166.5					ns	
"Low" Time	t_l	166.5					ns	
Duty Cycle			50				%	

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								$C_{OUT}=15\,pF$
Logical "1" Voltage	V_{OH}	4.6			4.6		V	$I_{LOAD} = -1.0\,mA$
Logical "0" Voltage	V_{OL}			0.4		0.4	V	$I_{LOAD} = 2.0\,mA$
Tristate Leakage	I_{OZ}			± 50		± 50	μA	$V_{OUT}=DGND$ to DV_{DD}
Data Valid Delay[2]	t_{DL}		55				ns	*(See Figure 1.)*
Data Enable Delay[2]	t_{DEN}		20				ns	*(See Figure 2.)*
Data Tristate Delay[2]	t_{DHZ}		26				ns	*(See Figure 2.)*
Output Capacitance[2]	C_O		5				pF	
POWER SUPPLIES								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}[6]	4		6.0	4	6.0	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			20		36	mA	

Notes:
1. *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width ($V_{REF}/256$) is the DNL error. The INL error is the maximum distance (in LSB) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (F_S).*
2. *Guaranteed. Not tested.*
3. *Specified values guarantee functionality. Refer to other parameters for accuracy.*
4. *See V_{IN} input equivalent circuit (Figure 4). Switched capacitor analog input requires driver with low output resistance.*
5. *All inputs have diodes to DV_{DD} and DGND.*
6. *DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply loop.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) . . . . +6.5 V
$V_{REF(+)}$ & $V_{REF(-)}$ . . . . GND –0.5 to V_{DD} +0.5 V
V_{IN} . . . . GND –0.5 to V_{DD} +0.5 V
Digital Inputs . . . . GND –0.5 to V_{DD} +0.5 V
Digital Outputs . . . . GND –0.5 to V_{DD} +0.5 V
Storage Temperature . . . . –65°C to +150°C

Lead Temperature (Soldering 10 seconds) . . . . +300°C
Package Power Dissipation Rating to 75°C
   CDIP, PDIP, SOIC 1000mW
   Derates above 75°C . . . . 14mW/°C
   SSOP 750mW
   Derates above 75°C . . . . 10mW/°C

Notes:
1. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*
2. *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.*
3. *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

DEVICE OPERATION

Figure 1. shows the timing diagram of the MP7683 8-bit Flash Converter. A reference voltage is applied between the $V_{REF(+)}$ and $V_{REF(-)}$ which drives 256 resistors and switches. The reference voltages drive the inverting inputs of comparators. There are four control lines: Clock, $\overline{OE1}$, OE2, and Phase. The Phase line determines the polarity of the clock.

Figure 2. shows waveforms with the phase line high and low. With 0 = 1, the "sample" occurs during the high period of the clock cycle and the "auto-balance" occurs during the low period of the clock. The "sample" is queued and pipelined through a series of registers and latches. It appears at the output after 2 clock periods and time delay (t_{DL}). After the sample is acquired the data is valid for every clock period. The $\overline{OE1}$ will independ-

ently disable DB0 through DB7 when it is in a high state. CE2 will independently disable DB0 through DB7 and the OFW buffers when it is in a low state. The Truth Table (*Table 1.*) summarizes this effect.

$\overline{OE1}$	OE2	DB7-DB0	OFW
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

Table 1. Truth Table
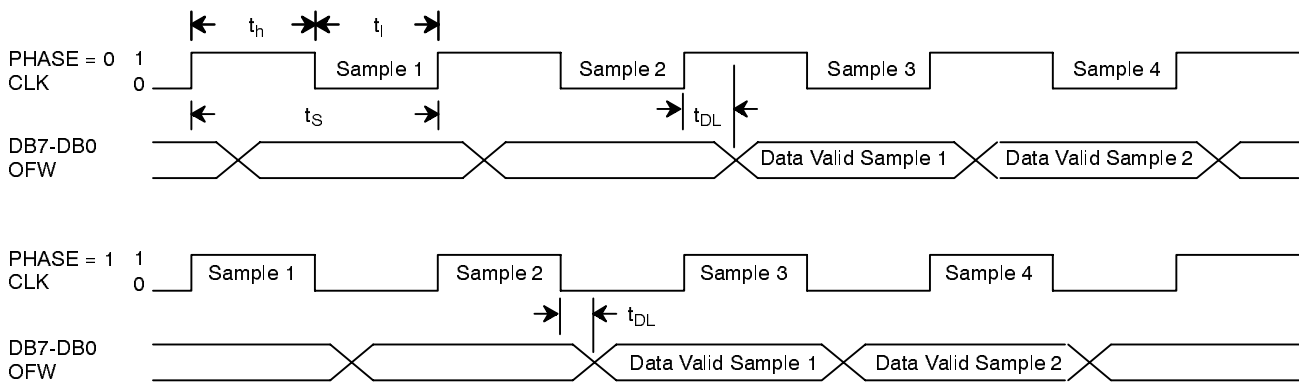
Figure 1. Timing Diagram
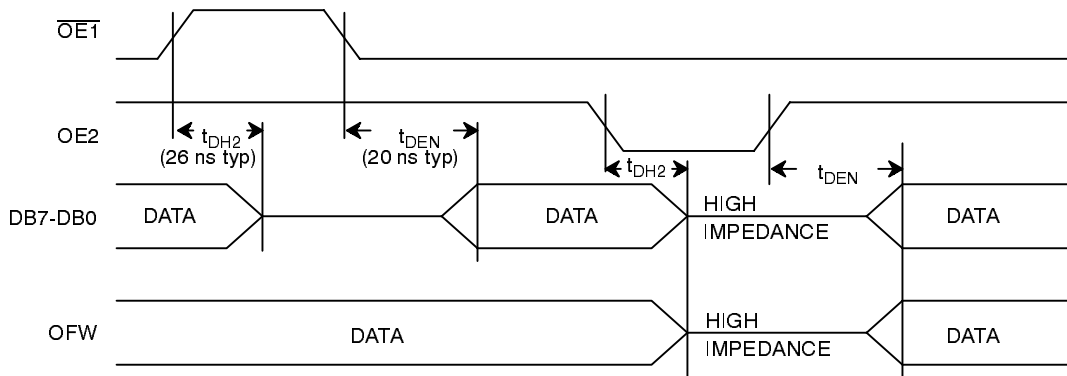
Figure 2. Output Enable and Disable Timing Diagram
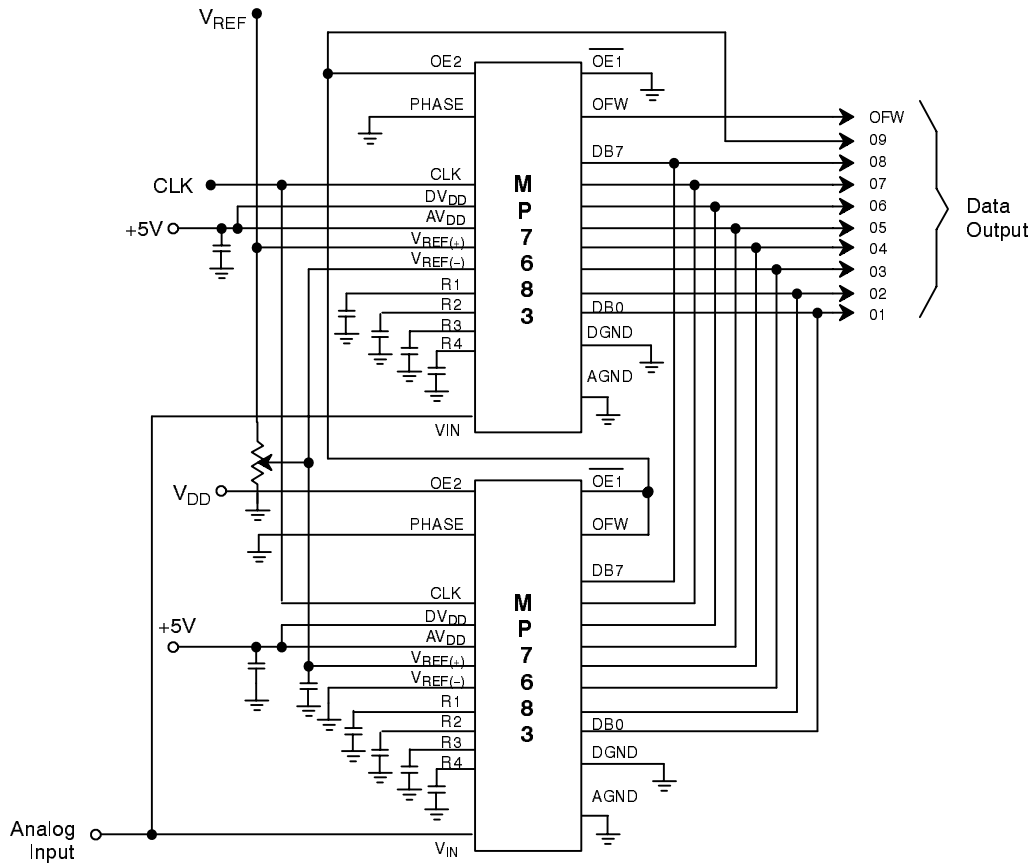
Figure 3. MP7683 9-Bit Resolution Configuration
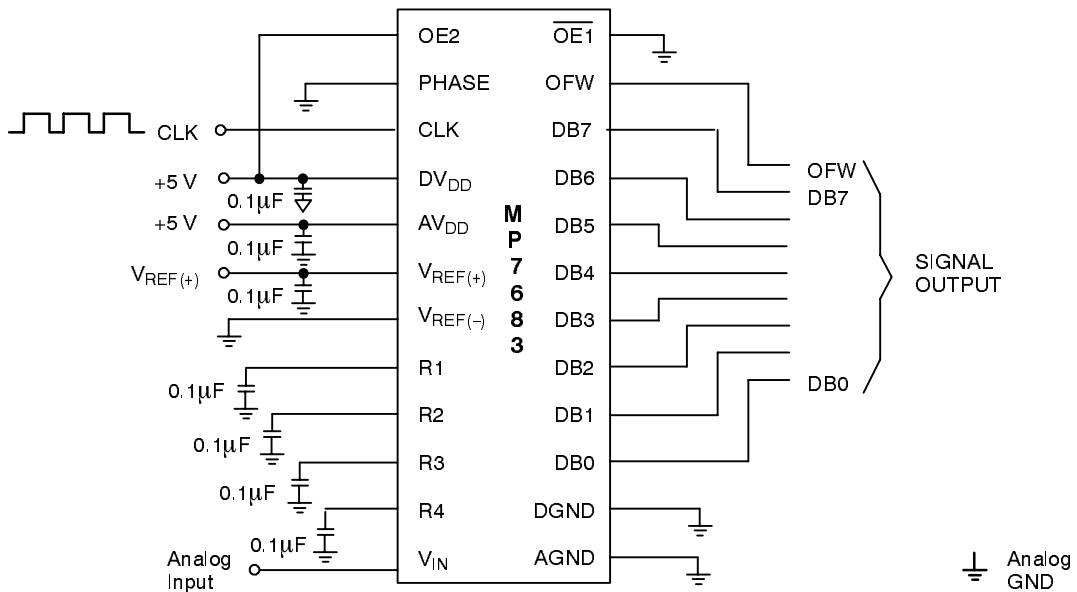
Figure 4. MP7683 Typical Connections

APPLICATION NOTES:

The following information will be useful in maximizing the performance of the MP7683.

1. This device may be susceptible to latch-up. All signals must not exceed AV_{DD} or AGND, or DV_{DD} or DGND at any time. Digital Supply (DV_{DD} & AV_{DD}) must be applied before all other signals to avoid a latch-up condition.

2. The design of a PC layout and assembly will seriously affect the accuracy of the MP7683. Use of wire wrap is not recommended.

3. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.

4. The analog input should be driven with a buffer op amp ($Z_{OUT} \leq 50\ \Omega$).

5. The use of a large shield plane is highly recommended, connected only at one point and connected to virtual ground. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.

6. The power supplies and reference voltages should be decoupled with ceramic (0.01 to 0.1 μF) and tantalum (10μF) capacitors as close to the device as possible.

7. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.
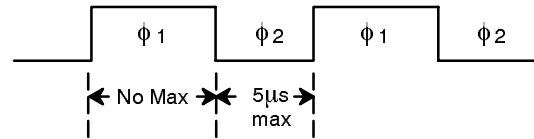
a. When at 50% Duty Cycle, the minimum clock rate is 100 kHz.
b. When at non-50% Duty Cycle, the minimum clock rate may be DC as long as 2 is kept to less than 5 μs.

8. To avoid a possible latch-up condition, power should be applied before any input signal is connected.
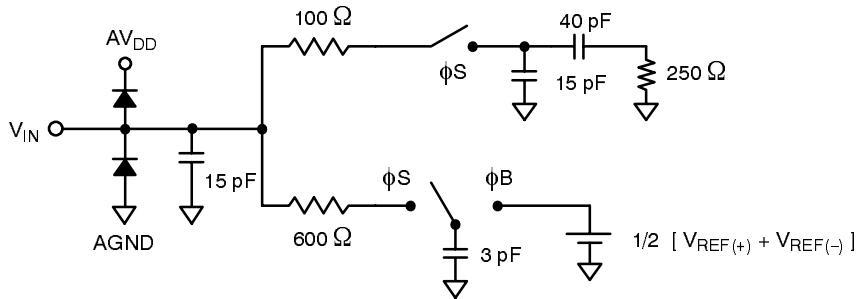
Figure 5. Analog Input Equivalent Circuit

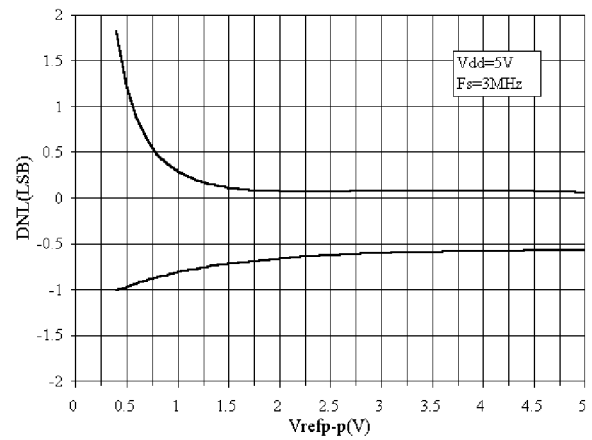**PERFORMANCE CHARACTERISTICS**
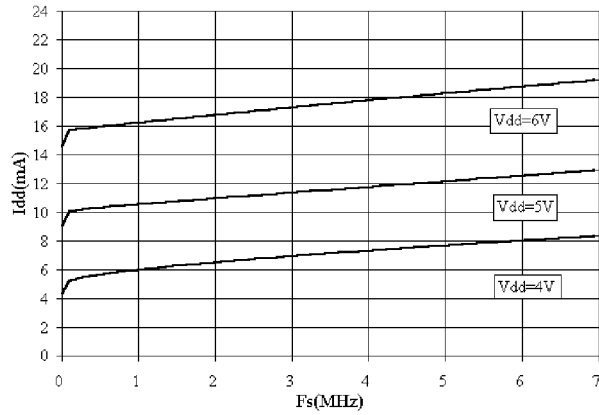
Graph 5. Supply Current vs. Sampling Frequency
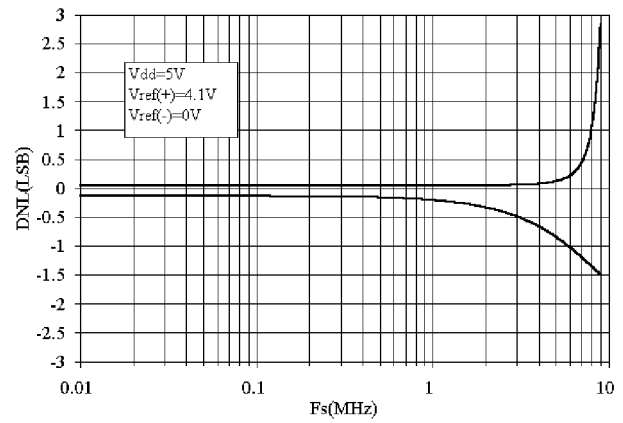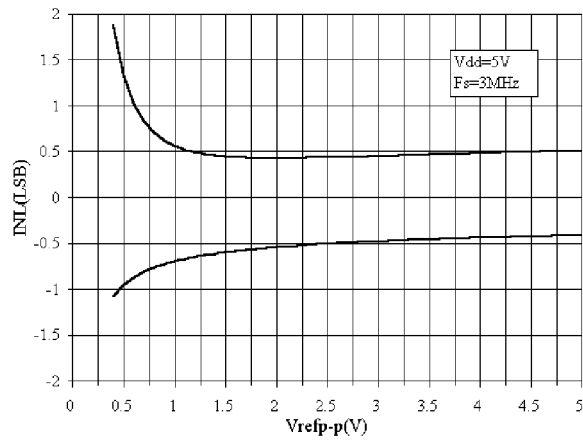

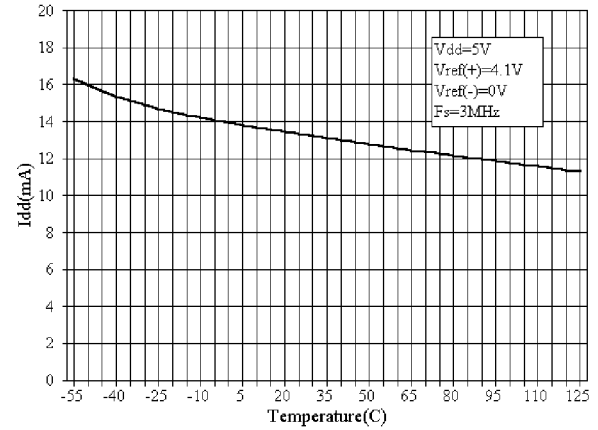**Graph 6. DNL vs. Sampling Frequency**
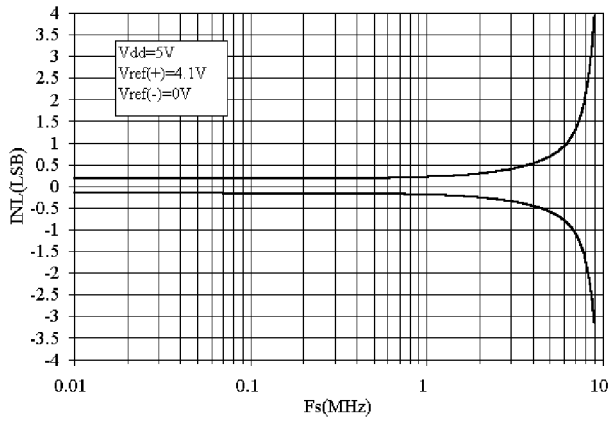
Graph 1. INL vs. Sampling Frequency

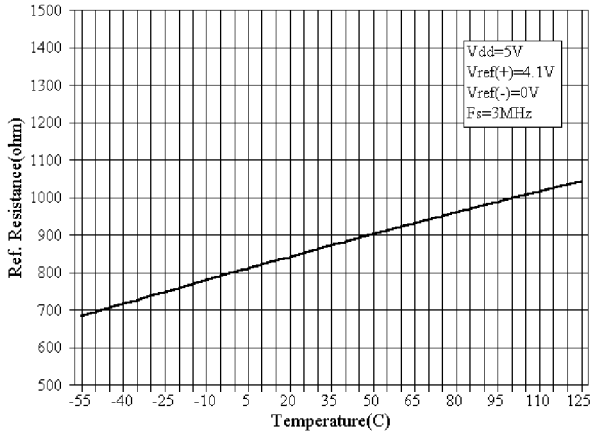**Graph 2. DNL vs. Reference Voltage**

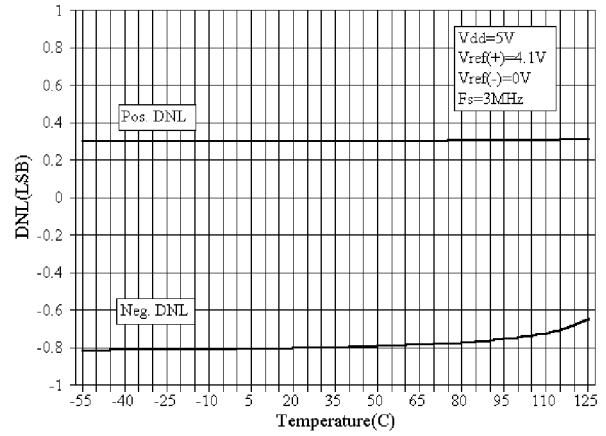**Graph 3. INL vs. Reference Voltage**

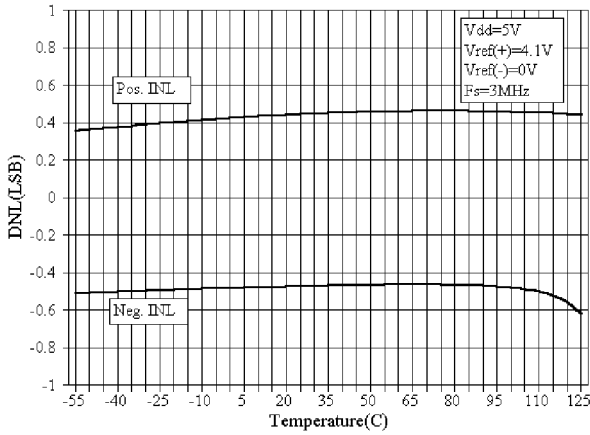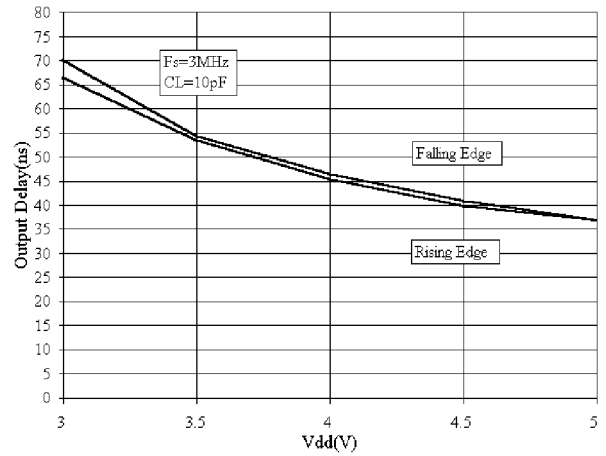**Graph 4. Supply Current vs. Temperature**

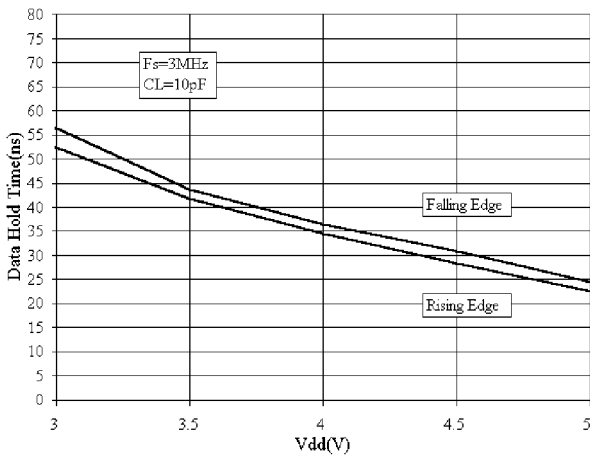**Graph 7. Reference Resistance vs. Temperature**

Graph 8. DNL vs. Temperature
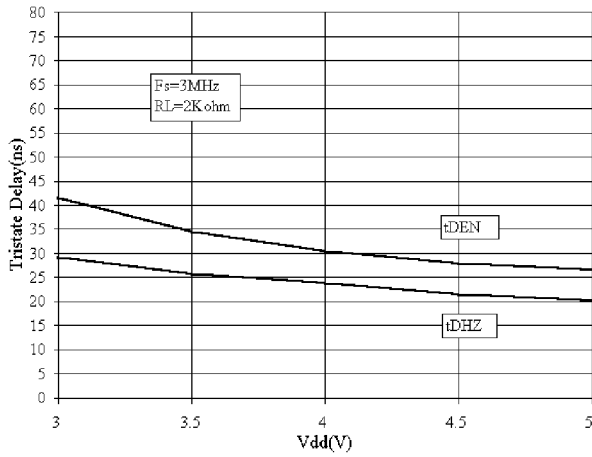

Graph 9. INL vs. Temperature

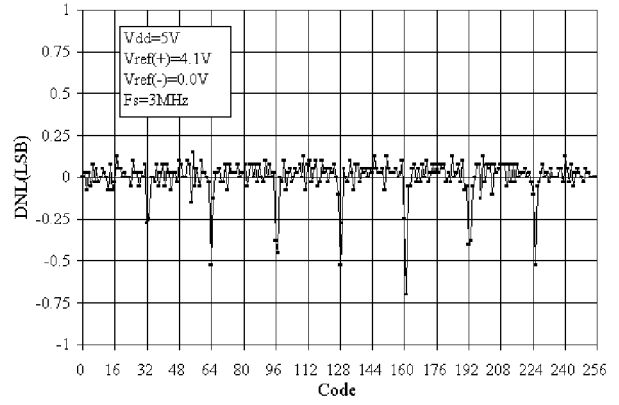**Graph 10. Output Delay vs. Supply Voltage**

Graph 11. Data Hold Time vs. Supply Voltage
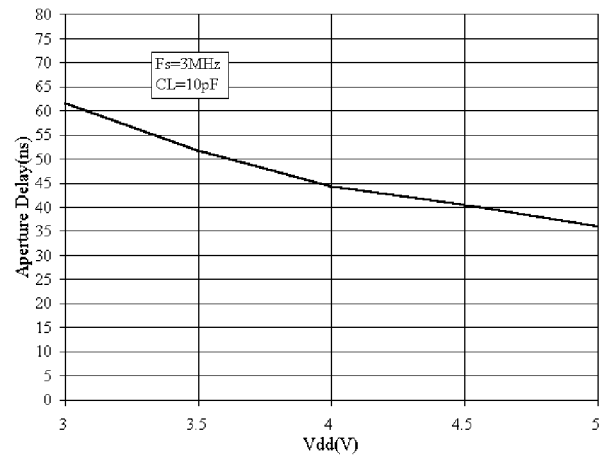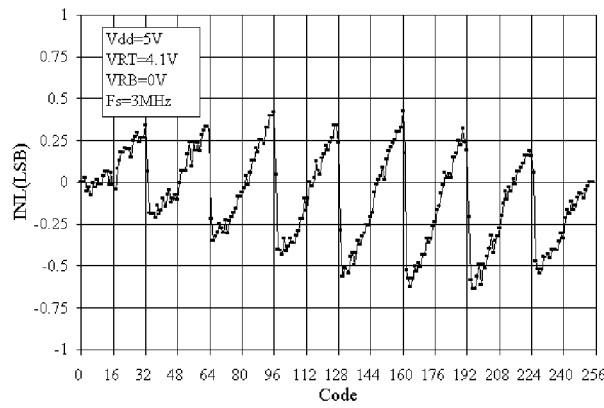

Graph 12. Aperture Delay vs. Supply Voltage

**Graph 13. Tristate Enable Delay
vs. Supply Voltage**

Graph 14. DNL Error Plot

Graph 15. INL Error Plot