Micro Linear

ML65245**/ML65L245*

High Speed Octal Buffer Transceivers

GENERAL DESCRIPTION

The ML65245 and ML65L245 are non-inverting octal transceivers. The high operating frequency (50MHz driving a 50pF load) and low propagation delay (ML65245 – 1.7ns, ML65L245 – 2ns) make them ideal for very high speed applications such as processor bus buffering and cache and main memory control.

These transceivers use a unique analog implementation to eliminate the delays inherent in traditional digital designs. Schottky clamps reduce under and overshoot, and special output driver circuits limit ground bounce. The ML65245 and ML65L245 conform to the pinout and functionality of the industry standard FCT245 and are intended for applications where propagation delay is critical to the system design.

Note: This part was previously numbered ML6580.

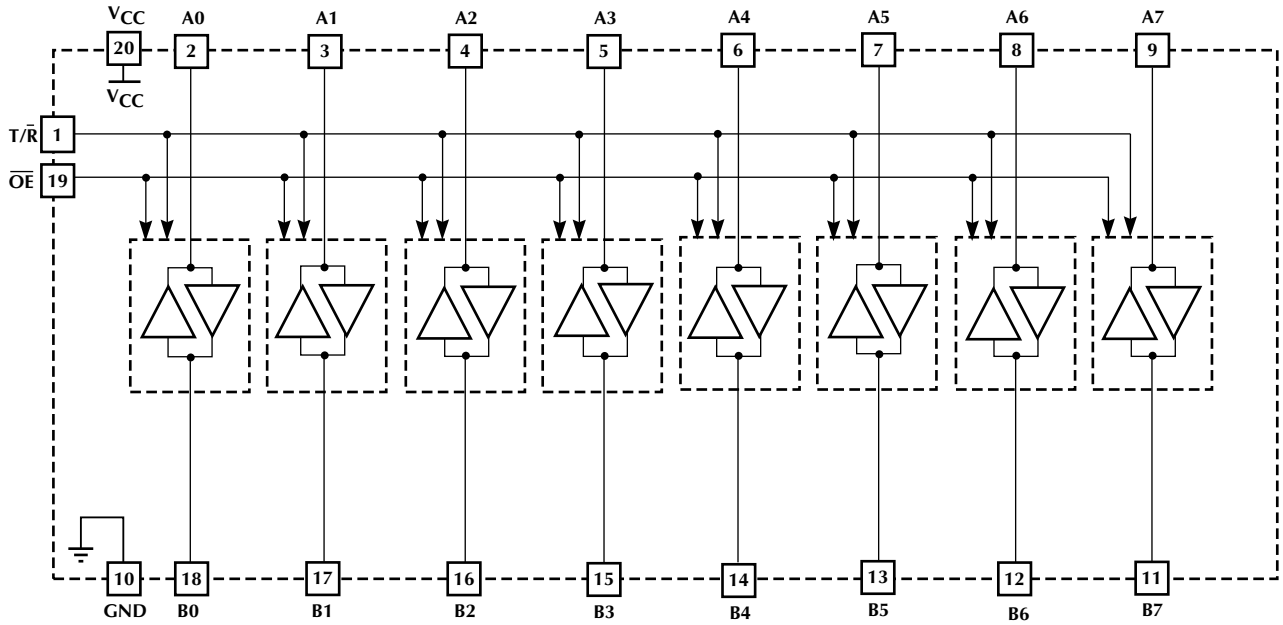
FEATURES

- Low propagation delay — 1.7ns ML65245
  2.0ns ML65L245
- Fast 8-bit TTL level transceiver with three-state capability on the output
- TTL compatible input and output levels
- Schottky diode clamps on all inputs to handle undershoot and overshoot
- Onboard schottky diodes minimize noise
- Reduced output swing of 0 – 4.1 volts
- Ground bounce controlled outputs, typically less than 400mV
- Industry standard FCT245 type pinout
- Applications include high speed cache memory, main memory, processor bus buffering, and graphics cards

** This Product Is End Of Life As Of August 1, 2000

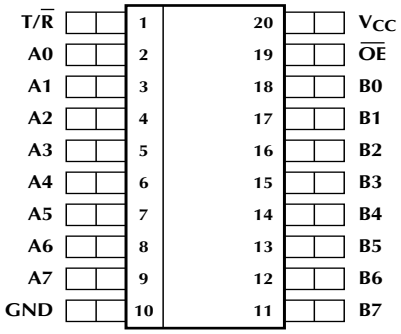
* This Product Is Obsolete

BLOCK DIAGRAM



PIN CONFIGURATION

20-Pin SOIC, QSOP



TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
Ai	I/O	Data Bus A
Bi	I/O	Data Bus B
T/$\overline{R}$	I	Direction select
$\overline{OE}$	I	Output Enable
GND	I	Signal Ground
V_{CC}	I	+ 5V supply

FUNCTION TABLE

$\overline{OE}$	T/$\overline{R}$	A	B	Function
H	X	Z	Z	Disable
L	L	Output	Input	Bus B to Bus A
L	H	Input	Output	Bus A to Bus B

L = Logic Low
H = Logic High
X = Don't Care
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

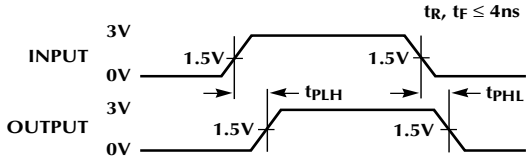
V_{CC} ..... –0.3V to 7V
DC Input voltage ..... –0.3V to V_{CC} + 0.3V
AC Input voltage (< 20ns) ..... –3.0V
DC Output voltage ..... –0.3V to V_{CC} + 0.3V
Output sink current (per pin) 120mA
Storage temperature ..... –65°C to 150°C
Junction temperature ..... 150°C
Thermal Impedance (θ_{JA})
SOIC ..... 96°C/W
QSOP ..... 100°C/W

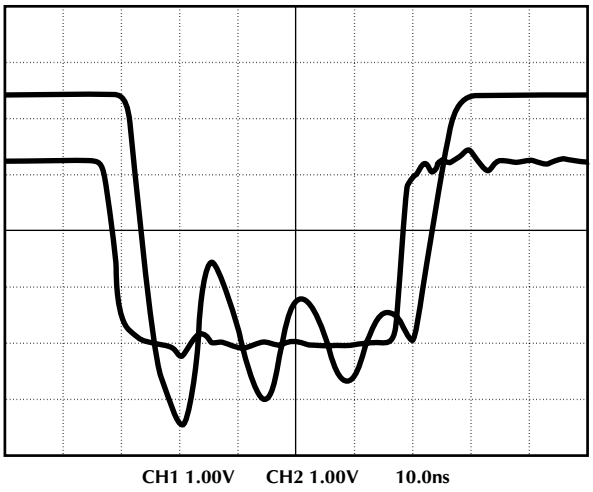
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: V_{CC} = 5.0 ± 5%V, T_A = 0°C to 70°C (Note 1)

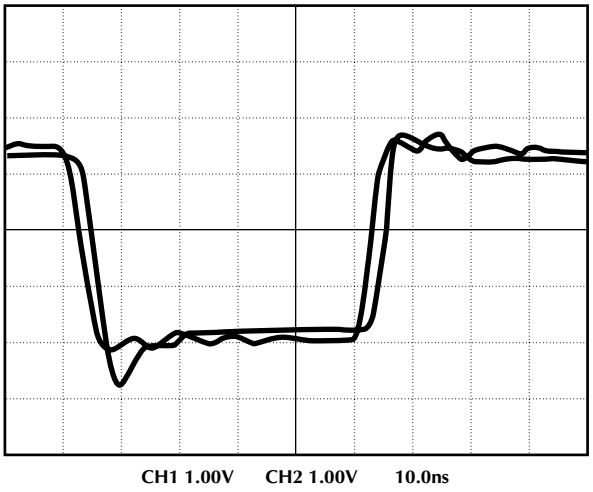
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = 500ý)							
t_{PLH}, t_{PHL}	Propagation delay	Ai to/from Bi (Note 2)	ML65245		1.4	1.7	ns
			ML65L245		1.6	2.0	ns
t_{OE}	Output enable time $\overline{OE}$, T/$\overline{R}$ to Ai/Bi				10	15	ns
t_{OD}	Output disable time $\overline{OE}$, T/$\overline{R}$ to Ai/Bi					10	ns
C_{IN}	Input Capacitance				8		pF
DC ELECTRICAL CHARACTERISTICS (unless otherwise stated C_{LOAD} = 50pF, R_{LOAD} = □)							
V_{IH}	Input high voltage	Logic HIGH		2.0			V
V_{IL}	Input low voltage	Logic LOW				0.8	V
I_{IH}	Input high current	Per pin, V_{IN} = 3V	ML65245		0.5	1.5	mA
			ML65L245		0.3	0.5	mA
I_{IL}	Input low current	Per pin, V_{IN} = 0V	ML65245		2.4	3.5	mA
			ML65L245		0.8	1.0	mA
I_{HI-Z}	Three-state output current	V_{CC} = 5.25V, 0 < V_{IN} < V_{CC}				5	µA
I_{OS}	Short circuit current	V_{CC} = 5.25V, V_O = GND (Note 3)		–60		–225	mA
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = 18mA			–0.7	–1.2	V
V_{OH}	Output high voltage	V_{CC} = 4.75V, I_{OH} = 100µA (Notes 4 & 5)		2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V, I_{OL} = 25mA (Notes 4 & 5)				0.6	V
V_{OFF}	V_{IN} – V_{OUT} per buffer	V_{CC} = 4.75V (Note 4)	ML65245	0	100	200	mV
			ML65L245	0	200	300	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = 5.25V, f = 0Hz, Inputs/outputs open			55	80	mA

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: One line switching, see Figure 3, t_{PLH}, t_{PHL} versus C_L.
Note 3: Not more than one output should be shorted for more than a second.
Note 4: This is a true analog buffer. In the linear region, the output tracks the input with an offset (V_{OFF}). For V_{OH}, V_{IN} = 2.7V. V_{IN} = 2.6V for the ML65245 and 2.7 for the ML65L425. $V_{OH\ MIN}$ includes V_{OFF}. For V_{OL}, V_{IN} = 0V, $V_{OL\ MAX}$ includes V_{OFF}
Note 5: See Figure 2 for I_{OH} versus V_{OH} and I_{OL} versus V_{OL} data.





74FCT245



ML65245

Figure 1. Ground Bounce Comparison, Four Outputs Switching into 50pF Loads.

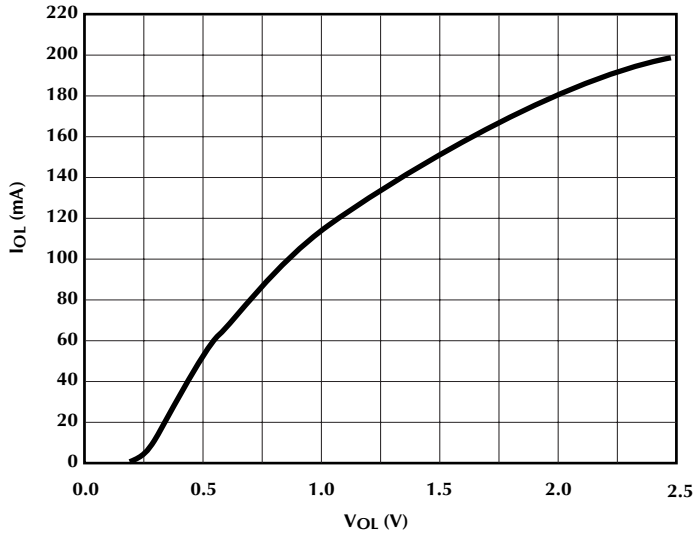


Figure 2a. Typical V_{OL} Versus I_{OL} for One Buffer Output.

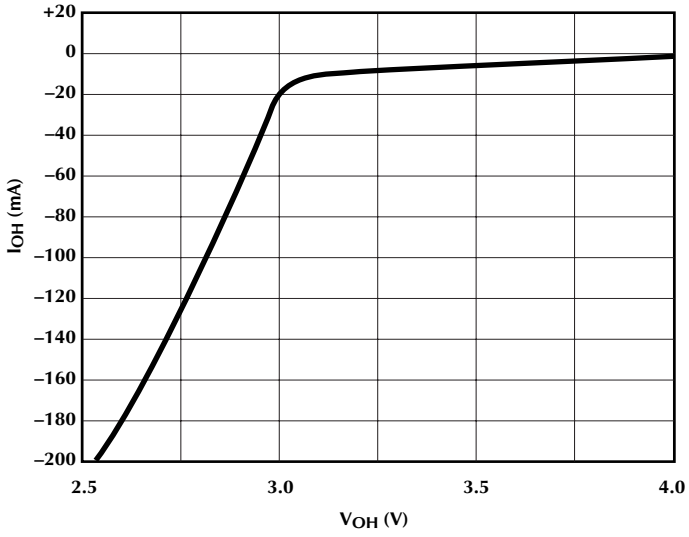


Figure 2b. Typical V_{OH} Versus I_{OH} for One Buffer Output.

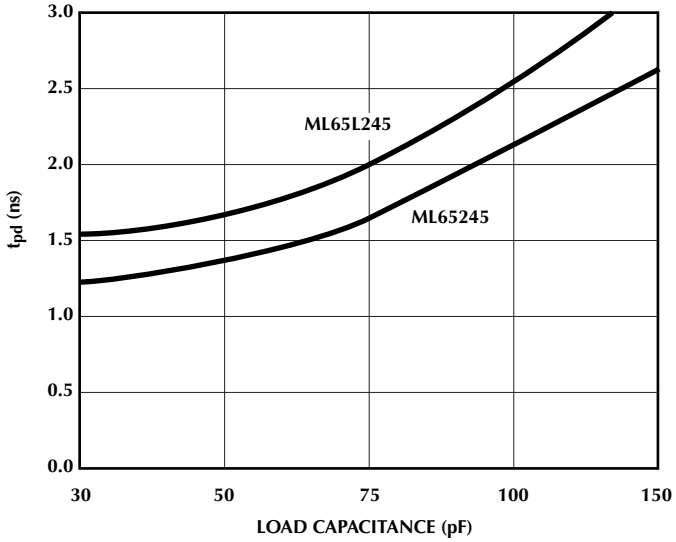


Figure 3. Propagation Delay (t_{PLH}, t_{PHL}) Versus Load Capacitance, One Output Switching.

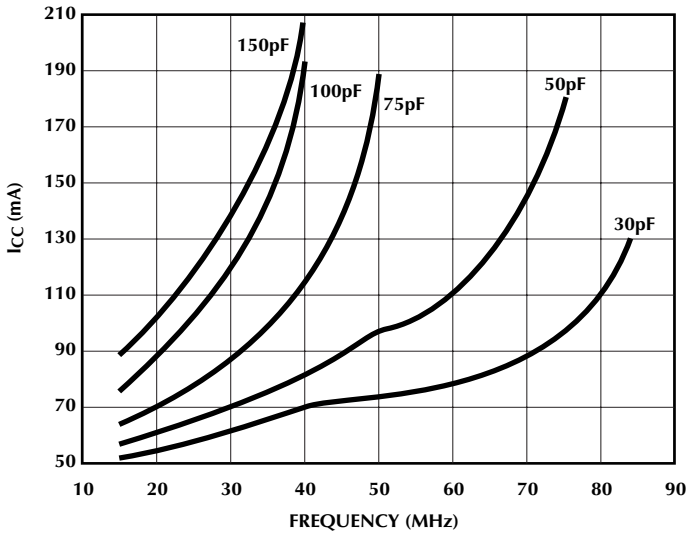


Figure 4. I_{CC} Versus Frequency for Various Load Capacitances, Four Outputs Switching.

FUNCTIONAL DESCRIPTION

The ML65245 and ML65L245 are very high speed non-inverting transceivers with three-state outputs which are ideally suited for bus-oriented applications. They provide a low propagation delay by using an analog design approach (a high speed unity gain buffer), as compared to conventional digital approaches. The ML65245 and ML65L245 follow the pinout and functionality of the industry standard FCT245 series of transceivers and are intended to replace them in designs where the propagation delay is a critical part of the system design considerations. The ML65245 and ML65L245 are capable of driving load capacitances several times larger than their input capacitance. They are configured so that signals pass from Ai to Bi, or from Bi to Ai, depending on the state of the T/$\overline{R}$ pin. All of the signal lines can be made high impedance via the $\overline{OE}$ pin.

These unity gain analog buffers achieve low propagation delays by having the output follow the input with a small offset. The output rise and fall times will closely match those of the input waveform. All inputs and outputs have Schottky clamp diodes to handle undershoot or overshoot noise suppression in unterminated applications. All outputs have ground bounce suppression (typically < 400mV), high drive output capability with almost immediate response to the input signal, and low output skew.

The I_{OL} current drive capability of a buffer/line driver is often interpreted as a measure of its ability to sink current in a dynamic sense. This may be true for CMOS buffer/line drivers, but it is not true for the ML65245 and ML65L245. This is because the their sink and source current capability depends on the voltage difference between the output and the input. The ML65245 can sink or source more than 100mA to a load when the load is switching due to the fact that during the transition, the difference between the input and output is large. I_{OL} is only significant as a DC specification, and is 25mA.

ARCHITECTURAL DESCRIPTION

Until now, buffer/line drivers have been implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these CMOS buffers has managed to drive a 50pF load capacitance with a delay of 3.2ns. Micro Linear has produced an octal transceiver with a delay less than 1.7ns by using a unique circuit architecture that does not require cascaded logic gates. The ML65245 uses a feedback technique to produce an output that follows the input. If the output voltage is not close to the input, then the feedback circuitry will source or sink enough current to the load capacitance to correct the discrepancy.

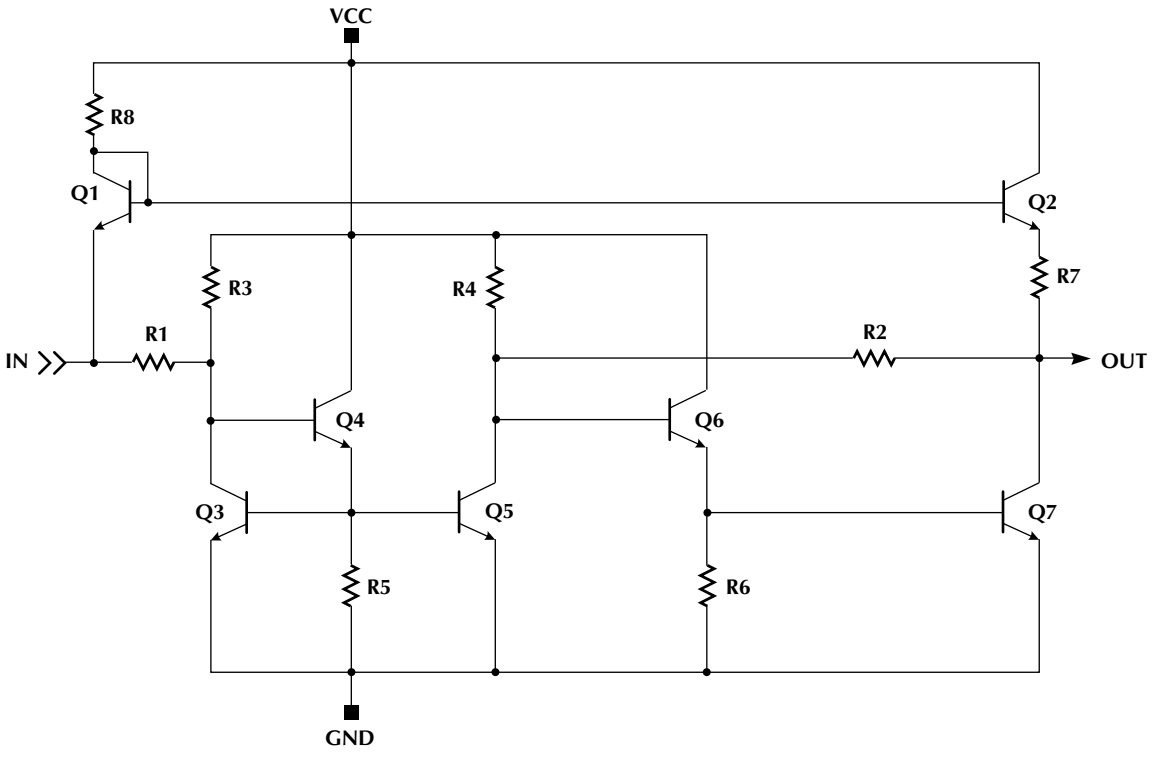


Figure 5. One buffer cell of the ML65245

The basic architecture of the ML65245 is shown in Figure 5. It is implemented on a 1.5µm BiCMOS process. However, in this particular circuit, all of the active devices are NPNs — the fastest devices available in the process.

In this circuit, there are two paths to the output. One path sources current to the load capacitance when the signal is asserted, and the other path sinks current from the output when the signal is negated.

The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2, and the bias resistor R8. It sources current to the output through the 75ý resistor R7 which is bypassed by another NPN (not shown) during fast input transients. The negation path is a current differencing op amp connected in a follower configuration. The active components in this amplifier are transistors Q3-Q7. R3-R6 are bias resistors, and R1 and R2 are the feedback resistors. The key to understanding the operation of the current differencing op amp is to know that the currents in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by β squared to the collector of Q7, closing the loop. The larger the discrepancy between the output and input, the larger the feedback current, and the harder Q7 sinks current from the load capacitor.

A number of MOSFETs are not shown in Figure 5. These MOSFETs are used to three-state dormant buffers. For instance, the feedback resistors R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines they are connected to. Similarly, there is a PMOS in series with R8 that is normally on but shuts off for disable. Other MOSFETs have been included to ensure that disabled buffers consume no power.

TERMINATION

R7 in Figure 5 also acts as a termination resistor. This 75ý resistor is in series with the output and therefore helps suppress noise caused by transmission line effects such as reflections from mismatched impedances. System designers using CMOS transceivers commonly have to use external resistors in series with each transceiver output to suppress this noise. Systems using the ML65245 or ML65L245 may not have to use these external resistors.

APPLICATIONS

There are a wide variety of needs for extremely fast buffers in high speed processor system designs like Pentium, PowerPC, Mips, Sparc, Alpha and other RISC processors. These applications are either in the cache memory area or the main memory (DRAM) area. In addition, fast buffers find applications in high speed graphics and multimedia applications. The high capacitive loading due to multiplexed address lines on the system bus demand external buffers to take up the excess drive current. The needed current to skew the transitions between rise and fall times must be done without adding excessive propagation delay. The ML65245 and ML65L245 are equipped with Schottky diodes to clean up ringing from overshoot and undershoot caused by reflections in unterminated board traces.

BUFFERING MAIN MEMORY

An example main memory application for the Intel PCI chipset with the Pentium processor is shown in Figure 6. This is only intended as a general reference. For details please refer to the appropriate Intel documentation. This system has a 66MHz host processor and a 33MHz main (DRAM) memory bus. The main memory row and column addresses (RAS & CAS) and write enable ($\overline{WE}$) signals are provided by the PCMC chip (PCI Cache and Memory Controller) device. The DRAM SIIMMs put a heavy load on the PCMC and must be buffered. Three buffered copies of the address signals and write enable are required to drive the six row array. The ML65245 provides the buffered signals and gives extra margin to be able to use slower memory modules instead of the normally required 50/70ns. The burst read (page-hit) performance is typically 7-4-4-4 at 66MHz for 70ns DRAMs or 6-3-3-3 at 66MHz for 50ns DRAMs. This usually translates to significantly higher costs. With the speed improvement offered by the ML65245, a 6-3-3-3 burst with 60ns DRAMs may be achievable. The extra margin comes from the 1.5ns propagation delay of the buffer. External resistor arrays are not necessary. This becomes even more of an issue in future PCI systems which may operate at 80MHz and beyond.

This kind of main memory application for the ML65245 could potentially extend to other kinds of processor systems which do not require latched buffering. Figure 7 shows a main memory design example with the ML65245 for the Mips R4X00 RISC processor based system without secondary cache. The faster propagation delay essentially translates to a faster main memory access.

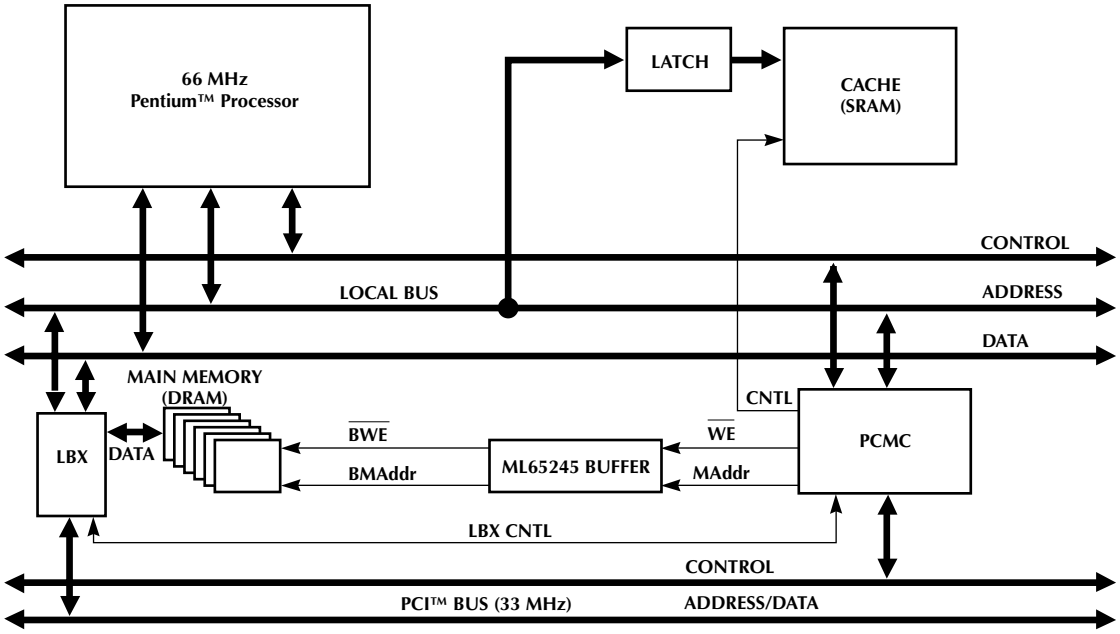


Figure 6. ML65245 in a main memory application for a Pentium based system. The high drive and low propagation delay are essential to buffer the write enable and memory addresses to the main memory SIIMMs.

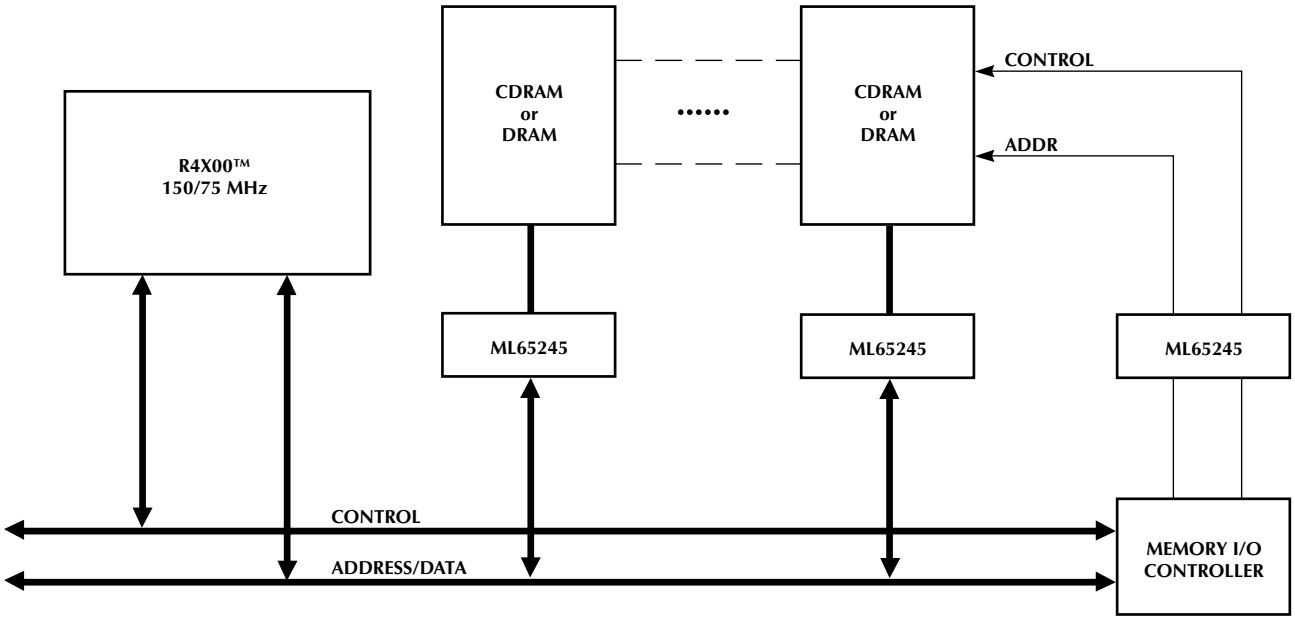


Figure 7. The ML65245 in a non-cache, main memory RISC application. The main memory could be DRAM or Cache DRAM. The ML65245 can be used as a data I/O transceiver as well as an address buffer, as shown above.

APPLICATION 2

BUFFERING CACHE MEMORY

With the advent of higher power operating systems like Windows NT, NeXT Step, Windows, OS/2 Warp, etc., RISC processor designs such as the Mips R4000 series are gaining momentum. In these systems the interface to secondary cache has a critical path in the address and bus control pins. As shown in Figure 8, any propagation delay time saved in the buffer translates to a slower SRAM access requirement and is therefore less expensive. Currently, the secondary cache bus operates at 75MHz.

In order to meet the 13ns cycle time, the SRAM and buffer must meet a total access time of 12ns. With the ML65245, the required SRAM access time is 10ns at 75MHz and 18ns at 50MHz. With the fastest FCT buffer available (3.2ns), the SRAM access time required in the above scenarios would be 8ns and 15ns respectively. This access time difference could mean the difference between using expensive BiCMOS SRAMs versus less expensive CMOS SRAMs.

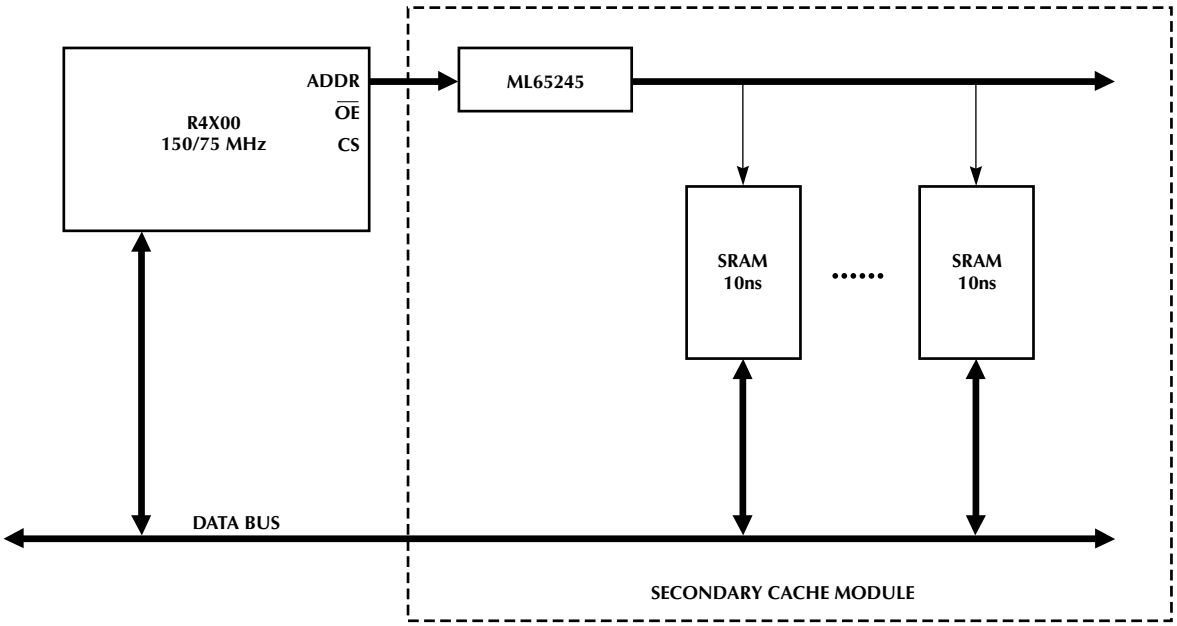


Figure 8. ML65245 in a R4X00 secondary cache application. The address and control signal path is critical and loads the R4X00 output pins. The ML65245 buffer alleviates the load on the R4X00 and because it is fast, slower, less expensive SRAMs can be used.

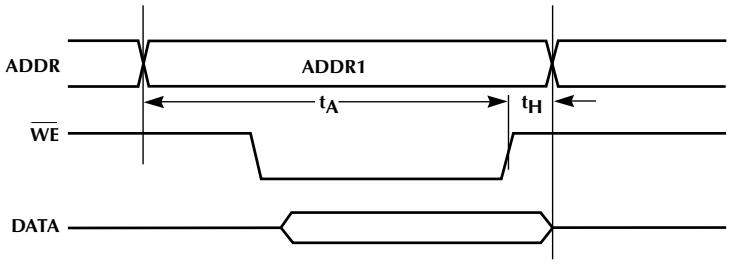
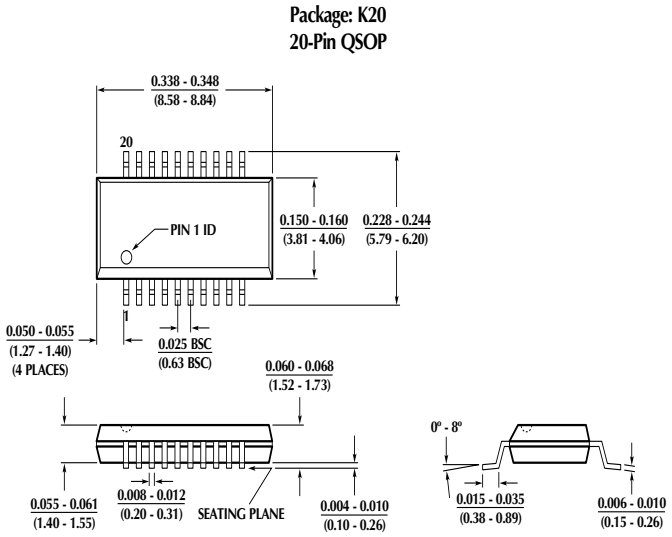


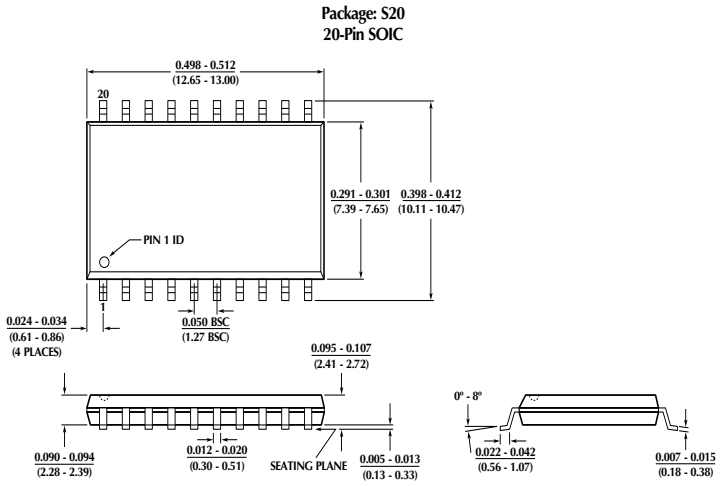
Figure 9. Timing waveform showing address buffer switching rate (t_A + t_H) in a secondary cache module.

PHYSICAL DIMENSIONS inches (millimeters)

Package: K20
20-Pin QSOP



Package: S20
20-Pin SOIC



ORDERING INFORMATION

PART NUMBER	SPEED	TEMPERATURE RANGE	PACKAGE
ML65245CK (EOL)	1.7ns	0°C to 70°C	20-Pin QSOP (K20)
ML65245CS (EOL)	1.7ns	0°C to 70°C	20-Pin SOIC (S20)
ML65L245CK (Obsolete)	2.0	0°C to 70°C	20-Pin QSOP (K20)
ML65L245CS (Obsolete)	2.0	0°C to 70°C	20-Pin SOIC (S20)

Intel, Pentium, PCI are registered trademarks of Intel Corporation. Mips, Alpha and Sparc are registered trademarks of Silicon Graphics, DEC and Sun Microsystems respectively.

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295