

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4000B

gates

Dual 3-input NOR gate and inverter

Product specification
File under Integrated Circuits, IC04

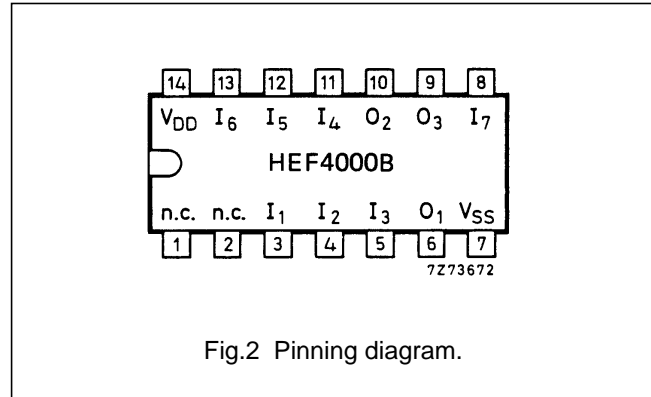
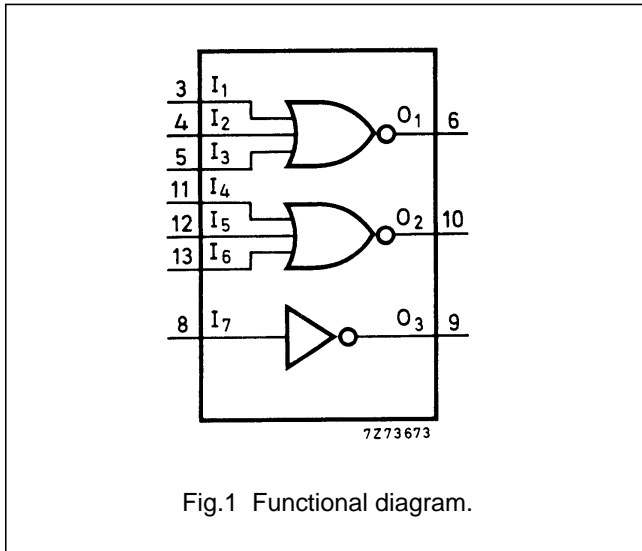
January 1995

Dual 3-input NOR gate and inverter

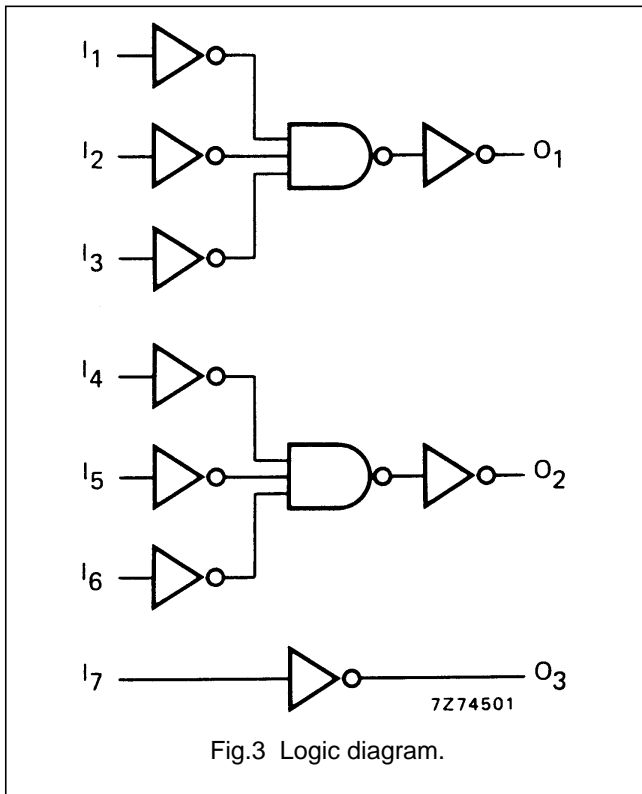
HEF4000B gates

DESCRIPTION

The HEF4000B provides the positive dual 3-input NOR function. A single stage inverting function with standard output performance is also accomplished. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4000BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4000BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4000BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

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HEF4000B gates

DC CHARACTERISTICS

For the single inverter stage (I₇/O₃):

see Family Specifications for input voltages HIGH and LOW (unbuffered stages only).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays I ₁ to I ₆ → O ₁ , O ₂	5	t _{PHL} ; t _{PLH}	70	140	ns	43 ns + (0,55 ns/pF) C _L
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L
	15		30	55	ns	22 ns + (0,16 ns/pF) C _L
I ₇ → O ₃ (unbuffered output)	5	t _{PHL} ; t _{PLH}	45	90	ns	18 ns + (0,55 ns/pF) C _L
	10		25	50	ns	14 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	7 700 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	28 700 f _i + ∑ (f _o C _L) × V _{DD} ²	

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APPLICATION INFORMATION

The following information (Figs 4 to 7) is only for the single inverter stage (I₇/O₃).

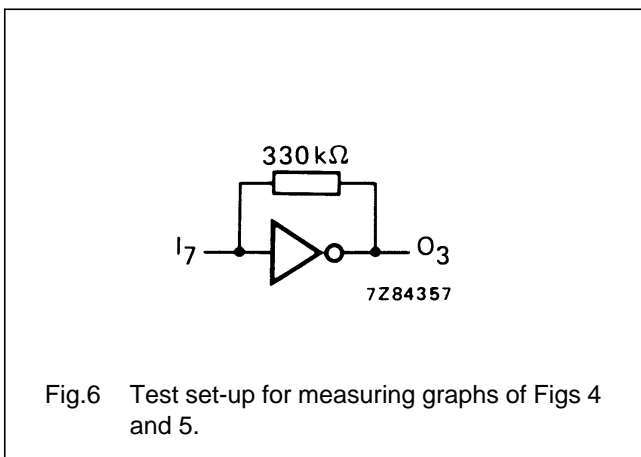
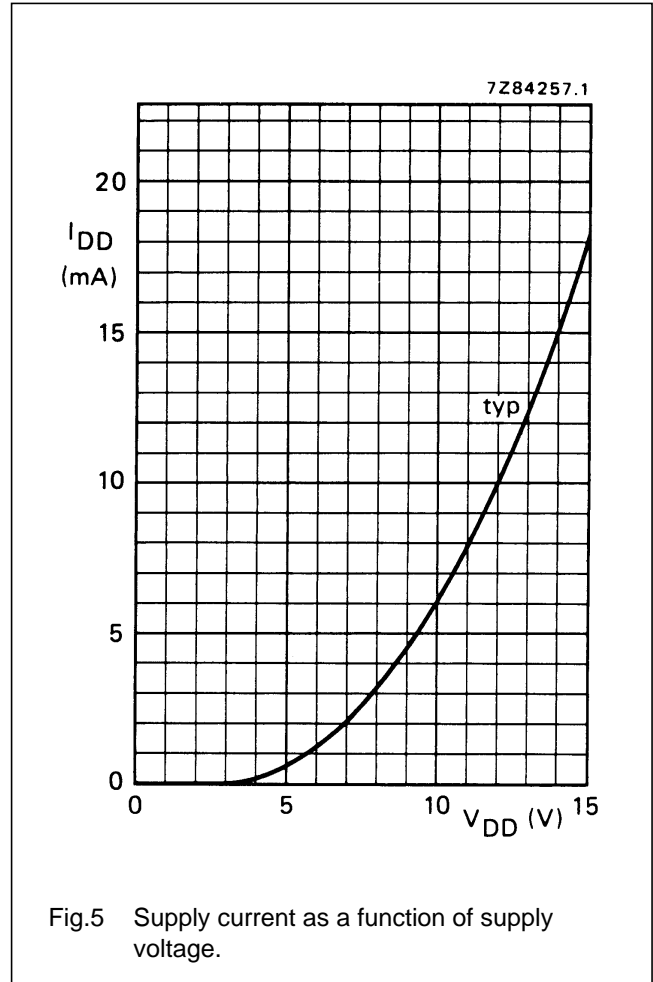
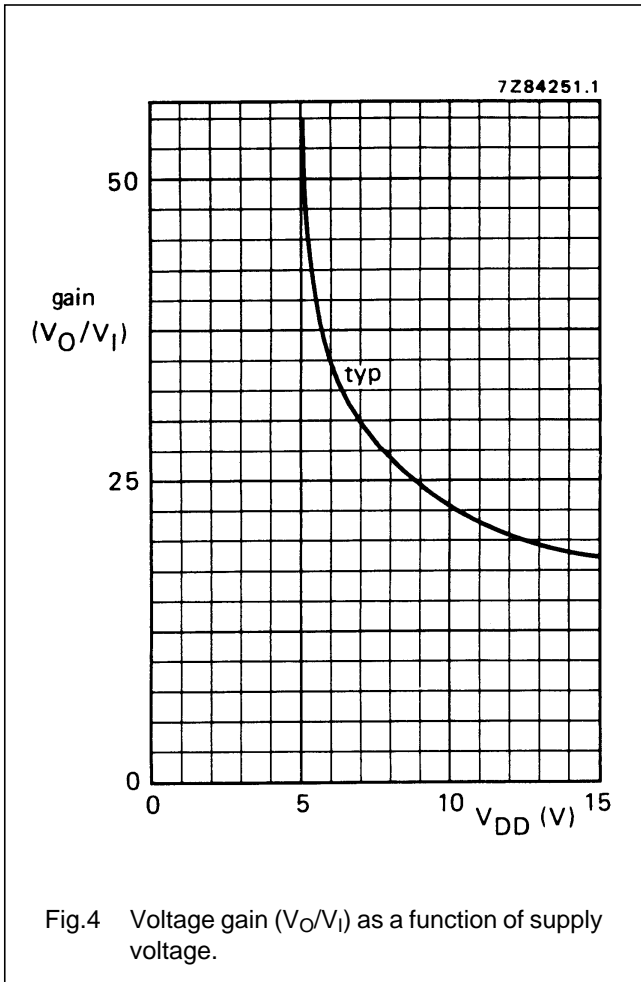


Fig.6 Test set-up for measuring graphs of Figs 4 and 5.

This is also an example of an analogue amplifier using the single inverter stage (I₇/O₃) of the HEF4000B.

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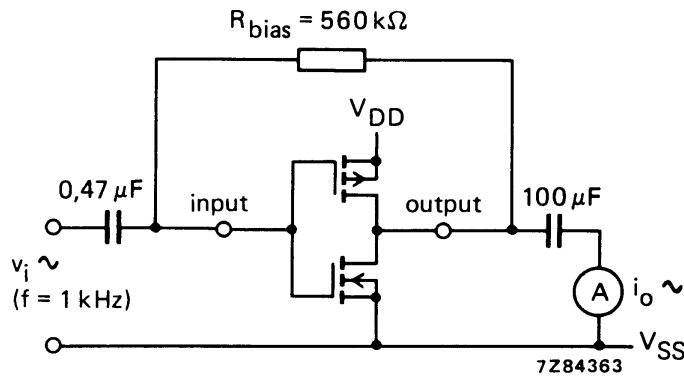
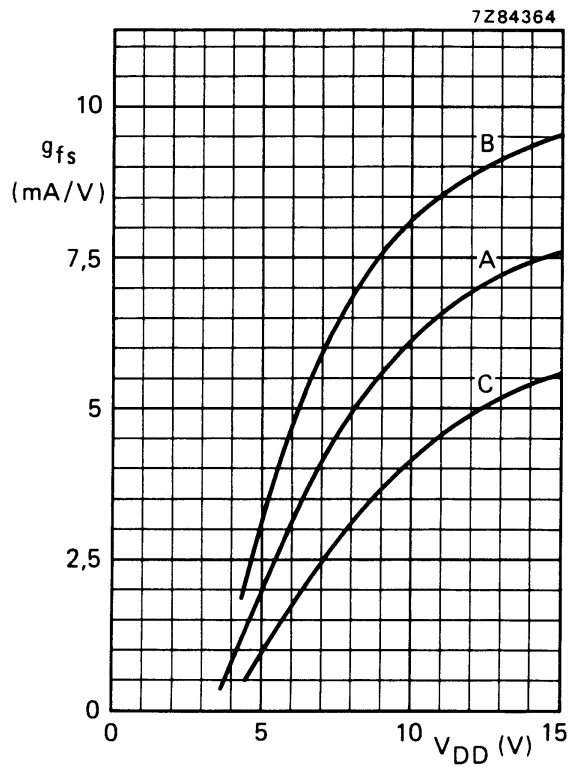


Fig.7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.8).



A: average
 B: average + 2 s,
 C: average - 2 s, in where 's' is the observed standard deviation.

Fig.8 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^\circ\text{C}$.