

TC74VHC175F, TC74VHC175FN, TC74VHC175FT

QUAD D-TYPE FLIP-FLOP WITH CLEAR

The TC74VHC175 is an advanced high speed CMOS QUAD D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These four flip-flops are controlled by a clock input (CK) and a clear input ($\overline{\text{CLR}}$).

The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and $\overline{\text{Q}}$ 1 thru $\overline{\text{Q}}$ 4) on the positive-going edge of the clock pulse.

When the CLR input is held low, the Q outputs are at the low logic level and the $\overline{\text{Q}}$ outputs are at the high logic level, regardless of other input conditions.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

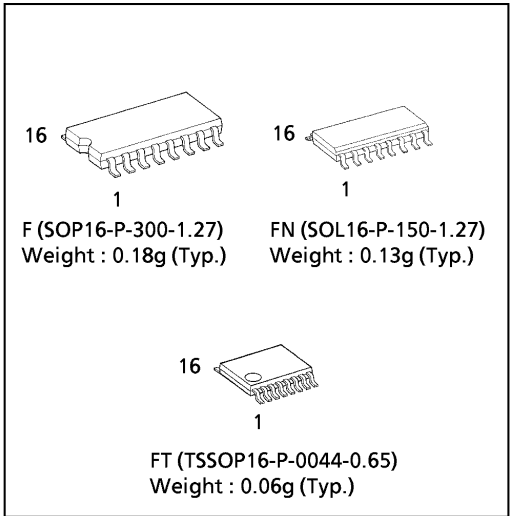
- High Speed..... $f_{\text{MAX}} = 210\text{MHz}(\text{typ.})$
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide Operating Voltage Range..... $V_{\text{CC}}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise $V_{\text{OLP}} = 0.8\text{V}$ (Max.)
- Pin and Function Compatible with 74 ALS175

TRUTH TABLE

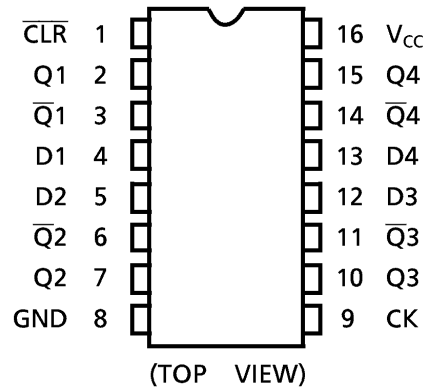
INPUTS			OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	X	X	L	H	CLEAR
H	L	\uparrow	L	H	—
H	H	\uparrow	H	L	—
H	X	\downarrow	Q_n	$\overline{\text{Q}}_n$	NO CHANGE

X : Don't Care

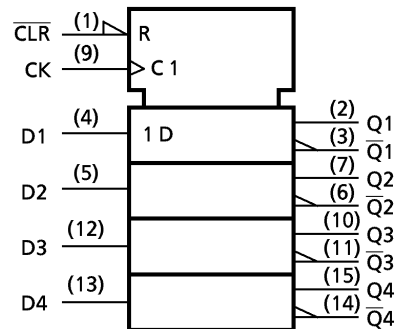
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



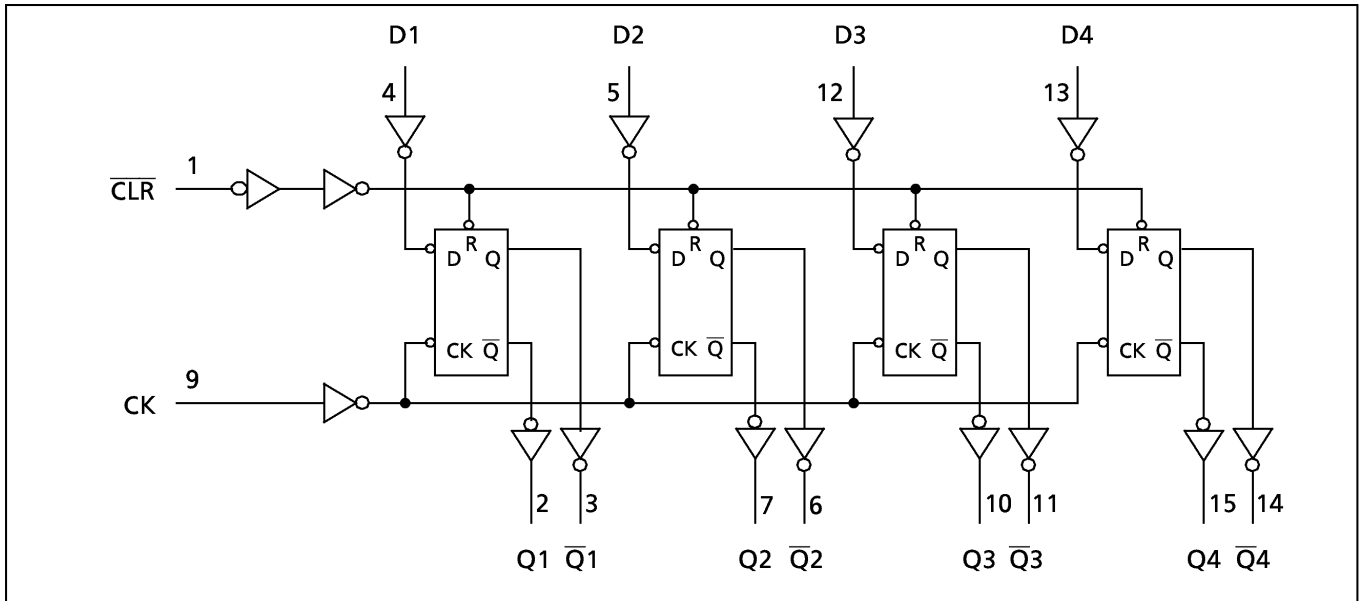
IEC LOGIC SYMBOL



961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

961001EBA2'

- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0~ 5.5	1.50 V _{CC} ×0.7	— —	— —	1.50 V _{CC} ×0.7	— —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} ×0.3	— —	0.50 V _{CC} ×0.3	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C		Ta = -40~85°C		UNIT
					TYP .	LIMIT	LIMIT		
Minimum Pulse Width (CK)	t _{W(L)} t _{W(H)}			3.3 ± 0.3	—	5.0	5.0	ns	
				5.0 ± 0.5	—	5.0	5.0		
Minimum Pulse Width (CLR)	t _{W(L)}			3.3 ± 0.3	—	5.0	5.0		
				5.0 ± 0.5	—	5.0	5.0		
Minimum Set - up Time	t _s			3.3 ± 0.3	—	5.0	5.0		
				5.0 ± 0.5	—	4.0	4.0		
Minimum Hold Time	t _h			3.3 ± 0.3	—	1.0	1.0		
				5.0 ± 0.5	—	1.0	1.0		
Minimum Removal Time (CLR)	t _{rem}			3.3 ± 0.3	—	5.0	5.0		
				5.0 ± 0.5	—	5.0	5.0		

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time (CK-Q, \bar{Q})	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	7.5	11.5	1.0	13.5	ns
				50	—	10.0	15.0	1.0	17.0	
			5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5	
				50	—	6.3	9.3	1.0	10.5	
Propagation Delay Time (CLR-Q, \bar{Q})	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	6.3	10.1	1.0	12.0	
				50	—	8.8	13.6	1.0	15.5	
			5.0 ± 0.5	15	—	4.3	6.4	1.0	7.5	
				50	—	5.8	8.4	1.0	9.5	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	15	90	140	—	75	—	MHZ
				50	50	75	—	45	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	85	115	—	75	—	
Output to Output Skew	$t_{oS LH}$ $t_{oS HL}$	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	44	—	—	—	

Note (1) Parameter guaranteed by design. $t_{oS LH} = |t_{pLH m} - t_{pLH n}|$, $t_{oS HL} = |t_{pHL m} - t_{pHL n}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per bit)}$$

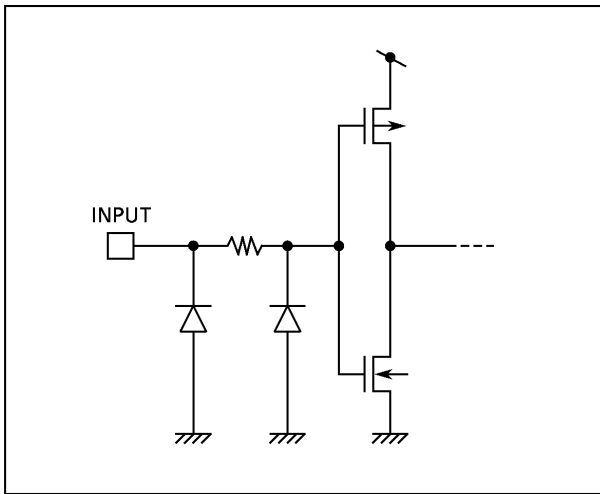
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation :

$$C_{PD} \text{ (total)} = 30 + 14 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

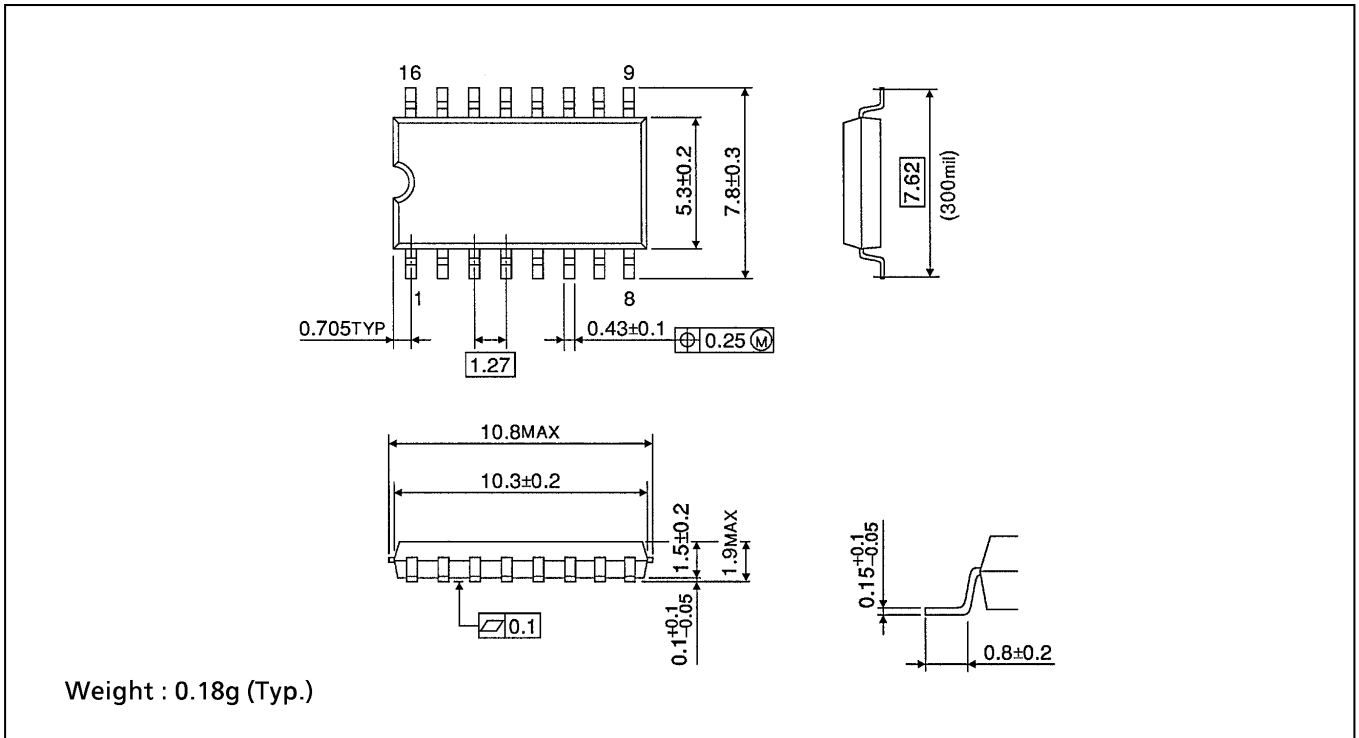
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

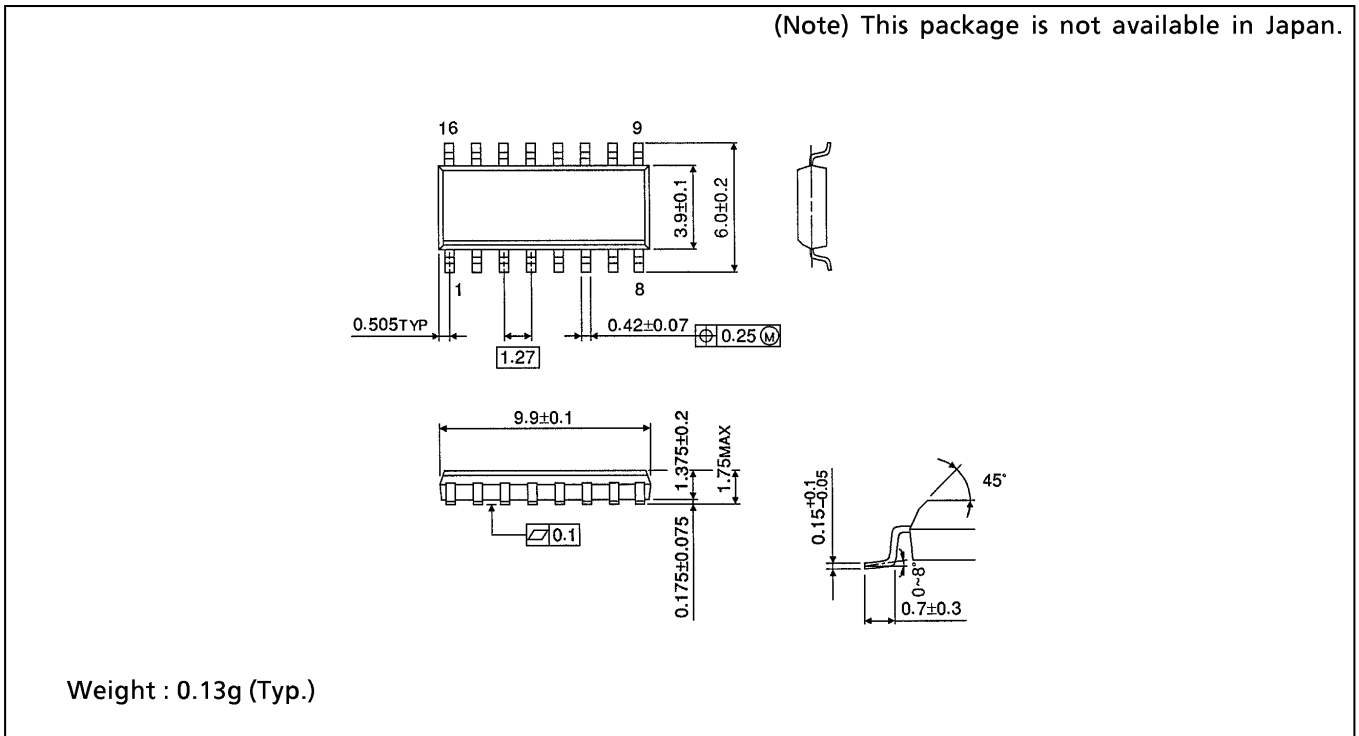
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOP16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm

