TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

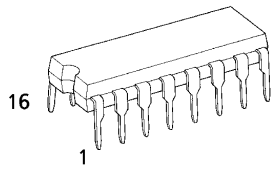
TC74HC40102AP, TC74HC40102AF
TC74HC40103AP, TC74HC40103AF

TC74HC40102AP/AF DUAL BCD PROGRAMMABLE DOWN COUNTER
TC74HC40103AP/AF 8 – BIT BINARY PROGRAMMABLE DOWN COUNTER

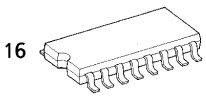
The TC74HC40102A and TC74HC40103A are high speed CMOS PROGRAMMABLE DOWN COUNTERS fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The output terminal ($\overline{CO}/\overline{ZD}$) goes to an active low state when the down count reaches zero. Since the TC74HC40102A is designed as a BCD counter, programming up to 99 counts is possible. The TC74HC40103A, with its 8-bit binary construction, can be set to provide up to 255 counts.
Both devices have Inhibit Clock ($\overline{CI}/\overline{CE}$), Asynchronous Preset Control ($\overline{APE}$), Synchronous Preset ($\overline{SPE}$) and Clear Control ($\overline{CLR}$) inputs for setting the counter to the maximum counting mode.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ····· f_{MAX} = 40MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 40102B, 40103B

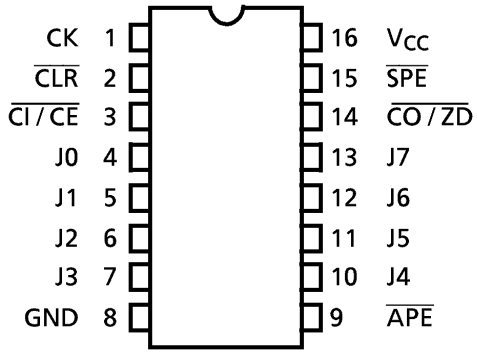


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

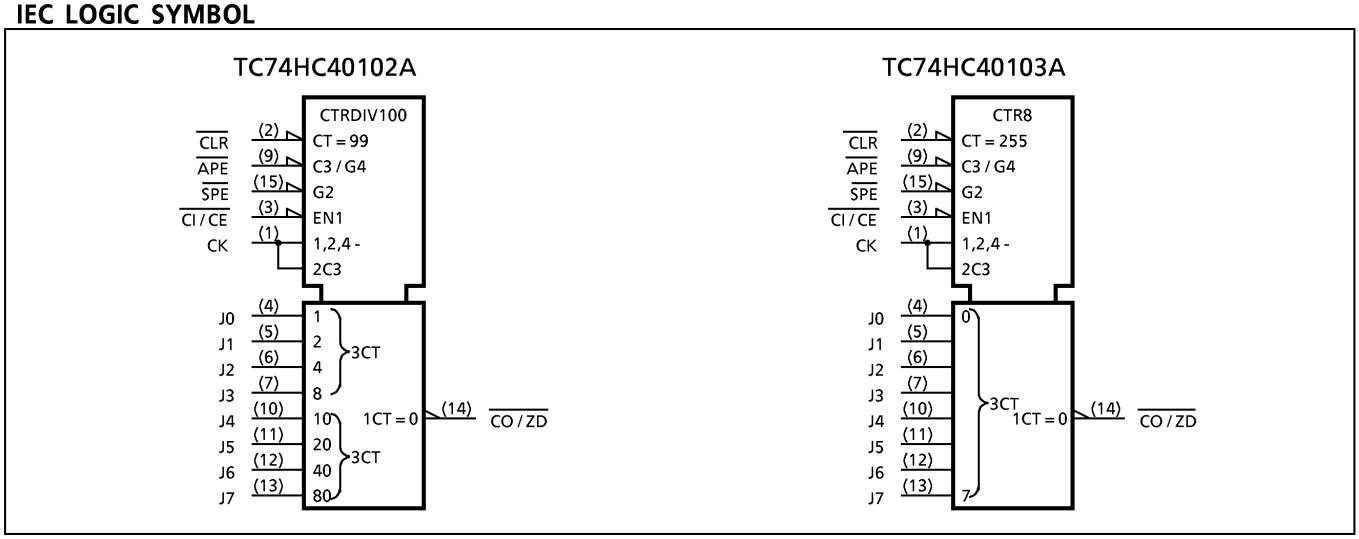
TRUTH TABLE

CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI}/\overline{CE}$		
H	H	H	H	Count inhibit	Count is inhibited regardless of other inputs.
H	H	H	L	Regular count	Down count on the rising edge of CK
H	H	L	X	Synchronous Preset	Input data is preset on the rising edge of CK
H	L	X	X	Asynchronous Preset	Input data is asynchronously preset to CK
L	X	X	X	Clear	Counter is set to maximum count.

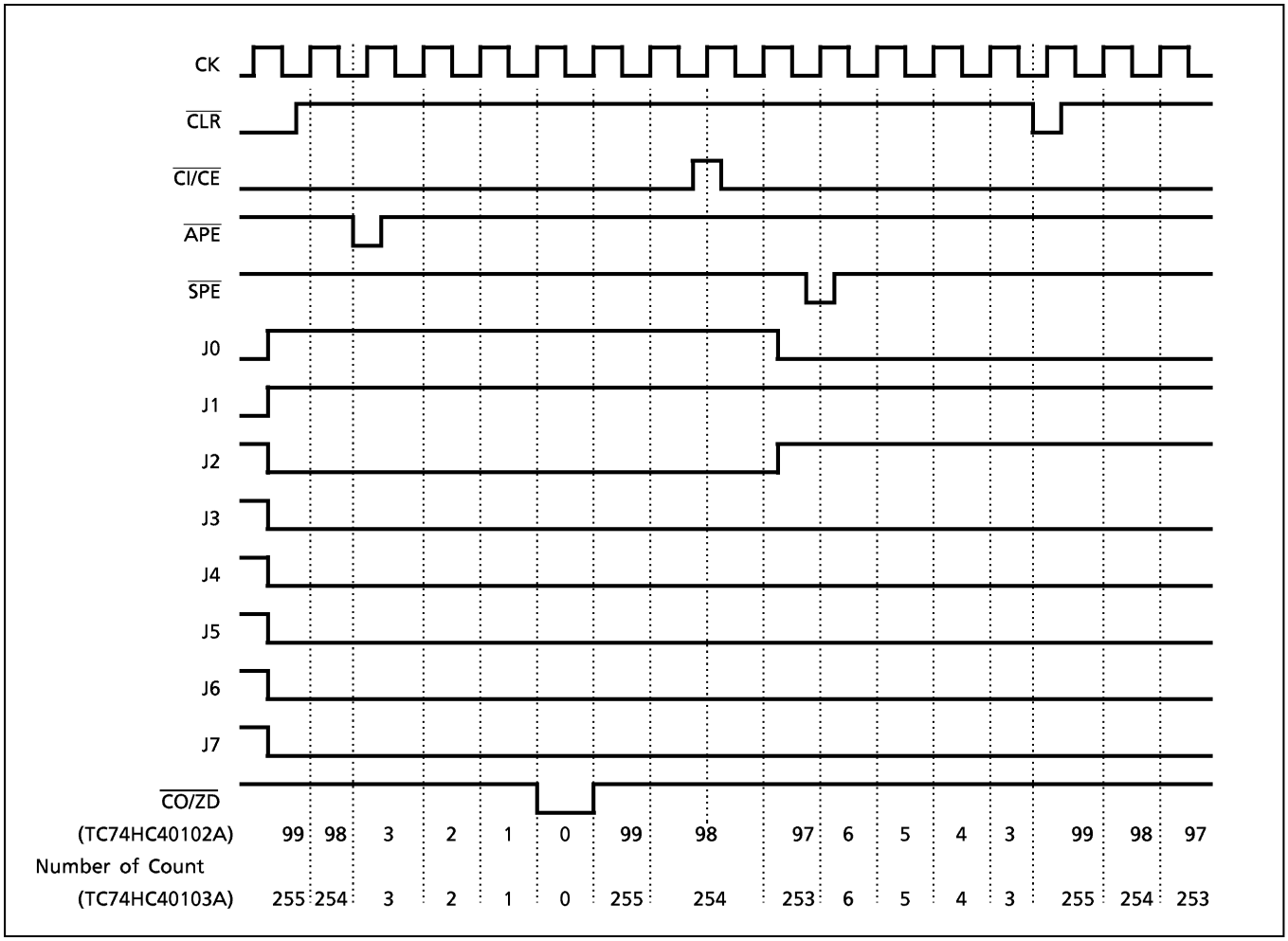
Note 1.X : Don't care
2. Maximum count : TC74HC40102A "99", TC74HC40103A "255"

980508EBA2

IEC LOGIC SYMBOL

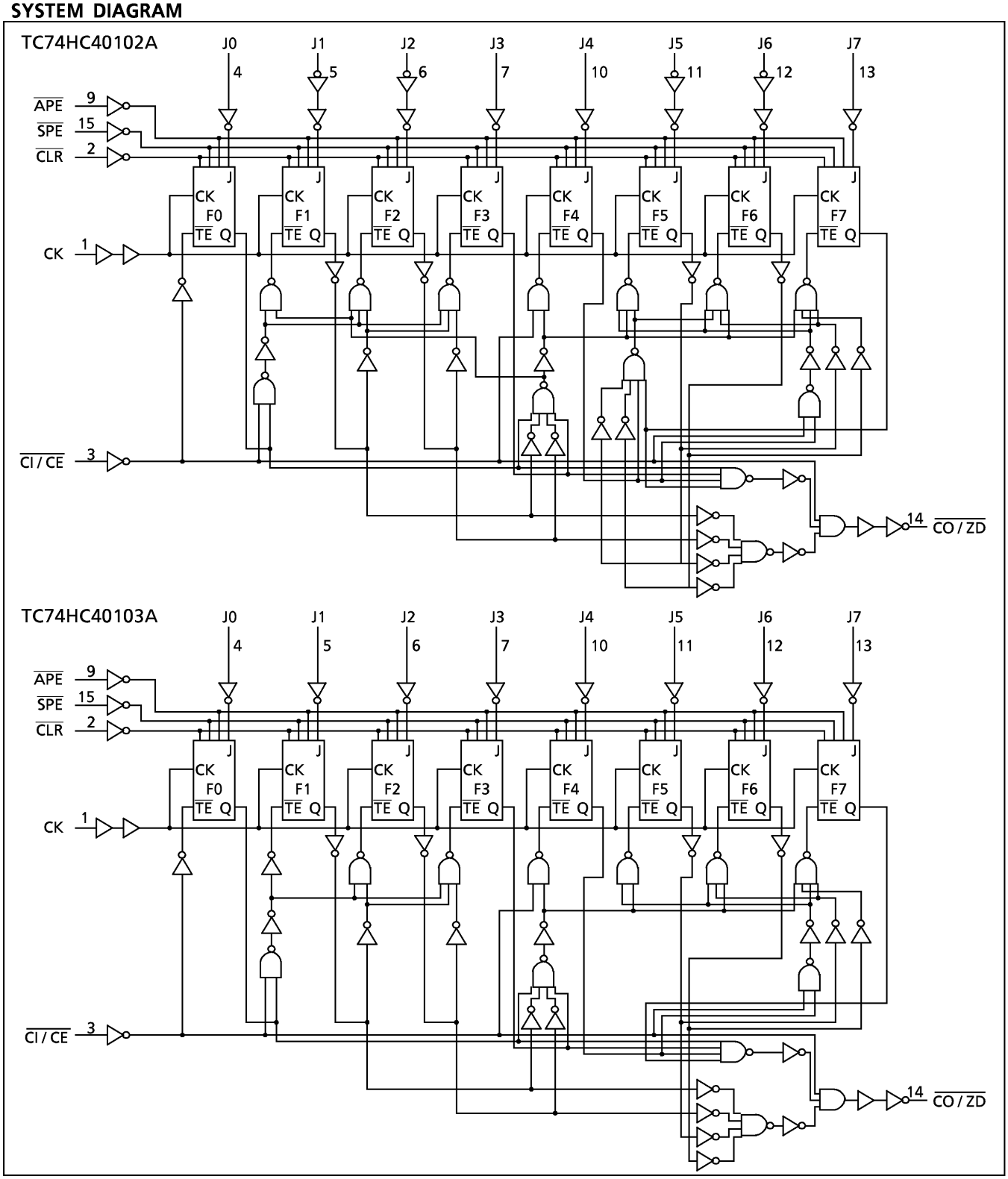


TIMING CHART

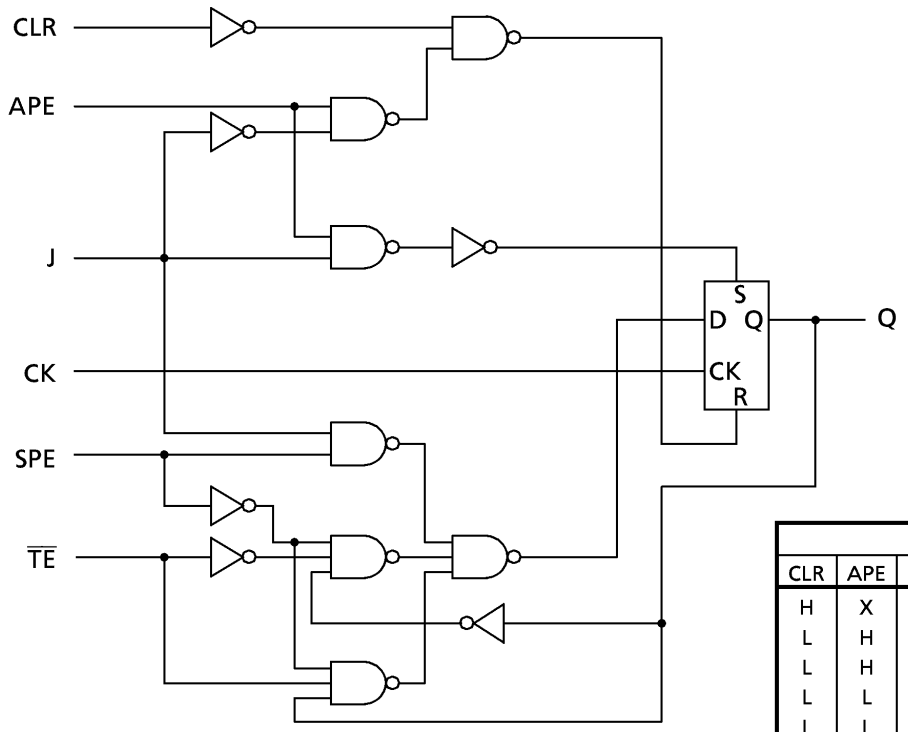


980508EBA2'

SYSTEM DIAGRAM



LOGIC DIAGRAM



INPUT						OUTPUT
CLR	APE	SPE	J	$\overline{TE}$	CK	Q
H	X	X	X	X	X	L
L	H	H	H	H	X	H
L	H	H	L	H	X	L
L	L	H	H	X	↑	H
L	L	H	L	X	↑	L
L	L	L	X	L	↑	$\overline{Qn}$
L	L	L	X	L	↓	Qn
L	L	L	X	H	X	Qn

FUNCTION DESCRIPTION

The TC74HC40102A and TC74HC40103A are 8-stage presettable synchronous down counters. Carry Out / Zero Detect ($\overline{CO / ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102A adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103A adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CK input. Count operation can be inhibited by setting Carry Input / clock Enable ($\overline{CI / CE}$) to the "H" level.

FUNCTION DESCRIPTION (Continued)

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102A and 255 for the TC74HC40103A) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102A and TC74HC40103A, respectively, when clock input alone is given without various kinds of preset operation.

PRESET OPERATION AND RESET OPERATION

When Clear ($\overline{CLR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLR}$ input. When Synvhrounous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with rise of clock.

As to these operation modes, refer to the truth table.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40~85°C MIN.	Ta=−40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH}=−4 mA I_{OH}=−5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=4 mA I_{OL}=5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		—	25	43	
Propagation Delay Time ($\overline{APE}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		—	25	49	
Propagation Delay Time ($\overline{CI}$ / $\overline{CE}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		—	10	19	
Propagation Delay Time ($\overline{CLR}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH}		—	24	36	
Maximum Clock Frequency	f_{MAX}		23	40	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	— — —	30 8 7	75 15 13	— — —	95 19 16	ns
Propagation Delay Time (CK − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	95 28 22	245 49 42	— — —	305 61 52	
Propagation Delay Time ($\overline{APE}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	100 30 25	300 60 51	— — —	375 75 64	
Propagation Delay Time ($\overline{CI}$ / $\overline{CE}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	38 13 11	115 23 20	— — —	145 29 25	
Propagation Delay Time ($\overline{CLR}$ − $\overline{CO}$ / $\overline{ZO}$)	t_{pLH}		2.0 4.5 6.0	— — —	85 28 23	240 48 41	— — —	300 60 51	
Maximum Clock Frequency	f_{MAX}		2.0 4.5 6.0	4 20 24	12 36 42	— — —	3 16 19	— — —	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	48	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

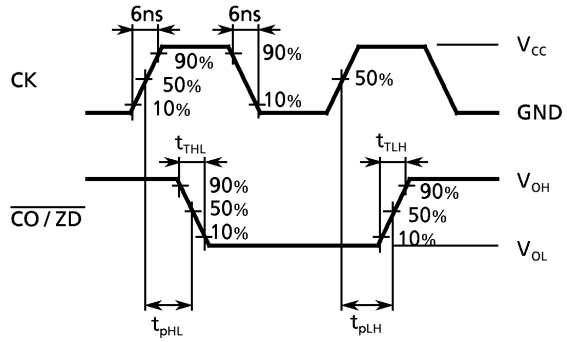
$$I_{CC}\,(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

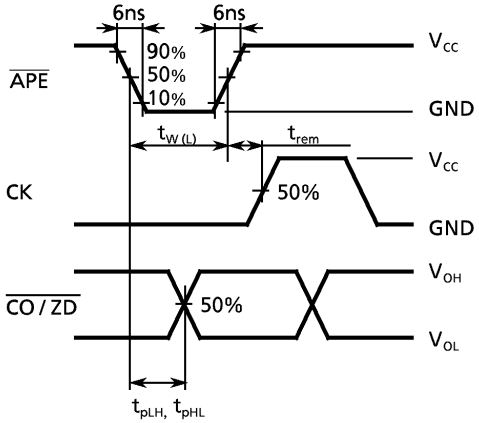
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{APE}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time ($\overline{SPE}$ − CK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time ($\overline{CI}$ / $\overline{CE}$ − CK)	t_s		2.0	—	150	190	
			4.5	—	30	38	
			6.0	—	26	32	
Minimum Set−up Time (Jn − CK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time (Jn − $\overline{APE}$)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time ($\overline{SPE}$ − CK)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time ($\overline{CI}$ / $\overline{CE}$ − CK)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (Jn − CK)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (Jn − $\overline{APE}$)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{APE}$)	t_{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Clock Frequency	f		2.0	—	4	3	MHz
			4.5	—	20	16	
			6.0	—	24	19	

SWITCHING CHARACTERISTICS TEST WAVEFORM

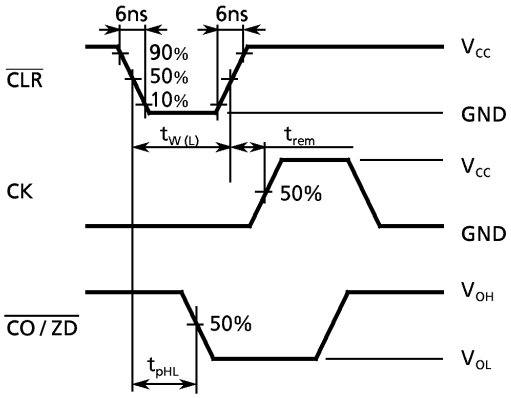
WAVEFORM 1



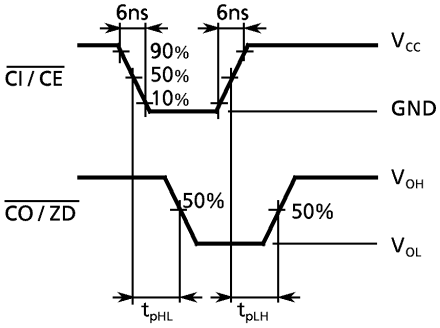
WAVEFORM 2



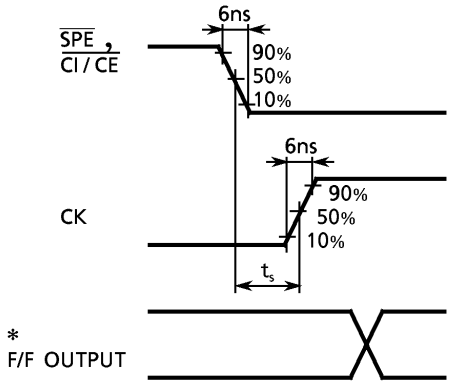
WAVEFORM 3



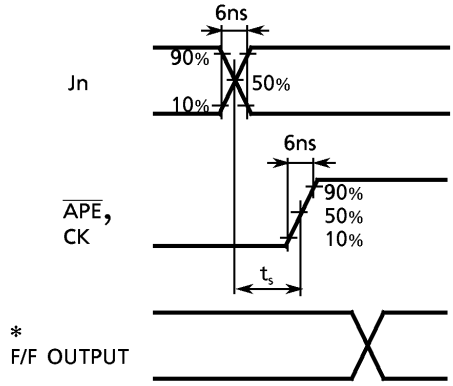
WAVEFORM 4



WAVEFORM 5



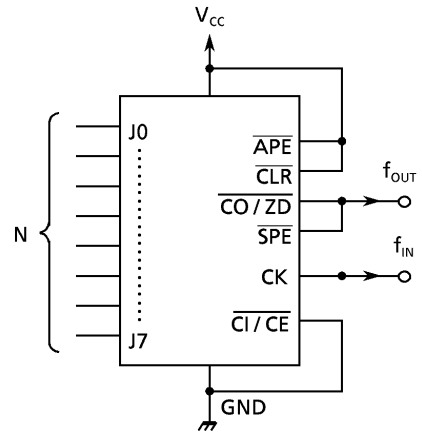
WAVEFORM 6



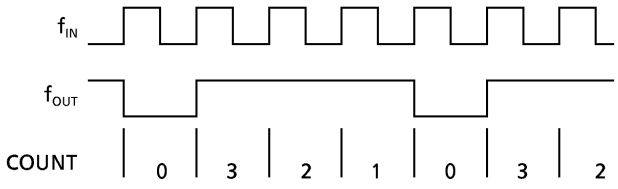
(** F/F output is internal signal of IC)

EXAMPLE OF TYPICAL APPLICATION

○ PROGRAMMABLE DIVIDE - BY - N COUNTER

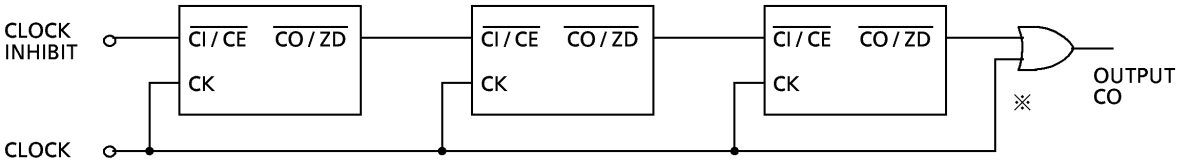


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N = "3" (J0, J1 = V_{CC}, J2~J7 = GND)



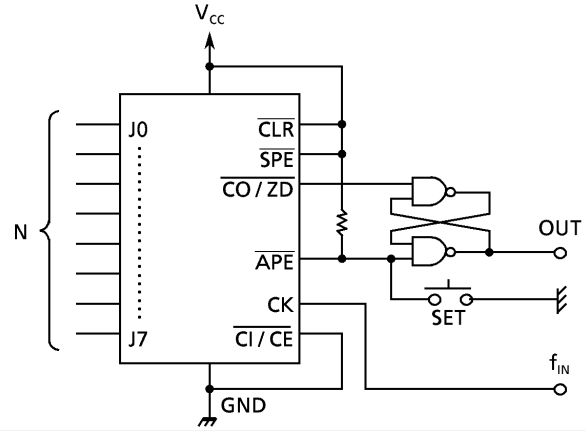
- TC74HC40102A ····· 1/2 to 1/100 are dividable.
- TC74HC40103A ····· 1/2 to 1/256 are dividable.

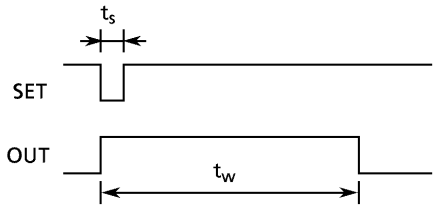
○ PARALLEL CARRY CASCADING



※ At synchronous cascade connection, huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate form TC74HC32A or the like, not form C0 output at the rear stage directly.

○ PROGRAMMABLE TIMER

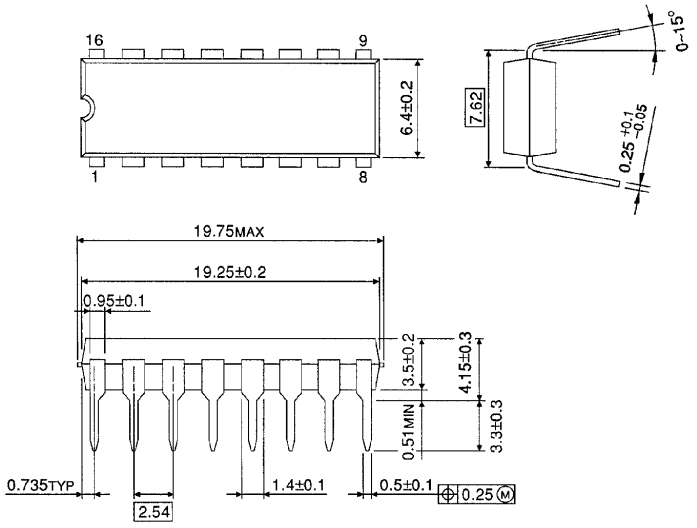




$t_w = \left(\frac{N}{f_{IN}} + t_s\right)$

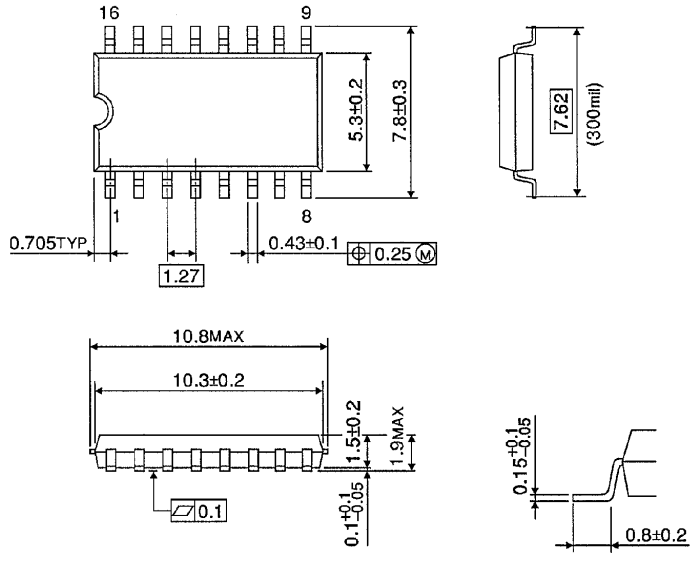
Note : The above formula dose not take into account the phase of ck input. Therefore, the real pulse width is the distance between the above formula - $1/f_{IN}$~the above formula.

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)