Ordering number : EN5377B

CMOS LSI

# LC72144M

## PLL Frequency Synthesizer

## Overview

The LC72144M is an electronic tuning PLL frequency synthesizer for use in car and home products, and allows high-performance multifunction tuners to be implemented easily, since it includes an A/D converter, a high-speed lockup circuit, and a crystal oscillator circuit that support AM up-conversion.

## Features

- High-speed programmable dividers for
  - — 10 to 160 MHz on FMIN using pulse swallower
  - — 0.5 to 40.0 MHz on AMIN using pulse swallower and direct division
- General-purpose counters
  - — HCTR for 0.4 to 25.0 MHz frequency measurement
  - — LCTR for 10 to 500 kHz frequency measurement and 4.0 Hz to $20 \times 10^3$ Hz period measurement
- 4.5, 7.2, 10.25 or 10.35 MHz crystal
- Twelve selectable reference frequencies (1, 3*2, 5, 9*2, 10, 3.125, 6.25, 12.5, 25, 30*2, 50 and 100*1 kHz)
  Note: 1. Not supported when a 10.35 or 10.25 MHz crystal oscillator is used.
  2. Not supported when a 10.25 MHz crystal oscillator is used.
- Phase comparator
  - — Insensitive band control
  - — Unlock detection
  - — Sub-charge pump for high-speed locking
  - — Deadlock clear circuit
- A/D converter: 6 bits, 2 inputs
- Serial data input and output
  Supports control and communication in the CCB format
- Power-on reset circuit
- On-chip crystal oscillator output buffer
- Inputs/outputs (using six general-purpose input/output ports)
- Operating ranges
  - — Power-supply voltage: 4.5 to 5.5 V
  - — Operating temperature: –40 to 85°C
- Package: MFP24S

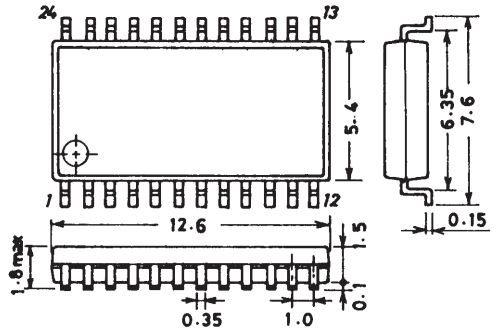
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

## Package Dimensions

unit: mm

**3112-MFP24S**

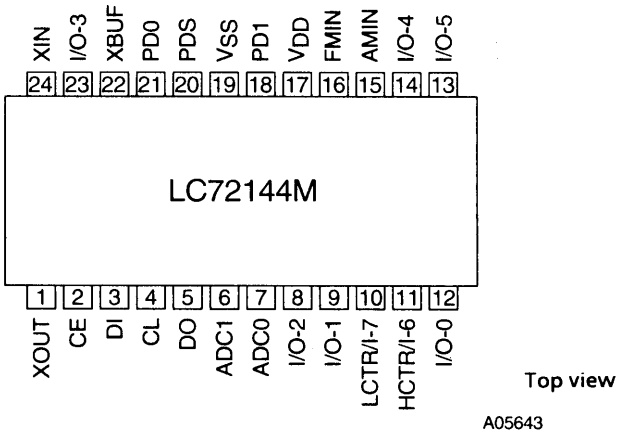
[LC72144M]



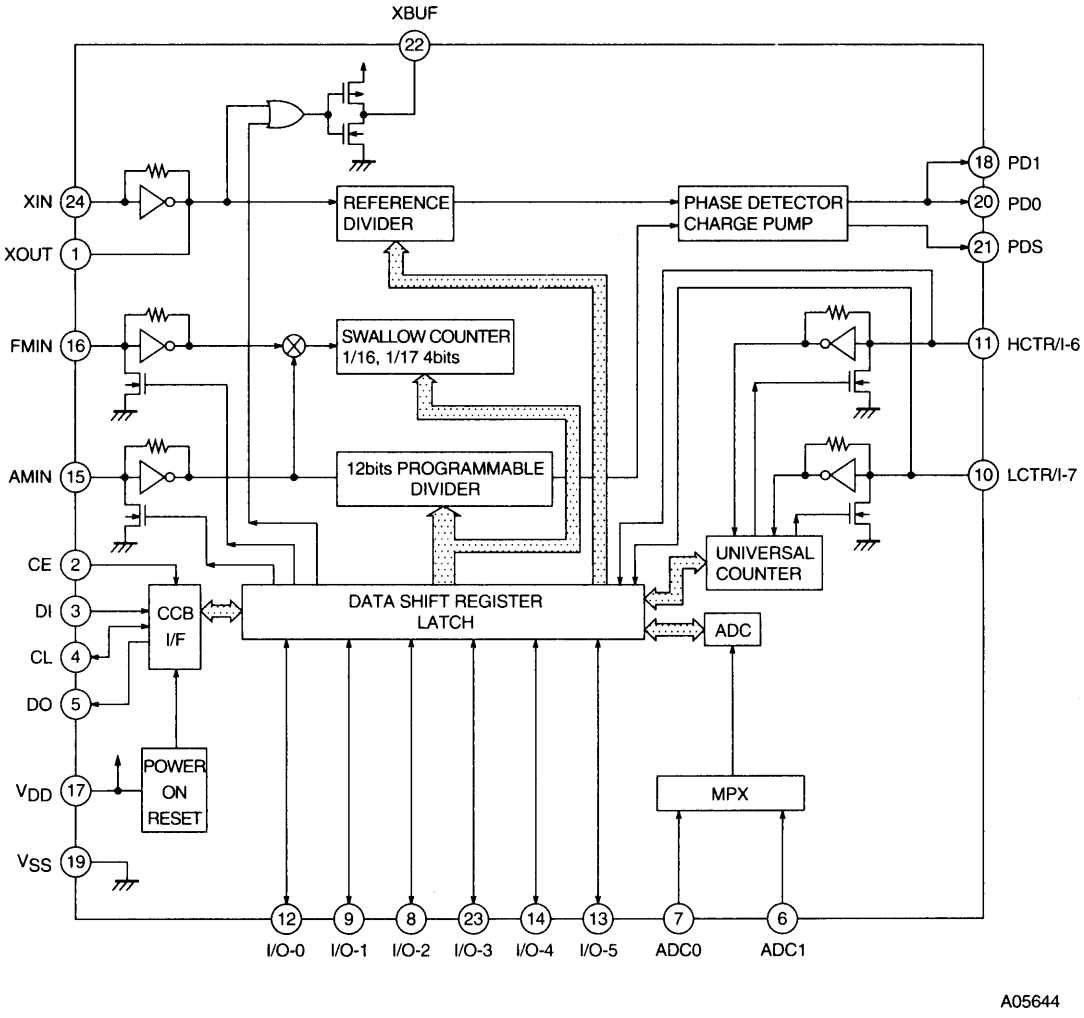

SANYO: MFP24S

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

## Pin Assignment




## Block Diagram



# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 to +7.0 | V |
| Maximum input voltage | $V_{IN}$1 max | CE, CL, DI | –0.3 to +7.0 | V |
| | $V_{IN}$2 max | XIN, FMIN, AMIN, HCTR/I-6, LCTR/I-7, I/O-0, I/O-4, I/O-5, ADC0, ADC1 | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{IN}$3 max | I/O-1 to I/O-3 | –0.3 to +15 | V |
| Maximum output voltage | $V_O$1 max | DO | –0.3 to +7.0 | V |
| | $V_O$2 max | XOUT, I/O-0, I/O-4, I/O-5, PD0, PD1, PDS, XBUF | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_O$3 max | I/O-1 to I/O-3 | –0.3 to +15 | V |
| Maximum output current | $I_O$1 max | I/O-0, I/O-4, I/O-5, XBUF | 0 to 3.0 | mA |
| | $I_O$2 max | DO | 0 to 6.0 | mA |
| | $I_O$3 max | I/O-1 to I/O-3 | 0 to 10 | mA |
| Allowable power dissipation | Pd max | Ta ≤85°C | 220 | mW |
| Operating temperature | Topr | | –40 to +85 | °C |
| Storage temperature | Tstg | | –55 to +125 | °C |

Note: A capacitor of at least 2000 pF must be inserted between the power supply, $V_{DD}$, and $V_{SS}$.

## Allowable Operating Ranges at Ta = –40 to 85°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$1 | $V_{DD}$ | 4.5 | | 5.5 | V |
| | $V_{DD}$2 | $V_{DD}$: Serial data hold voltage | 2.0 | | | |
| Input high-level voltage | $V_{IH}$1 | CE, CL, DI, I/O-1 to I/O-3 | 2.2 | | 6.5 | V |
| | $V_{IH}$2 | I/O-0, I/O-4, I/O-5, HCTR/I-6, LCTR/I-7 | 2.2 | | $V_{DD}$ | V |
| | $V_{IH}$3 | LCTR/I-7: Pulse waveform, *1 | 2.2 | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}$1 | CE, CL, DI, I/O-0 to I/O-5, HCTR/I-6, LCTR/I-7 | 0 | | 0.8 | V |
| | $V_{IL}$2 | LCTR/I-7: Pulse waveform, *1 | 0 | | 0.8 | V |
| Output voltage | $V_O$1 | DO | 0 | | 6.5 | V |
| | $V_O$2 | I/O-1 to I/O-3 | 0 | | 13 | V |
| Input frequency | $f_{IN}$1 | XIN: Sine wave, capacitor coupled | 1.0 | | 8.0 | MHz |
| | $f_{IN}$2 | FMIN: Sine wave, capacitor coupled | 10 | | 160 | MHz |
| | $f_{IN}$3 | AMIN: Sine wave, capacitor coupled | 0.5 | | 40 | MHz |
| | $f_{IN}$4 | HCTR/I-6: Sine wave, capacitor coupled | 0.4 | | 25 | MHz |
| | $f_{IN}$5 | LCTR/I-7: Sine wave, capacitor coupled | 10 | | 500 | kHz |
| | $f_{IN}$6 | LCTR/I-7: Pulse waveform, DC coupled, *1 | 4.0 | | $20 \times 10^3$ | Hz |
| Guaranteed crystal oscillator ranges | Xtal1 | XIN, XOUT: CI ≤ 120 Ω | 4.0 | | 7.0 | MHz |
| | Xtal2 | XIN, XOUT: CI ≤ 50 Ω | 7.1 | | 10.5 | MHz |
| Input amplitudes | $V_{IN}$1 | XIN | 200 | | 1500 | mVrms |
| | $V_{IN}$2-1 | FMIN: 10 ≤ f < 130 MHz, *2 | 40 | | 1500 | mVrms |
| | $V_{IN}$2-2 | FMIN: 130 ≤ f < 160 MHz, *2 | 70 | | 1500 | mVrms |
| | $V_{IN}$3-1 | AMIN: 2 ≤ f < 25 MHz, *2 | 40 | | 1500 | mVrms |
| | $V_{IN}$3-2 | AMIN: 25 ≤ f < 40 MHz, *2 | 70 | | 1500 | mVrms |
| | $V_{IN}$3-3 | AMIN: 0.5 ≤ f < 2.5 MHz, *2 | 40 | | 1500 | mVrms |
| | $V_{IN}$3-4 | AMIN: 2.5 ≤ f ≤ 10 MHz, *2 | 70 | | 1500 | mVrms |
| | $V_{IN}$4-1 | HCTR/I-6: 0.4 ≤ f ≤ 25 MHz, *3 | 40 | | 1500 | mVrms |
| | $V_{IN}$4-2 | HCTR/I-6: 8 ≤ f ≤ 12 MHz, *4 | 70 | | 1500 | mVrms |
| | $V_{IN}$5-1 | LCTR/I-7: 10 ≤ f < 400 kHz, *3 | 40 | | 1500 | mVrms |
| | $V_{IN}$5-2 | LCTR/I-7: 400 ≤ f < 500 kHz, *3 | 20 | | 1500 | mVrms |
| | $V_{IN}$5-3 | LCTR/I-7: 400 ≤ f < 500 kHz, *4 | 70 | | 1500 | mVrms |
| Input voltage range | $V_{IN}$6 | ADC0, ADC1 | 0 | | $V_{DD}$ | V |

Note: 1. Period measurement
2. Refer to the item on the structure of the programmable divider.
3. Serial data: CTC = 0
4. Serial data: CTC = 1

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Conditions | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Data setup time | $t_{SU}$ | DI, CL: *1 | | 0.45 | | | µs |
| Data hold time | $t_{HD}$ | DI, CL: *1 | | 0.45 | | | µs |
| Clock low-level time | $t_{CL}$ | CL: *1 | | 0.45 | | | µs |
| Clock high-level time | $t_{CH}$ | CL: *1 | | 0.45 | | | µs |
| CE wait time | $t_{EL}$ | CE, CL: *1 | | 0.45 | | | µs |
| CE setup time | $t_{ES}$ | CE, CL: *1 | | 0.45 | | | µs |
| CE hold time | $t_{EH}$ | CE, CL: *1 | | 0.45 | | | µs |
| Data latch change time | $t_{LC}$ | *1 | | | | 0.45 | µs |
| Data output time | $t_{DC}$ | DO, CL | Differs depending on the values of the pull-up resistor and the printed circuit board capacitances. *1 | | | 0.2 | µs |
| | $t_{DH}$ | DO, CE | | | | 0.2 | µs |

Note: Refer to the serial data timing.

## Electrical Characteristics for the Allowable Operating Ranges

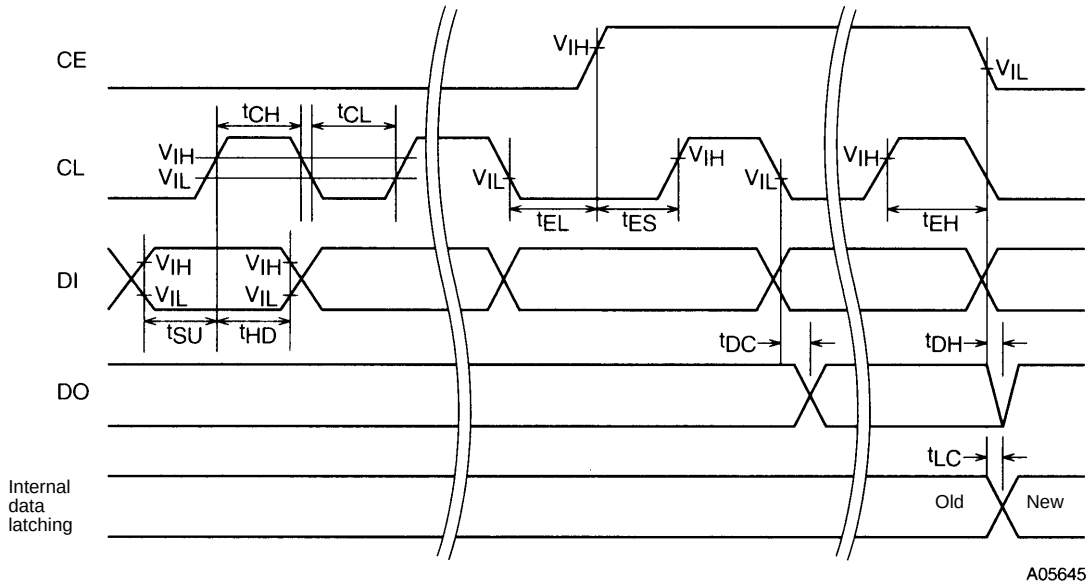
| Parameter | Symbol | Conditions | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Built-in feedback resistors | $R_f1$ | XIN | | | 1.0 | | MΩ |
| | $R_f2$ | FMIN | | | 500 | | kΩ |
| | $R_f3$ | AMIN | | | 500 | | kΩ |
| | $R_f4$ | HCTR/I-6 | | | 250 | | kΩ |
| | $R_f5$ | LCTR/I-7 | | | 250 | | kΩ |
| Hysteresis | $V_{HIS}$ | CE, CL, DI, LCTR/I-7 | | | 0.1 $V_{DD}$ | | V |
| High-level output voltage | $V_{OH}1$ | PD0, PD1, PDS, I/O-0, I/O-4, I/O-5 | $I_O$ = –0.5 mA | $V_{DD}$ – 0.5 | | | V |
| | | | $I_O$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| | | | $I_O$ = –2 mA | $V_{DD}$ – 2.0 | | | V |
| | $V_{OH}2$ | XBUF | $I_O$ = –0.5 mA | $V_{DD}$ – 1.5 | | | V |
| Low-level output voltage | $V_{OL}1$ | PD0, PD1, PDS, I/O-0, I/O-4, I/O-5 | $I_O$ = 0.5 mA | | | 0.5 | V |
| | | | $I_O$ = 1 mA | | | 1.0 | V |
| | | | $I_O$ = 2 mA | | | 2.0 | V |
| | $V_{OL}2$ | XBUF | $I_O$ = 0.5 mA | | | 1.5 | V |
| | $V_{OL}3$ | I/O-1 to I/O-3 | $I_O$ = 1 mA | | | 0.2 | V |
| | | | $I_O$ = 2.5 mA | | | 0.5 | V |
| | | | $I_O$ = 5 mA | | | 1.0 | V |
| | | | $I_O$ = 9 mA | | | 1.8 | V |
| | $V_{OL}4$ | DO: $I_O$ = 5 mA | | | | 1.0 | V |
| High-level input current | $I_{IH}1$ | CE, CL, DI: $V_I$ = 6.5 V | | | | 5.0 | µA |
| | $I_{IH}2$ | I/O-1 to I/O-3: $V_I$ = 13 V | | | | 5.0 | µA |
| | $I_{IH}3$ | I/O-0, I/O-4, I/O-5, ADC0, ADC1, HCTR/I-6, LCTR/I-7: $V_I = V_{DD}$ | | | | 5.0 | µA |
| | $I_{IH}4$ | XIN: $V_I = V_{DD}$ | | 2.0 | | 11 | µA |
| | $I_{IH}5$ | FMIN, AMIN: $V_I = V_{DD}$ | | 4.0 | | 22 | µA |
| | $I_{IH}6$ | HCTR/I-6, LCTR/I-7: $V_I = V_{DD}$ | | 8.0 | | 44 | µA |
| Low-level input current | $I_{IL}1$ | CE, CL, DI: $V_I$ = 0 V | | | | 5.0 | µA |
| | $I_{IL}2$ | I/O-0, to I/O-3: $V_I$ = 0 V | | | | 5.0 | µA |
| | $I_{IL}3$ | I/O-0, I/O-4, I/O-5, ADC0, ADC1, HCTR/I-6, LCTR/I-7: $V_I$ = 0 V | | | | 5.0 | µA |
| | $I_{IL}4$ | XIN: $V_I$ = 0 V | | 2.0 | | 11 | µA |
| | $I_{IL}5$ | FMIN, AMIN: $V_I$ = 0 V | | 4.0 | | 22 | µA |
| | $I_{IL}6$ | HCTR/I-6, LCTR/I-7: $V_I$ = 0 V | | 8.0 | | 44 | µA |
| Output off leakage current | $I_{OFF}1$ | I/O-1 to I/O-3: $V_O$ = 13 V | | | | 5.0 | µA |
| | $I_{OFF}2$ | DO: $V_O$ = 6.5 V | | | | 5.0 | µA |

Continued on next page.

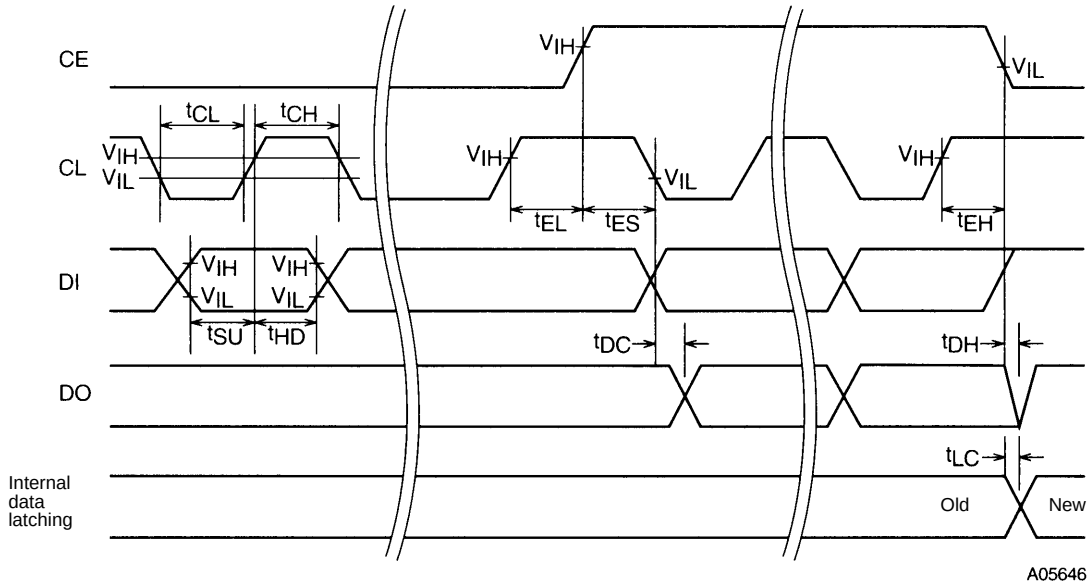
Continued from preceding page.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| High-level 3-state off leakage current | $I_{OFFH}$ | PD0, PD1, PDS: $V_O = V_{DD}$ | | 0.01 | 200 | nA |
| Low-level 3-state off leakage current | $I_{OFFL}$ | PD0, PD1, PDS: $V_O = 0$ V | | 0.01 | 200 | nA |
| Input capacitance | $C_{IN}$ | FMIN | | 6 | | pF |
| A/D converter linearity error | Err | ADC0, ADC1 | –0.5 | | +0.5 | LSB |
| Pull-down transistor on resistance | Rpd1 | FMIN | 80 | 200 | 600 | kΩ |
| | Rpd2 | AMIN | 80 | 200 | 600 | kΩ |
| Current drain | $I_{DD}1$ | $V_{DD}$: Xtal = 10.35 MHz, $f_{IN}2$ = 160 MHz, $V_{IN}2$ = 70 mVrms, $f_{IN}4$ = 25 MHz, $V_{IN}4$ = 40 mVrms | | 10 | 15 | mA |
| | $I_{DD}2$ | $V_{DD}$: PLL block stopped (PLL INHIBIT), Xtal oscillator operating (Xtal = 10.35 MHz) | | 0.5 | 1.5 | mA |
| | $I_{DD}3$ | $V_{DD}$: PLL block stopped, Xtal oscillator stopped | | | 10 | µA |

## Serial Data Timing

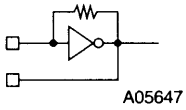
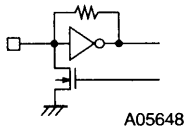
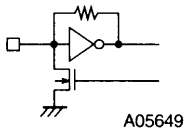
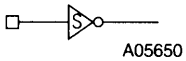
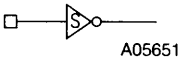
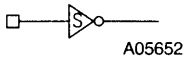
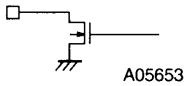
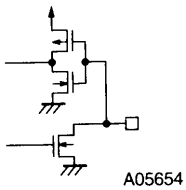
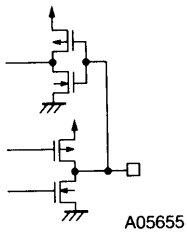



When CL is stopped at the low level



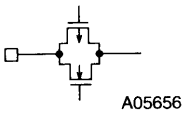
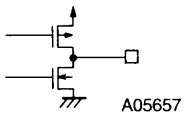
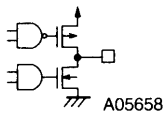
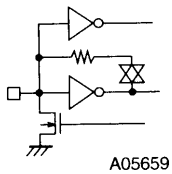
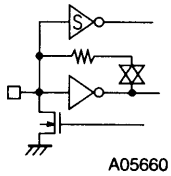
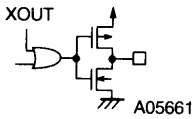

When CL is stopped at the high level

## Pin Functions

| Pin No. | Symbol | Type | Function | Pin circuit |
|---|---|---|---|---|
| 24<br>1 | XIN<br>XOUT | Xtal oscillator | Crystal oscillator connection<br>(4.5, 7.2, 10.25, or 10.35 MHz) |  <br>A05647 |
| 16 | FMIN | Local oscillator signal input | FMIN is selected when DVS in the serial data input is set to 1.<br>The input frequency range is 10 to 160 MHz.<br>The signal is transmitted to the swallow counter.<br>The divisor can be set to a value in the range 272 to 65,535. |  <br>A05648 |
| 15 | AMIN | Local oscillator signal input | AMIN is selected when DVS in the serial data input is set to 0.<br>When SNS in the serial data input is set to 1:<br>• The input frequency range is 2 to 40 MHz.<br>• The signal is transmitted to the swallow counter.<br>• The divisor can be set to a value in the range 272 to 65,535.<br>When SNS in the serial data input is set to 0:<br>• The input frequency range is 0.5 to 10 MHz.<br>• The signal is transmitted to the 12-bit programmable divider.<br>• The divisor can be set to a value in the range 4 to 4,095. |  <br>A05649 |
| 2 | CE | Chip enable | This pin must be set high during serial data input (DI) to the LC72144M, or during serial data output (DO). |  <br>A05650 |
| 4 | CL | Clock | Used for data synchronization during serial data input (DI) to the LC72144M, or during serial data output (DO). |  <br>A05651 |
| 3 | DI | Input data | Used to input serial data transferred to the LC72144M from the controller. |  <br>A05652 |
| 5 | DO | Output data | Used to output serial data transferred the controller from the LC72144M. |  <br>A05653 |
| 17 | $V_{DD}$ | Power supply | The LC72144M power supply connection. Provide a voltage between 4.5 and 5.5 V when the PLL circuit is in operation.<br>The power on reset circuit operates when power is first applied. | — |
| 19 | $V_{SS}$ | Ground | The LC72144M ground connection. | — |
| 9<br>8<br>23 | I/O-1<br>I/O-2<br>I/O-3 | General-purpose I/O ports | General-purpose I/O ports<br>The output circuits are open-drain circuits.<br>I/O-1 and I/O-2 are set to be input ports after the power on reset. I/O-3 becomes an output port fixed at the low level.<br>These pins are switched between input and output by the I/O-1 to I/O-3 bits in the serial data transferred from the controller. |  <br>A05654 |
| 12<br>14<br>13 | I/O-0<br>I/O-4<br>I/O-5 | General-purpose I/O ports | General-purpose I/O ports<br>The output circuits are complementary circuits.<br>These ports are set to be input ports after the power on reset.<br>These pins are switched between input and output by the I/O-0, I/O-4, and I/O-5 bits in the serial data transferred from the controller. |  <br>A05655 |

Continued on next page.

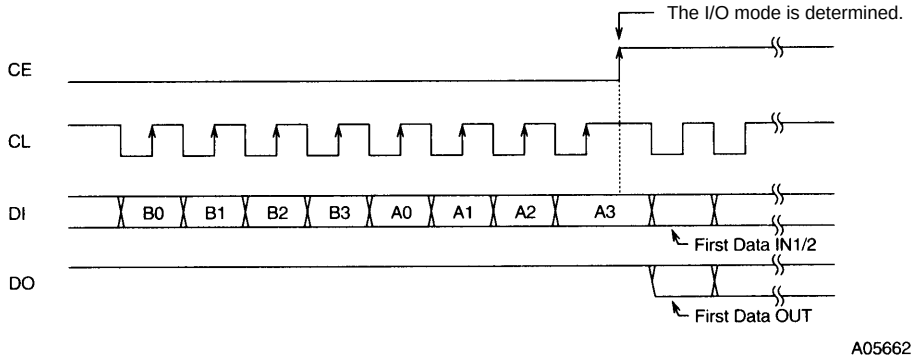
Continued from preceding page.

| Pin No. | Symbol | Type | Function | Pin circuit |
|---|---|---|---|---|
| 7<br>6 | ADC0<br>ADC1 | A/D converter input | A/D converter inputs<br>6-bit successive-approximation A/D converter<br>See the item on the structure of the A/D converter for details. |  <br>A05656 |
| 21<br>18 | PD0<br>PD1 | Main charge pump output | PLL charge pump output<br>A high level is output from the PD0 pin when the frequency created by dividing the local oscillator frequency by N is higher than the reference frequency. A low level is output when the frequency is lower. The pin goes to the high-impedance state when the frequencies agree.<br>The PD1 pin operates in the same manner. |  <br>A05657 |
| 20 | PDS | Sub-charge pump output | A high-speed lockup circuit can be formed by using this pin in combination with the main charge pump.<br>See the item on the structure of the charge pump for details. |  <br>A05658 |
| 11 | HCTR/I-6 | General-purpose counter | HCTR is selected when the CTS1 bit in the serial data is set to 1.<br>• The input frequency range is 0.4 to 25 MHz.<br>• The signal passes through a divide-by-2 circuit and then is input to a general-purpose counter. An integrating count can also be performed.<br>• The result of the count is output from the MSB of the general-purpose counter through the DO output pin.<br>• See the item on the structure of the general-purpose counter for details.<br>When the serial data H/I-6 bit is set to 0:<br>• This pin functions as an input port, and its state is output from the DO output pin. |  <br>A05659 |
| 10 | LCTR/I-7 | General-purpose counter | LCTR is selected when the CTS1 bit in the serial data is set to 0.<br>When the CTS0 bit in the serial data is set to 1:<br>• The circuit switches to frequency measurement mode.<br>• The input frequency range is 10 to 500 kHz.<br>• The signal is input directly to the general-purpose counter without passing through the divide-by-2 counter.<br>• The result of the count is output from the MSB of the general-purpose counter through the DO output pin.<br>When the CTS0 bit in the serial data is set to 0:<br>• The circuit switches to period measurement mode.<br>• The input frequency range is 4 Hz to 20 kHz.<br>• The measurement period can be set to be 1 or 2 periods.<br>• The result of the count is output from the MSB of the general-purpose counter through the DO output pin.<br>• See the item on the structure of the general-purpose counter for details.<br>When the L/I-7 bit in the serial data is set to 0.<br>• This pin functions as an input port, and its state is output from the DO output pin. |  <br>A05660 |
| 22 | XBUF | Xtal oscillator buffer | Output buffer for the crystal oscillator circuit.<br>If the XB bit in the serial data is set to 1, the output buffer operates and the crystal oscillator signal (a pulse waveform) is output.<br>If XB is 0, this pin outputs a low level. (Since XB is set to 0 after the power on reset, the output will be fixed at the low level.) |  <br>XOUT<br>A05661 |

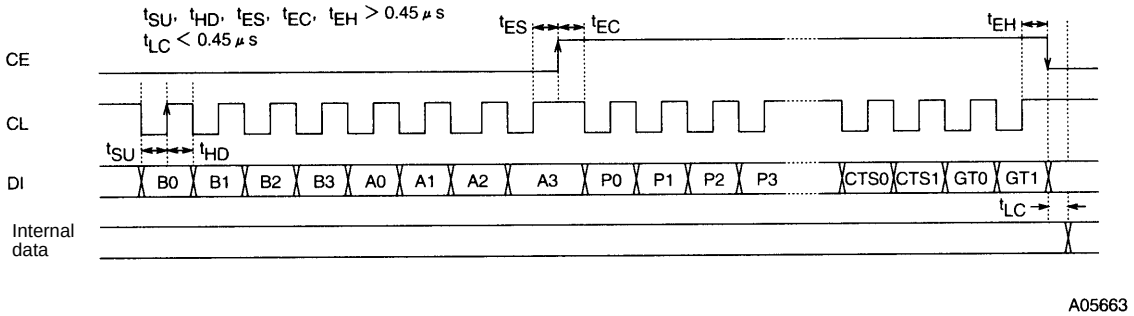
## Serial Data Input and Output Methods

Data is input and output using the CCB (computer control bus) format, which is Sanyo's audio LSI serial bus format.

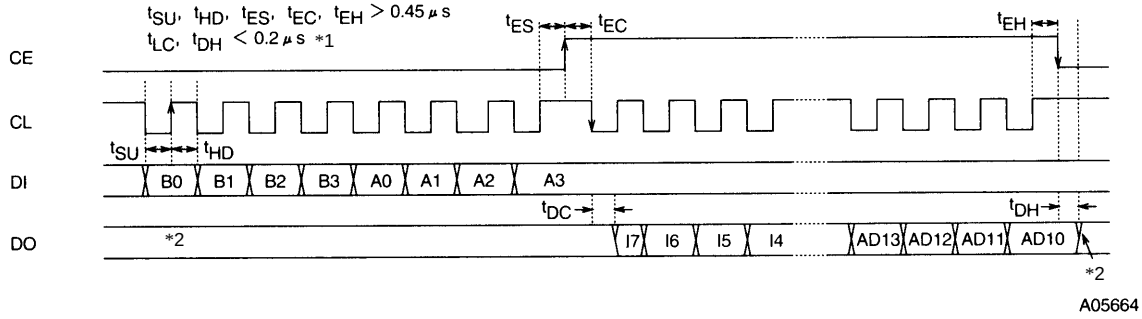
| | I/O mode | Address | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|
| | | B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | |
| (1) | IN1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | • Control data input mode (serial data input)<br>• 32 bits of data are input. |
| (2) | IN2 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | • Control data input mode (serial data input)<br>• 32 bits of data are input. |
| (3) | OUT | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | • Data output mode (serial data output)<br>• A number of bits equal to the number of clock cycles is output. |




1. Serial data input (IN1/IN2)



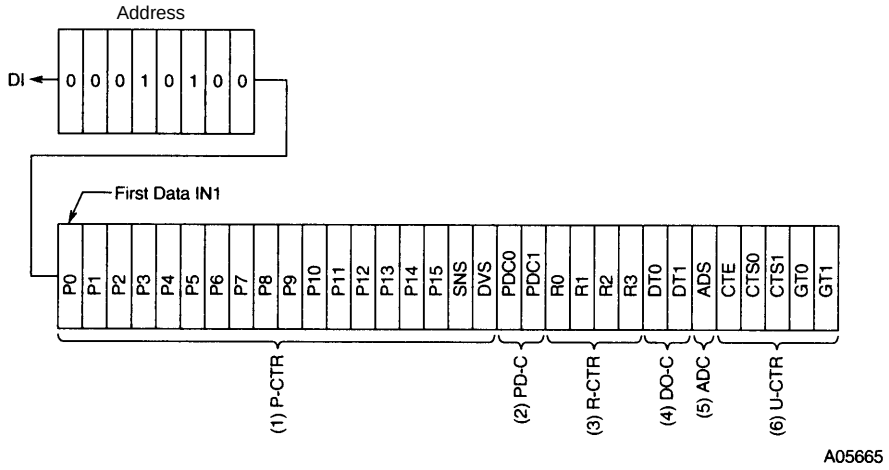

2. Serial data output (OUT)



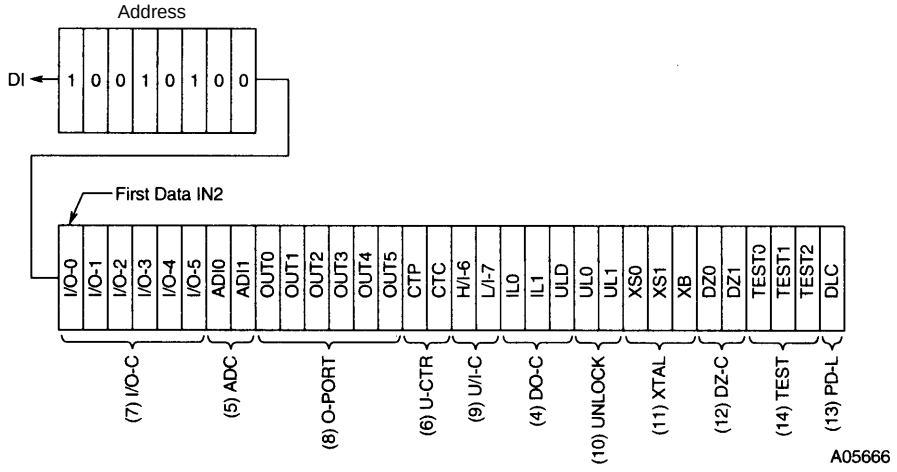

Note: 1. Since the DO pin is an n-channel open drain output, the data value transition time will differ depending on the value of the pull-up resistor and the printed circuit board capacitance values.
2. The DO pin is normally open.

## Structure of the DI Control Data

1. IN1




2. IN2

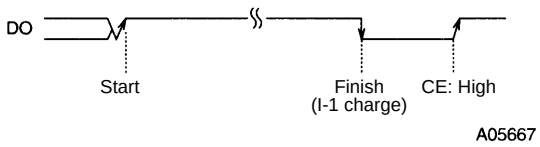


## Control Data Functions

<table>
<tr><th>No.</th><th>Control section/ data</th><th>Function</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data<br>P0 to P15, DVS, SNS</td><td>
Data that sets the programmable divider's divisor. It is a binary value and P15 is the MSB. The LSB differs depending on the DVS and SNS bits. (×: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th></tr>
<tr><td>1</td><td>×</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td></tr>
</table>
Note: When P4 is the LSB, P0 to P3 are ignored.<br>
These bits select the signal input pin (FMIN or AMIN) for the programmable divider and switch the input frequency range.
<table>
<tr><th>DVS</th><th>SNS</th><th>Input port</th><th>Input frequency range (MHz)</th></tr>
<tr><td>1</td><td>×</td><td>FMIN</td><td>10 to 160</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10</td></tr>
</table>
Note: See the "Programmable Divider Structure" item for details.
</td><td></td></tr>
<tr><td>(2)</td><td>Sub-charge pump<br>control data<br>PDC0, PDC1</td><td>
Data that controls the sub-change pump
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Sub-charge pump state</th></tr>
<tr><td>0</td><td>×</td><td>High impedance</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump operates (when unlocked)</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump operates (normal operation)</td></tr>
</table>
Note: The sub-charge pump can form a high-speed lockup circuit when combined with the PD0 and PD1 pins (the main charge pump).<br>
See the item on the structure of the charge pump for details.
</td><td>UL0, UL1, DLC</td></tr>
<tr><td>(3)</td><td>Reference divider data<br>R0 to R3</td><td>
Data that selects the reference frequency (fref)
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100*1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9*2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3*2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30*2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>*3, PLL inhibited and crystal oscillator stopped</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>*3, PLL inhibited</td></tr>
</table>
Note: 1. Cannot be used when the crystal oscillator frequency is 10.25 or 10.35 MHz.<br>
2. Cannot be used when the crystal oscillator frequency is 10.25 MHz.<br>
3. PLL inhibit (backup mode)<br>
The programmable divider block is stopped and FMIN and AMIN are both pulled down to ground. The charge pump output goes to the floating state.
</td><td></td></tr>
</table>

Continued on next page.

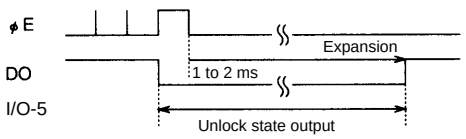
Continued from preceding page.

<table>
<tr><th>No.</th><th>Control section/ data</th><th>Function</th><th>Related data</th></tr>
<tr><td>(4)</td><td>Control data for the DO and I/O-5 pins<br>ULD, DT0, DT1, IL0, IL1</td><td>
Data that determines the DO and I/O-5 pin outputs
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO</th><th>I/O-5</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when unlocked</td><td rowspan="4">OUT5 flag*2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>end-AD</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN*1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td><td rowspan="4">Low when unlocked*2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>end-AD</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN*1</td></tr>
</table>
Note: end-AD: A/D converter conversion completion<br>
end-UC: General-purpose counter conversion completion<br>


<br>
Note: 1.
<table>
<tr><th>IL1</th><th>IL0</th><th>IN state</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>I-1 (pin state)</td></tr>
<tr><td>1</td><td>0</td><td>I-2 (pin state)</td></tr>
<tr><td>1</td><td>1</td><td>DO goes low when I-1 changes.</td></tr>
</table>
However, this pin becomes open if the I/O-1 and I/O-2 pins are specified to be output ports.<br>
2. Invalid if the I/O-5 pin is specified to be an input port.<br>
Note: Cannot be used when the crystal oscillator is stopped. (The DO pin will not change state.)<br>
(Reference divider: When R3 = R2 = R1 = 1, and R0 = 0)
</td><td>OUT5<br>I/O-1, I/O-2, I/O-5</td></tr>
<tr><td>(5)</td><td>A/D converter control data<br>ADS, ADI0, ADI1</td><td>
A/D converter conversion start data<br>
ADS = 1: Resets and starts the A/D converter<br>
= 0: Resets the A/D converter
<table>
<tr><th>ADI1</th><th>ADI0</th><th>AD input pin</th></tr>
<tr><td>1</td><td>1</td><td>Stopped</td></tr>
<tr><td>1</td><td>0</td><td>ADC0</td></tr>
<tr><td>0</td><td>1</td><td>ADC1</td></tr>
<tr><td>0</td><td>0</td><td>ADC0, ADC1</td></tr>
</table>
If ADC0 and ADC1 are specified for AD input at the same time, conversions are performed in the order ADC0 first, then ADC1.<br>
See the item on the structure of the A/D converter for details.
</td><td></td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control section/ data</th><th>Function</th><th>Related data</th></tr>
<tr><td>(6)</td><td>General-purpose counter control data<br>CTS0, CTS1, CTE, GT0, GT1<br>CTP, CTC</td><td>
Data that selects the input pin (HCTR or LCTR) for the general-purpose counter
<table>
<tr><th>CTS1</th><th>CTS0</th><th>Input pin</th><th>Measurement mode</th></tr>
<tr><td>1</td><td>X</td><td>HCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>1</td><td>LCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>0</td><td>LCTR</td><td>Period</td></tr>
</table>
Data that specifies the start of a general-purpose counter measurement operation<br>
CTE = 1: Count start<br>
= 0: Count reset<br>
Data that determines the general-purpose counter measurement time (in frequency mode) and number of periods (in period mode)
<table>
<tr><th rowspan="2">GT1</th><th rowspan="2">GT0</th><th colspan="3">Frequency measurement mode</th><th rowspan="2">Period measurement mode</th></tr>
<tr><th>Measurement time (ms)</th><th colspan="2">Wait time (ms)</th></tr>
<tr><th></th><th></th><th></th><th>CTP = 0</th><th>CTP = 1</th><th></th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td><td>1 to 2</td><td>1 period</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td><td>1 to 2</td><td>1 period</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td><td>1 to 2</td><td>2 periods</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td><td>1 to 2</td><td>2 periods</td></tr>
</table>
CTP = 0: The general-purpose counter input is pulled down at count reset time (when CTE = 0).<br>
= 1: The wait time is shortened by not pulling down the general-purpose counter input count reset time (when CTE = 0). However, immediately after CTP is set to 1, the system must wait until the general-purpose counter input pin is biased before starting a count.<br>
The input sensitivity is lowered by setting CTC to 1. (Sensitivity: 10 to 30 mVrms)
</td><td>H/I-6, L/I-7</td></tr>
<tr><td>(7)</td><td>I/O port control data<br>I/O-0 to I/O-5</td><td>
Data that specifies the input or output state of the I/O ports<br>
Data value = 0: Input port<br>
= 1: Output port<br>
Note: I/O-0, I/O-1, I/O-2, I/O-4, and I/O-5 are set to function as input ports after the power on reset.<br>
I/O-3 is set to function as an output port after the power on reset.
</td><td>OUT0 to OUT5, ULD</td></tr>
<tr><td>(8)</td><td>Output port data<br>OUT0 to OUT5</td><td>
Data that determines the output values of output ports O-0 to O-5<br>
Data value = 1: Open or high<br>
= 0: Low<br>
Note: This data is invalid when the corresponding port is specified to function as an input port or as an unlock state output.
</td><td>I/O-0 to I/O-5, ULD</td></tr>
<tr><td>(9)</td><td>General-purpose counter input control data<br>H/I-6, L/I-7</td><td>
Data that sets the general-purpose counter pins to function as input ports<br>
H/I-6 = 0: I-6 (input port)<br>
= 1: HCTR (general-purpose counter)<br>
L/I-7 = 0: I-7 (input port)<br>
= 1: LCTR (general-purpose counter)
</td><td>CTS0, CTS1</td></tr>
<tr><td>(10)</td><td>Unlock detection data<br>UL0, UL1</td><td>
Data that selects the phase error (øE) detection width used for PLL lock state discrimination<br>
If a phase error in excess of the øE detection width listed in the table below is detected, the system considers a phase error to have occurred and the PLL to be in the unlocked state. The detection pin (DO or I/O-5) is set low in the unlocked state.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection pin output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE output</td></tr>
<tr><td>1</td><td>0</td><td>±0.5 µs</td><td>øE with 1 to 2 ms expansion</td></tr>
<tr><td>1</td><td>1</td><td>±1.0 µs</td><td>øE with 1 to 2 ms expansion</td></tr>
</table>


A05668
</td><td>ULD, DT0, DT1</td></tr>
</table>

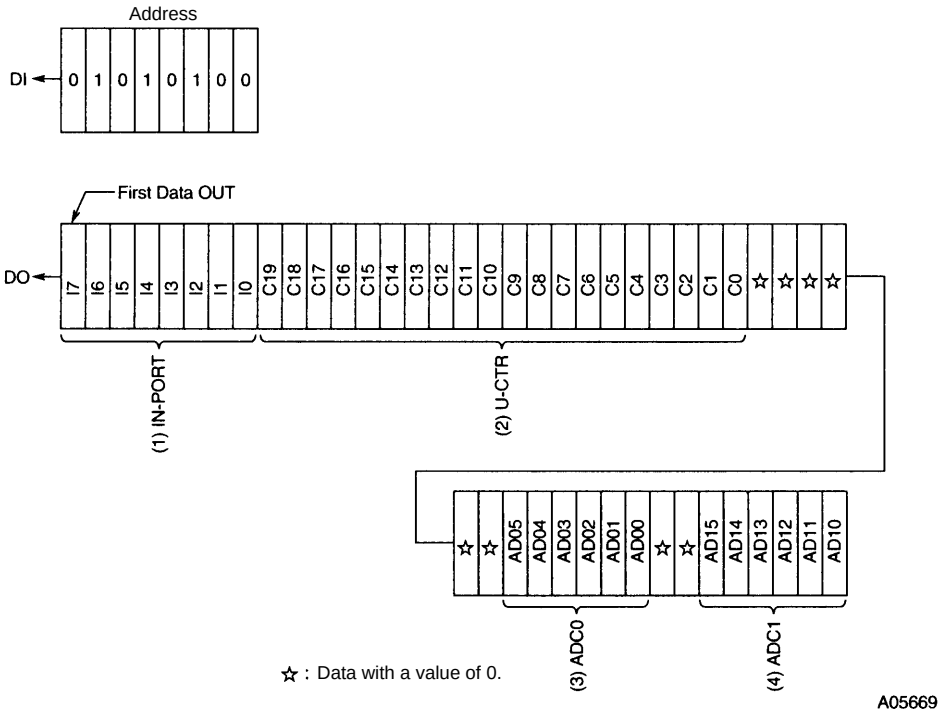
Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control section/ data</th><th>Function</th><th>Related data</th></tr>
<tr><td>(11)</td><td>Crystal oscillator circuit<br>XS0, XS1, XB</td><td>Data that selects the crystal oscillator element
<table>
<tr><th>XS1</th><th>XS0</th><th>Xtal OSC</th></tr>
<tr><td>0</td><td>0</td><td>4.5 MHz</td></tr>
<tr><td>0</td><td>1</td><td>7.2 MHz</td></tr>
<tr><td>1</td><td>0</td><td>10.25 MHz</td></tr>
<tr><td>1</td><td>1</td><td>10.35 MHz</td></tr>
</table>
Note: The 10.25 MHz setting is selected after the power on reset.<br>
Data that controls the crystal oscillator element buffer output<br>
XB = 0: Buffer output off (This mode is selected after the power on reset.)<br>
= 1: Buffer output on<br>
Note: Turn off the XBUF output in FM reception mode (PD0 pin used).</td><td>R0 to R3</td></tr>
<tr><td>(12)</td><td>Phase comparator control data<br>DZ0, DZ1</td><td>Data that controls the phase comparator dead band
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Insensitive band (dead zone) mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Note: DZA is selected after power-on reset.</td><td></td></tr>
<tr><td>(13)</td><td>Charge pump control data<br>DLC</td><td>Data that forces the charge pump output to the low level (VSS level).<br>
DLC = 1: Low level<br>
= 0: Normal operation<br>
Note: If a deadlock occurs due to the VCO oscillator being stopped by the VCO control voltage ($V_{tune}$) becoming 0, the deadlock can be resolved by setting the charge pump output to the low level and then setting $V_{tune}$ to $V_{CC}$.<br>
This data is set to the normal operating mode state after the power on reset.</td><td></td></tr>
<tr><td>(14)</td><td>LSI test data<br>TEST0, TEST1, TEST2</td><td>Data that controls LSI testing<br>
This data must all be set to 0, i.e.:<br>
TEST0 = 0<br>
TEST1 = 0<br>
TEST2 = 0<br>
Note: All the test data is set to 0 after the power on reset.</td><td></td></tr>
</table>

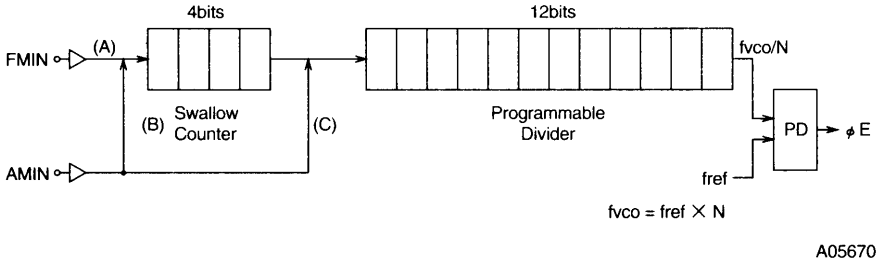
## Structure of the DO Output Data (Serial Data Output)

3. OUT




| No. | Control section/ data | Function | Related data |
|---|---|---|---|
| (1) | I/O port data<br>I0 to I7 | I/O port data: The I0 to I7 pins reflect the latched I/O-0 to I/O-7 I/O port pin states. Data is latched when data output mode is entered.<br>The pin states are latched regardless of the input or output mode specification.<br>Pin state = high: 1, low: 0 | I/O-0 to I/O-5,<br>H/I-6, L/I-7 |
| (2) | General-purpose counter binary data<br>C0 to C19 | Counter contents<br>Bits C0 to C19 are the latched contents of the 20-bit binary counter. C0 is the LSB.<br>C19: MSB<br>C0: LSB | CTS0, CTS1, CTE |
| (3) | A/D converter ADC0 data<br>AD00 to AD05 | The result of A/D conversion of the signal input to the ADC0 pin is latched and output from the AD00 to AD05 pins<br>AD05: MSB<br>AD00: LSB | ADI0, ADI1, ADS |
| (4) | A/D converter data<br>ADC1 data<br>AD10 to AD15 | The result of A/D conversion of the signal input to the ADC1 pin is latched and output from the AD10 to AD15 pins<br>AD15: MSB<br>AD10: LSB | ADI0, ADI1, ADS |

## Programmable Divider



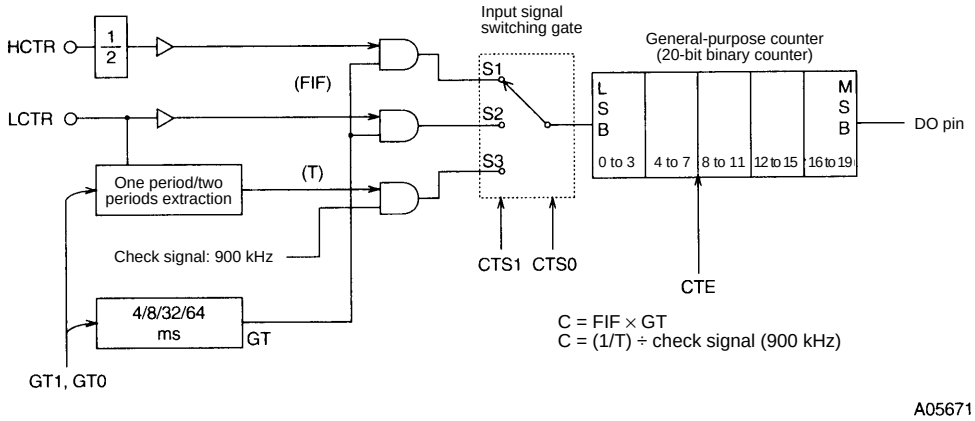

| | DVS | SNS | Divisor setting (N) | Input frequency range | Input port |
|---|---|---|---|---|---|
| (A) | 1 | × | 272 to 65535 | 10 to 160 MHz | FMIN |
| (B) | 0 | 1 | 272 to 65535 | 2 to 40 MHz | AMIN |
| (C) | 0 | 0 | 4 to 4095 | 0.5 to 10 MHz | AMIN |

Note: × = don't care

| | Minimum input sensitivity (f [MHz]) | |
|---|---|---|
| (A) FMIN | 10 ≤ f< 130 | 130 ≤ f < 160 |
| | 40 mVrms | 70 mVrms |
| (B) AMIN | 2 ≤ f < 25 | 25 ≤ f < 40 |
| | 40 mVrms | 70 mVrms |
| (C) AMIN | 0.5 ≤ f < 2.5 | 2.5 ≤ f < 10 |
| | 40 mVrms | 70 mVrms |

## General-Purpose Counter

The LC72144M includes a general-purpose 20-bit binary counter whose value can be read out from the DO pin, MSB first.




When using this counter for frequency measurement, one of four measurement times (4, 8, 32, or 64 ms) is selected by GT0 and GT1. The frequency input to either the HCTR or the LCTR pin can be measured by determining the number of pulses input to the counter during the measurement period.
This counter can be used to measure the period of the signal input to the LCTR pin by determining how many cycles of a reference signal (900 kHz) are input to the counter during one or two periods of the LCTR pin signal.

## Check Signal Frequency

| Xtal OSC | 4.5 MHz | 7.2 MHz | 10.25 MHz | 10.35 MHz | |
|---|---|---|---|---|---|
| | | | | fref = 30, 9, 3 kHz | fref: A frequency other than 3, 9, or 30 kHz |
| Check signal | 900 kHz | 900 kHz | 1025 kHz | 1030 kHz | 1150 kHz |

| | CTS1 | CTS0 | Input pin | Measurement mode | Frequency range | Input sensitivity |
|---|---|---|---|---|---|---|
| S1 | 1 | × | HCTR | Frequency | 0.4 to 25.0 MHz | 40 mVrms* |
| S2 | 0 | 1 | LCTR | Frequency | 10 to 500 kHz | 40 mVrms* |
| S3 | 0 | 0 | LCTR | Period | 4.0 to 20 × $10^3$ Hz | (pulse) |

Note: * CTC = 0: 40 mVrms
CTC = 1: 70 mVrms
However, the frequency ranges will be as follows when CTC is 1.
HCTR: 8 to 12 MHz, LCTR: 400 to 500 kHz

The CTC data is input sensitivity switching data, and the input sensitivity is degraded when CTC is set to 1.

| | HCTR: Minimum input sensitivity rating [f (MHz)] | | | LCTR: Minimum input sensitivity rating [f (kHz)] | |
|---|---|---|---|---|---|
| CTC | 0.4 ≤ f < 8 | 8 ≤ f < 12 | 12 ≤ f < 25 | 10 ≤ f < 400 | 400 ≤ f < 500 |
| 0 (normal mode) | 40 mVrms | 40 mVrms (1 to 10 mVrms) | 40 mVrms | 40 mVrms | 20 mVrms (0.1 to 3 mVrms) |
| 1 (degraded mode) | — | 70 mVrms (30 to 40 mVrms) | — | — | 70 mVrms (10 to 15 mVrms) |

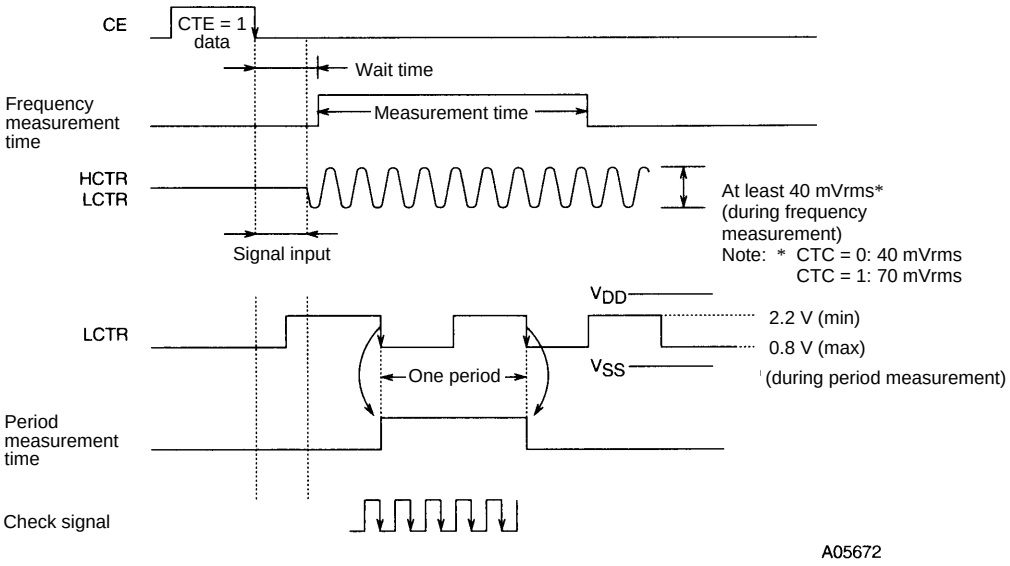
—: Not stipulated (not included in device guarantee)
( ): Actual performance estimates (reference values)

The CTP data determines the state of the general-purpose counter input pin (HCTR/LCTR) when the general-purpose counter is reset (CTE = 0).
CTP = 0: The general-purpose counter input pin is pulled down.
= 1: The wait time is shortened to 1 to 2 ms by not pulling down the general-purpose counter input pin.
If CTP is set to 1, is must be set to 1 at least 4 ms before a count start (CTE = 1) is issued.
CTP must be set to and left at 0 if the counter is not used.

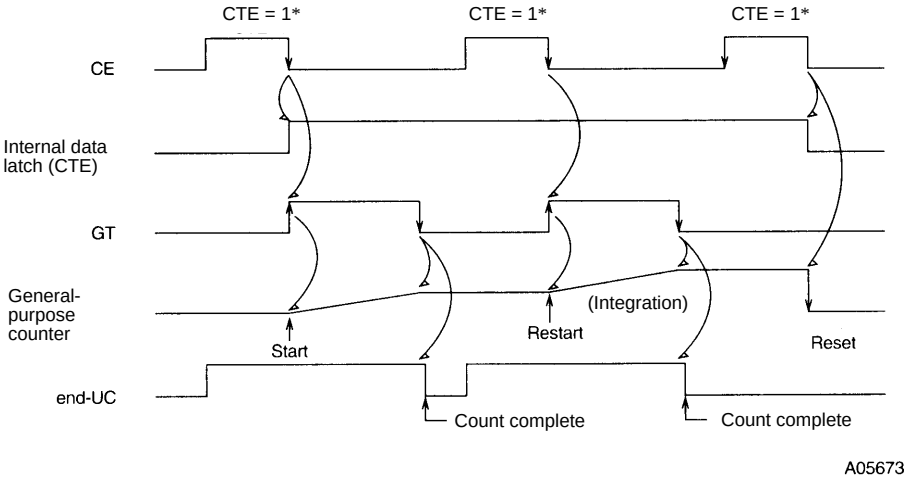
| GT1 | GT0 | Frequency measurement mode | | | Period measurement mode |
|---|---|---|---|---|---|
| | | Measurement time (ms) | Wait time (ms) | | |
| | | | CTP = 0 | CTP = 1 | |
| 0 | 0 | 4 | 3 to 4 | 1 to 2 | 1 period |
| 0 | 1 | 8 | 3 to 4 | 1 to 2 | 1 period |
| 1 | 0 | 32 | 7 to 8 | 1 to 2 | 2 periods |
| 1 | 1 | 64 | 7 to 8 | 1 to 2 | 2 periods |

## IF Counter Operation

Before starting a count operation with the general-purpose counter, reset that counter by setting CTE to 0.
A general-purpose counter count operation is started by setting the CTE bit in the serial data to 1. Although the serial data is loaded into the LC72144M internal registers by changing the level on the CE input pin from high to low, the input to the HCTR or LCTR pin must be provided within the wait period that follows the point when CE goes low at the latest.
Next, the count result in the general-purpose counter after the measurement completes must be read out in the period when CTE is 1, since the general-purpose counter is reset when CTE is set to 0.
Also note that although the signal input to the LCTR pin is transmitted directly to the general-purpose counter, the signal input to the HCTR pin is only transmitted to the general-purpose counter after first being divided by two internally. Thus the value of the result in the general-purpose counter is 1/2 the actual frequency of the signal input to the HCTR pin.




## Integrating Count



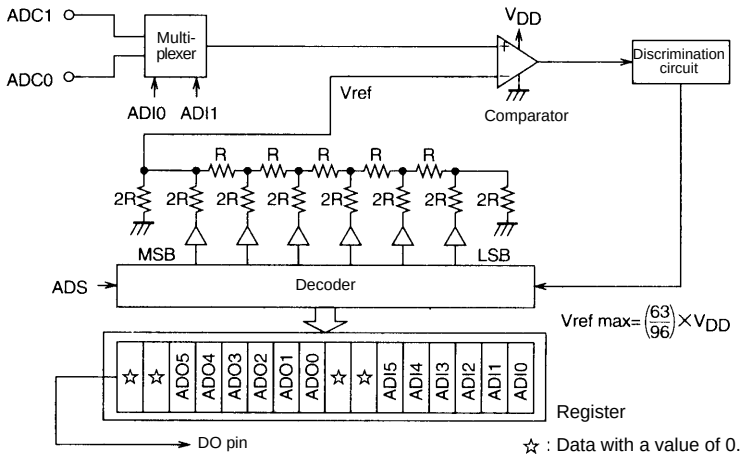

Note: CTE: 0 → • General-purpose counter reset

1 → { • General-purpose counter start
• Restarts on a new 1 setting

In integrated count mode, the count value is accumulated in the general-purpose counter.
Care is required to handle counter overflow.
Counter values: $0_H$ to $FFFFF_H$ (1,048,575)
To implement the integrating count operation leave CTE set to 1. When the serial data (IN1) is transmitted again, the general-purpose counter will start to measure the input again and the result will be added to the count.

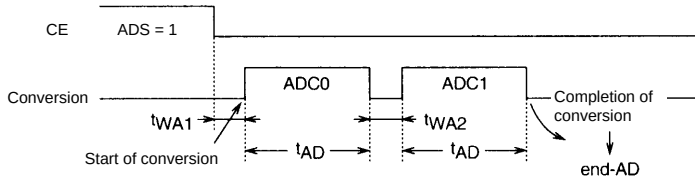
## Structure of the A/D Converter

The A/D converter is a 6-bit successive-approximation converter with a conversion time of 0.56 ms. The full-scale input level (for a data value of $3F_H$) is $(63/96) \times V_{DD}$.




A05674

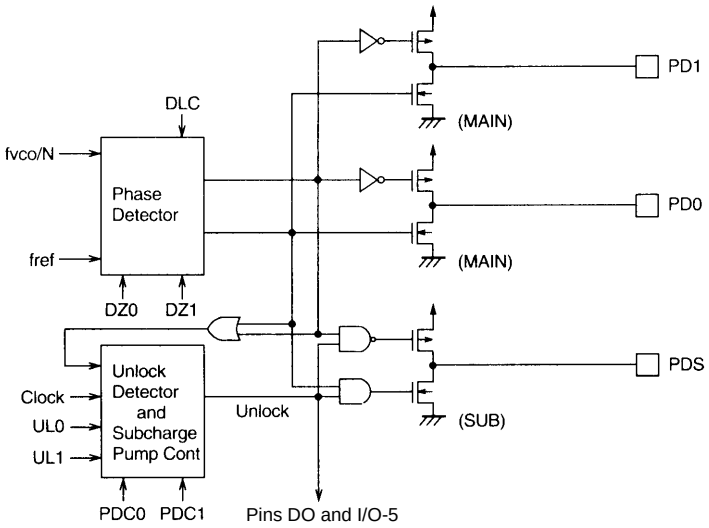
| ADI1 | ADI0 | Input pin |
|---|---|---|
| 1 | 1 | Illegal value |
| 1 | 0 | ADC0 |
| 0 | 1 | ADC1 |
| 0 | 0 | ADC0/ADC1 |




$T_{WA1}$ : 0.08 to 0.11 ms
$T_{WA1}$ : 0.08 to 0.09 ms
$T_{AD}$ : 0.56 to 0.62 ms

A05675

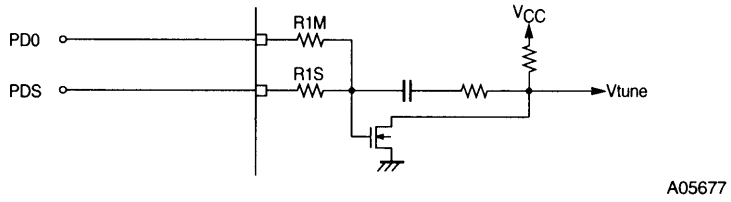
## Charge Pump




| PDC1 | PDC0 | PDS (sub-charge pump state) |
|---|---|---|
| 0 | × | High impedance |
| 1 | 0 | Charge pump operates (when unlocked) |
| 1 | 1 | Charge pump operates (normal operation) |

| DLC | PD1, PD0, PDS |
|---|---|
| 0 | Normal operation |
| 1 | Forced to low |

When unlock is detected following a channel change, PDS (the sub-charge pump) operates. The value of R1 changes to R1M // R1S (R1S ≈ 100 Ω), as shown in following figure, decreasing the low-pass filter time-constant and accelerating PLL locking.




The unlock detection data UL1 must be set to 1. The unlock detection range will be set to ±0.5 µs or ±1 µs. If a phase difference in excess of these values is detected the circuit will go to the unlock state and the sub-charge pump will operate. When the circuit approaches the lock state and the phase difference falls under the unlock detection range, the sub-charge pump operation will stop, i.e., the sub-charge pump will go to the high impedance state.

## Others

1. Notes on the phase comparator dead zone

| DZ1 | DZ0 | Dead zone mode | Charge pump | Dead zone |
|---|---|---|---|---|
| 0 | 0 | DZA | ON/ON | – –0 s |
| 0 | 1 | DZB | ON/ON | –0 s |
| 1 | 0 | DZC | OFF/OFF | +0 s |
| 1 | 1 | DZD | OFF/OFF | + +0 s |

Cases where the charge pump is in the ON/ON state require special care during system design since the charge pump outputs correction pulses even when the PLL is locked and it is easy for the loop to become unstable.
The following problems may occur in the ON/ON state.
① Sidebands may be generated by reference frequency leakage.
② Sidebands may be generated by low frequency leakage due to the correction pulse envelope.
The settings that have a dead zone (the OFF/OFF settings) provide good loop stability, but it is hard to achieve a good C/N ratio with these settings. Inversely, the settings with no dead zone (the ON/ON settings) allow a high C/N ratio to be achieved but it is hard to achieve good loop stability with these settings.
Therefore, it can be effective to select either the DZA or DZB setting, i.e., a setting which has no dead zone, when an S/N ratio of between 90 and 100 dB or higher is required in FM mode, or when the AM stereo pilot margin needs to be increased. However, in cases where such a high FM S/N ratio is not required and where an adequate AM stereo pilot margin can be achieved or AM stereo is not used, either the DZC or DZD setting, i.e., a setting which has a dead zone, should be selected.

Dead Zone Definition
The phase comparator compares fp with a reference frequency (fr) as shown in Figure 1. Figure 2 shows the characteristics of an ideal phase comparator, which outputs an output voltage (A) that is proportional to the phase difference ø. However, in an actual IC, a region (dead zone) in which minute phase differences cannot be detected occurs due to internal circuit delays and other factors (B). To implement an end product with a high S/N ratio, the dead zone should be as small as possible.
However, there are cases where a larger dead zone can make a popularly-priced model easier to use. This is because it is possible for RF leakage from the mixer to the VCO to modulate the VCO in popularly-priced models when a strong RF input is applied. When the dead zone is small an output that compensates for this problem is generated, and this output may itself modulate the VCO and generate beating with the RF frequency.

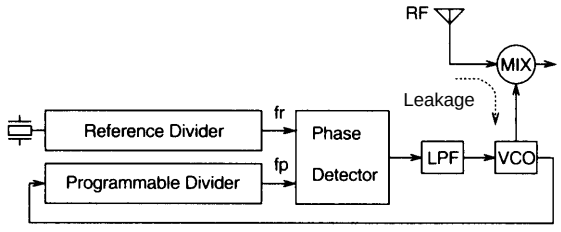



**Figure 1**

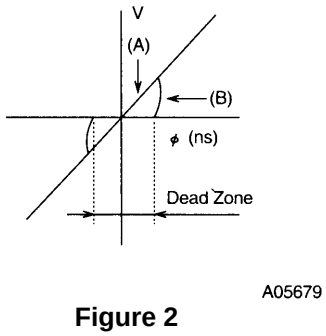



**Figure 2**

2. Notes on the FMIN, AMIN, HCTR/I-6, and LCTR/I-7 Pins
   The coupling capacitors must be placed as close to the pin as possible. A capacitance of about 100 pF is desirable. In particular, only use capacitances of under 1000 pF with the HCTR/I-6, and LCTR/I-7 pins. Large capacitances will increase the time required for the pin to reach the bias level and, depending on the relationship with the wait time, may cause counting errors.

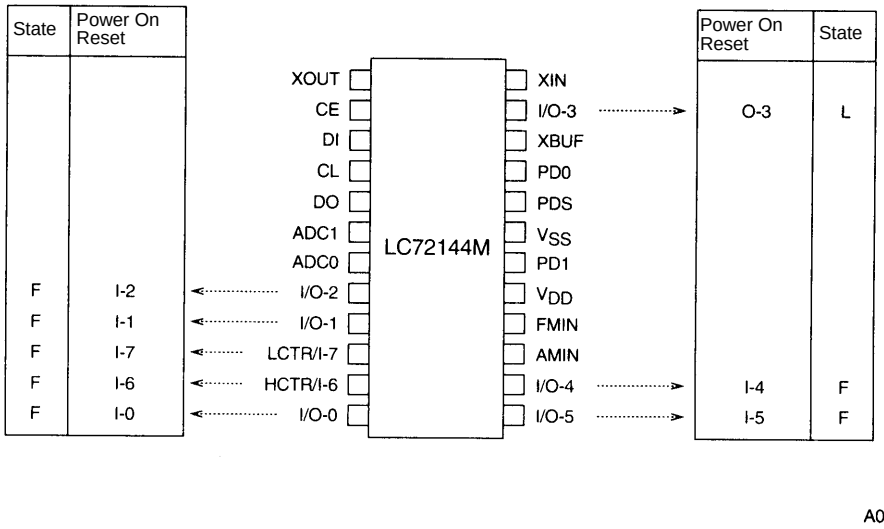
3. Notes on IF counting → SD must be used together with IF counting
   When using the general-purpose counter for IF counting, always use the IF-IC SD (station detect) signal. The microcontroller should first check for the presence of the SD signal, and then turn on the IF count buffer only if that signal is present to perform an IF count. Techniques that use only an IF count to implement an autosearch function are dangerous because they may stop at frequencies that do not have a station due to leakage from the IF count buffer.

4. Using the DO pin
   In modes other than data output mode, the DO pin is also used for counter completion, unlock detection, and for checking for changes in the input pin.
   The state of the input pin (I/O-1, I/O-2) can be input to the controller directly through the DO pin.

5 Notes on using XBUF
   When the XBUF output is turned on (when AM up-conversion is used), since the XBUF signal leaks into adjacent pins, the pins PD0 and I/O-3, which are adjacent to XBUF, must not be used for AM reception control. Use the PD1 pin for the AM reception charge pump. Turn off the XBUF output (by setting the XB data to 0) when using PD0 and I/O-3 for FM reception control.

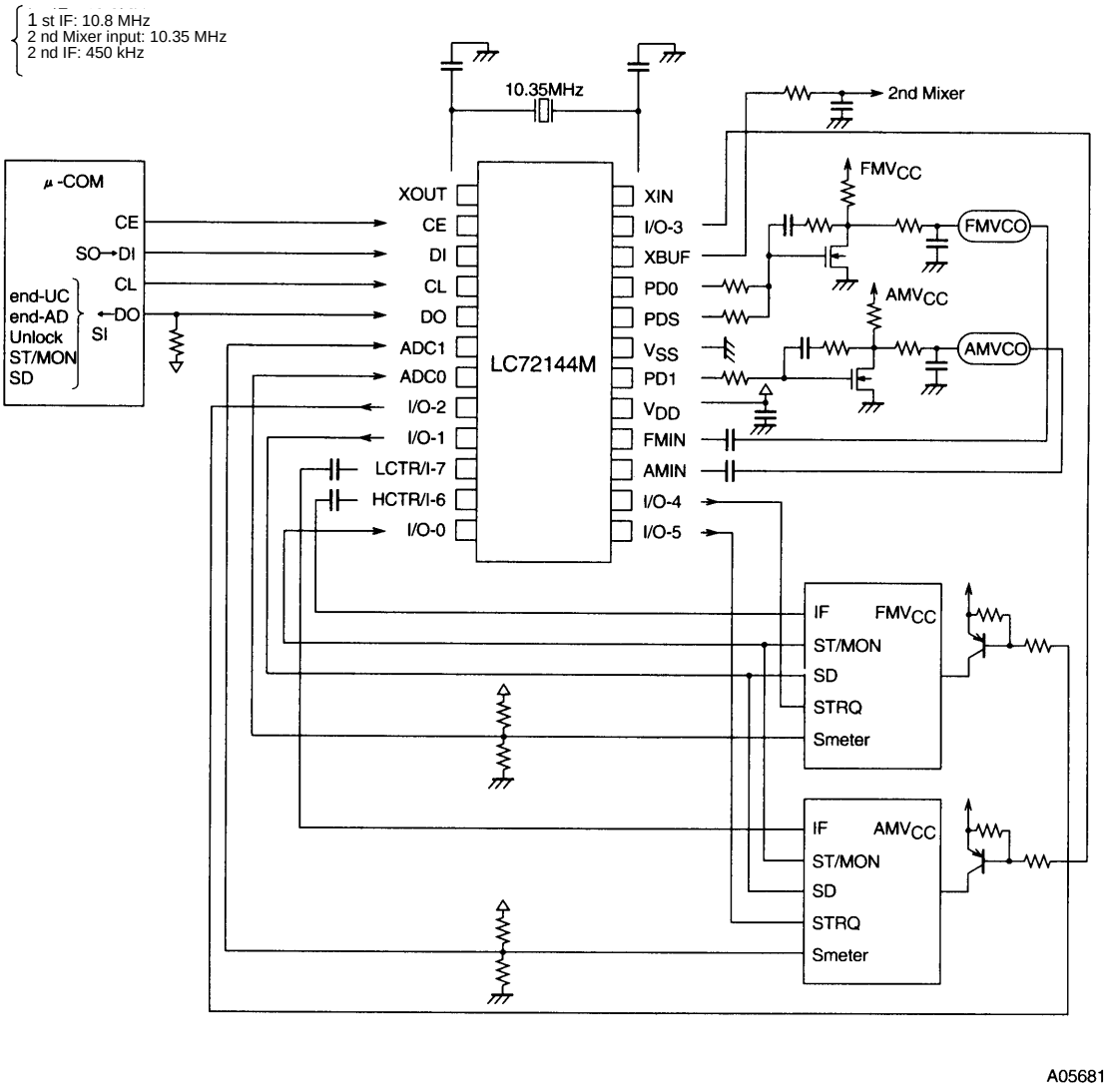
6 Power supply pins
   To exclude noise, a capacitor of at least 2000 pF must be inserted between the power supply $V_{DD}$ and $V_{SS}$ lines. Locate this capacitor as close to the chip's $V_{DD}$ and $V_{SS}$ pins as possible.

### Pin States at Power On and Reset




F: Floating
L: Low

## Application System Example




A05681