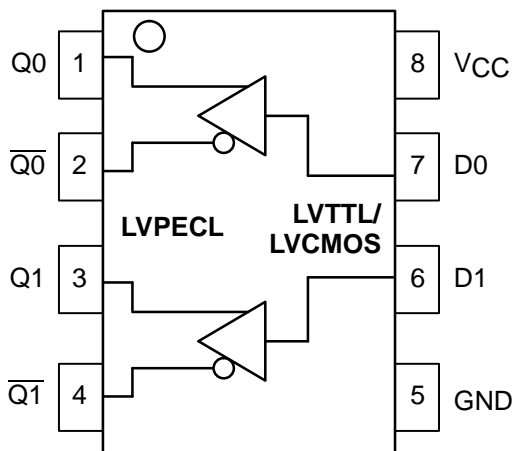


# Dual LVTTTL/LVCMOS to Differential LVPECL Translator

The MC100LVELT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

- 350ps Typical Propagation Delay
- <100ps Output-to-Output Skew
- Differential LVPECL Outputs
- Small Outline SOIC Package
- Flow Through Pinouts

### LOGIC DIAGRAM AND PINOUT ASSIGNMENT



## MC100LVELT22



**D SUFFIX**  
8-LEAD PLASTIC SOIC PACKAGE  
CASE 751-05

### PIN DESCRIPTION

PIN	FUNCTION
Qn	Diff PECL Outputs
Dn	LVTTTL/LVCMOS Inputs
VCC	+3.3V Supply
GND	Ground



# MC100LVELT22

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	7.0	V
V <sub>IN</sub>	Input Voltage	0 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current Applied to Output in Low Output State	50 100	mA
	Continuous Surge		
T <sub>A</sub>	Operating Temperature Range (In Free-Air)	-40 to 85	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## LVTTTL/LVCMOS INPUT DC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ±5%; T<sub>A</sub> = -40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>IN</sub> = 2.7V
I <sub>IHH</sub>	Input HIGH Current			100	μA	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current			-0.2	mA	V <sub>IN</sub> = 0.5V
V <sub>IK</sub>				-1.2	V	I <sub>IN</sub> = -18mA
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	

## LVPECL OUTPUT DC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ±5%; T<sub>A</sub> = -40°C to 85°C)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V <sub>OH</sub>	Output HIGH Voltage	2.275	2.420	2.275	2.420	2.275	2.345	2.420	2.275	2.420	V	V <sub>CC</sub> = 3.3V Note 1.
V <sub>OL</sub>	Output LOW Voltage	1.490	1.680	1.490	1.680	1.490	1.595	1.680	1.490	1.680	V	V <sub>CC</sub> = 3.3V Note 1.
I <sub>CC</sub>	Power Supply Current		23		23			23		24	mA	

1. Levels will vary 1:1 with V<sub>CC</sub>.

## AC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ±5%; T<sub>A</sub> = -40°C to 85°C)

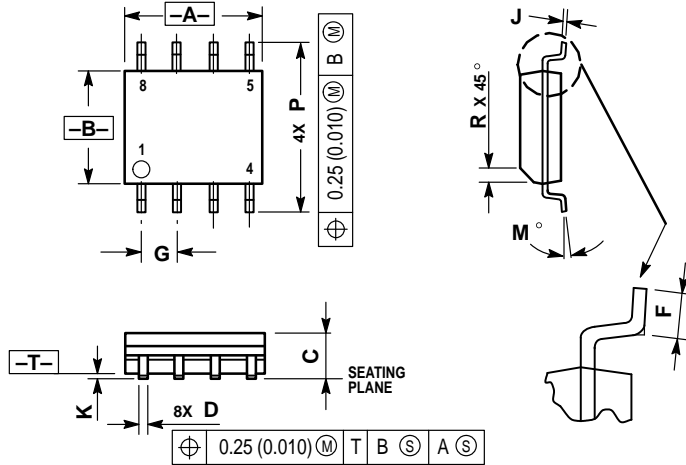
Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	200	600	200	600	200	350	600	200	600	ps	Note 2.
t <sub>skew</sub>	Skew Output-to-Output Part-to-Part		100 400		100 400		30	100 400		100 400	ps	
t <sub>r</sub> /t <sub>f</sub>	Output Rise/Fall Time	250	550	200	500	200		500	200	500	ps	20-80%
f <sub>MAX</sub>	Maximum Input Frequency	300		300		300			300		MHz	Note 3.

2. Specifications for standard TTL input signal.

3. f<sub>MAX</sub> specification is set to anticipated input frequency limitations.

OUTLINE DIMENSIONS


D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-05  
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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