SONY

CXA2557R

RF Amplifier for CD Player/CD-ROM

Description

The CXA2557R is an RF signal processing IC for CD players, CD-ROM and CD-RW (playback).

Features

- Wide-band RF AC amplifier
- Supports CD-RW playback (RF DC, RF AC, FE, TE and AL amplifiers)
- 5-mode RF AC equalizer (active filter type)
- RF AC equalizer boost amount and cut-off frequency adjustable
- Voltage gain adjustable for RF DC, RF AC, FE, TE and AL amplifier
- RF DC amplifier offset voltage switchable
- FE and TE amplifier bias voltage adjustable
- Tracking error amplifier cut-off frequency adjustable
- Alignment amplifier
- Center error amplifier
- AGC (Automatic Gain Control) function
- APC (Automatic Power Control) function
- VC/VC IN separation
- Supports laser coupler/3 spots

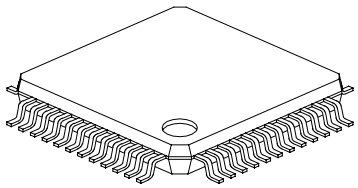
Functions

- RF DC summing amplifier
- RF AC summing amplifier
- RF AC equalizer
- Focus error (FE) amplifier
- Tracking error (TE) amplifier
- Alignment (AL) amplifier
- Center error (CE) amplifier
- Mirror circuit
- AGC circuit
- VREF output

Applications

- CD players
- CD-ROM drives

48 pin LQFP (Plastic)



Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

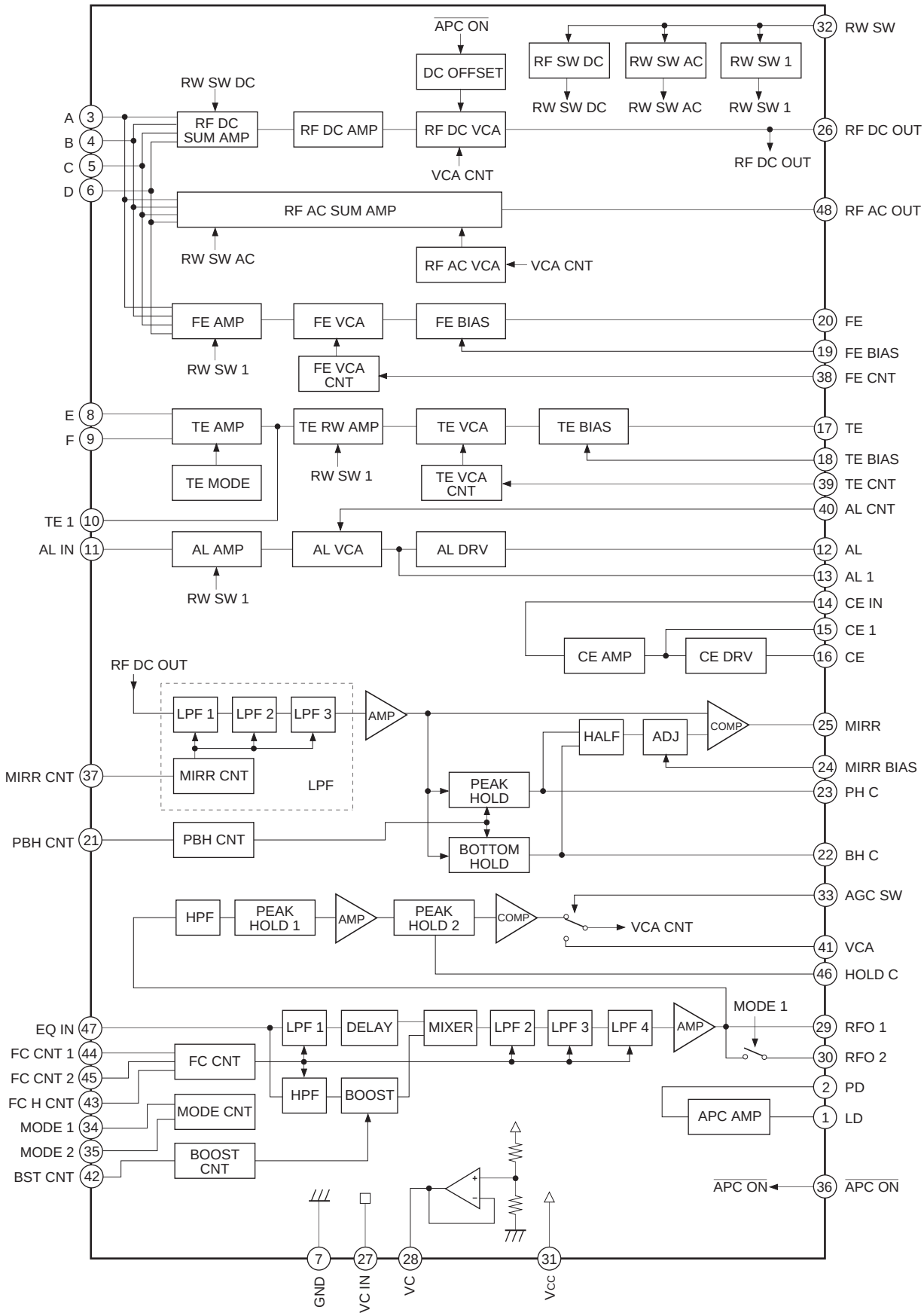
• Supply voltage	V_{CC} – GND	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Power consumption	P_D	400	mW

Operating Conditions (Ta = 25°C)

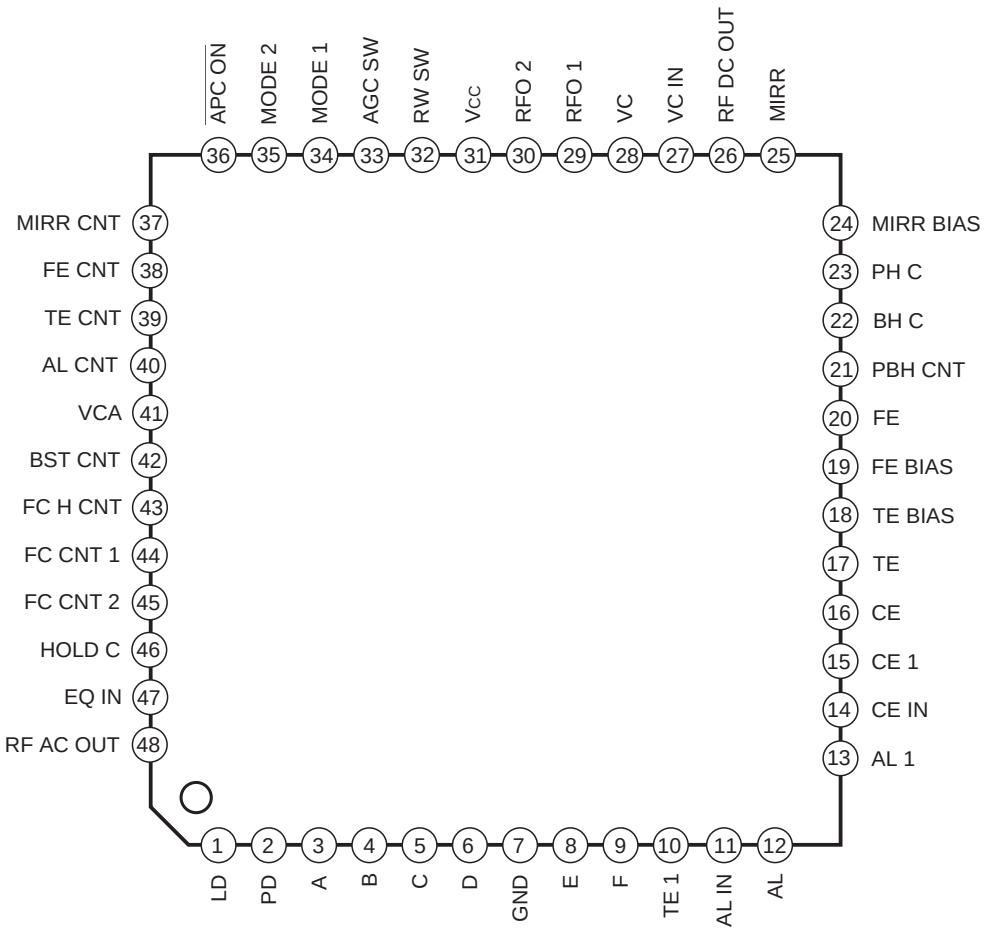
• Supply voltage	V_{CC} – GND	3.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

E97757-PS

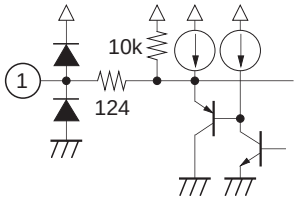
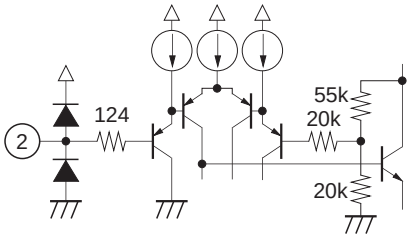
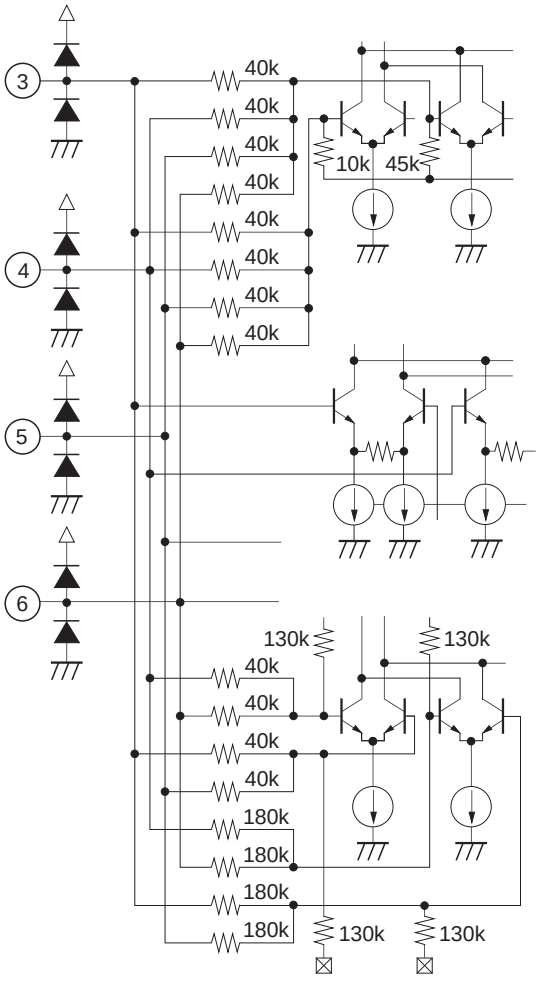
Block Diagram

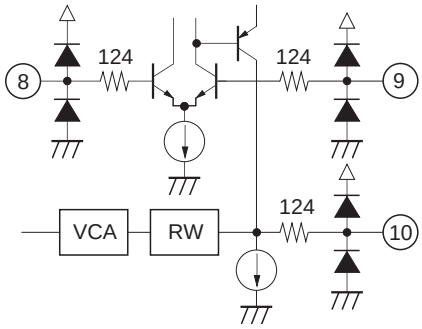
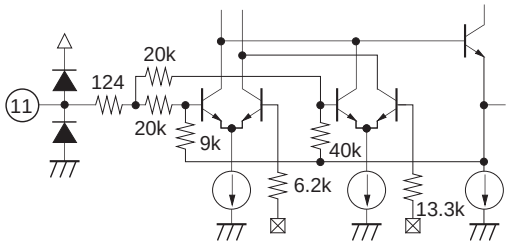
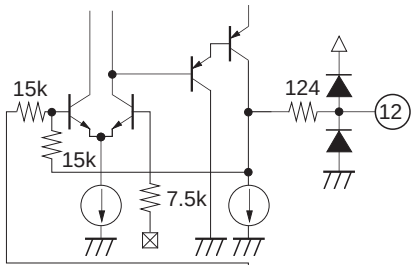
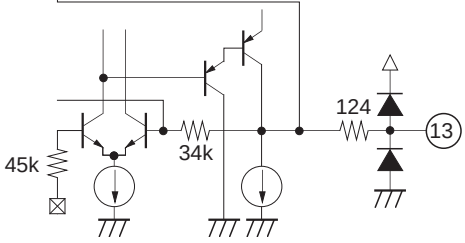
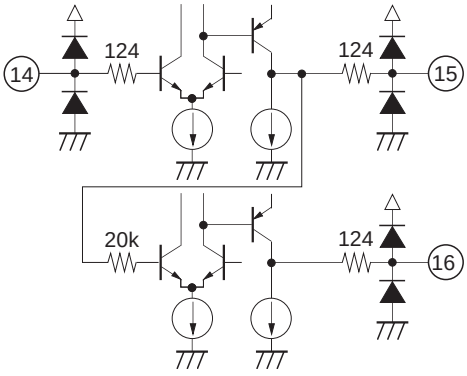


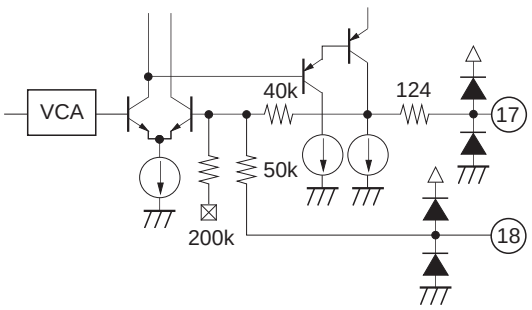
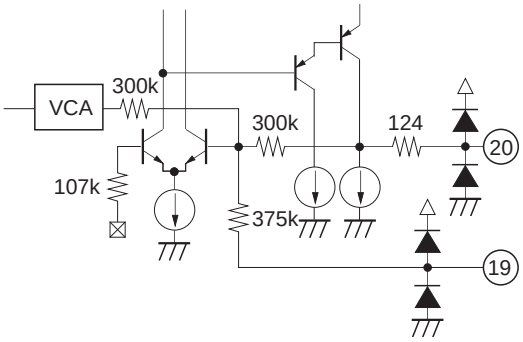
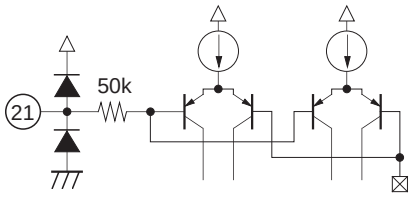
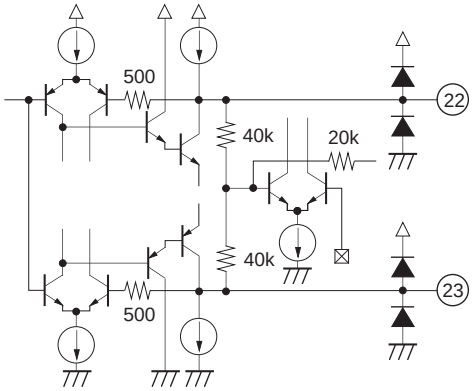
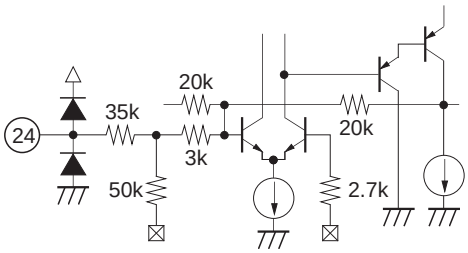
Pin Configuration

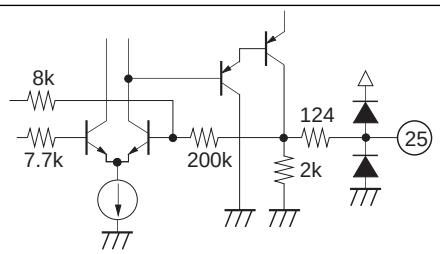
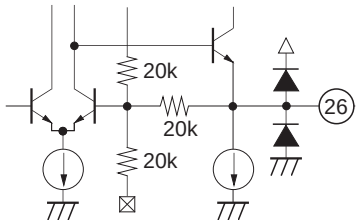
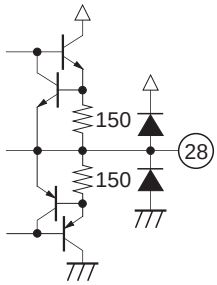
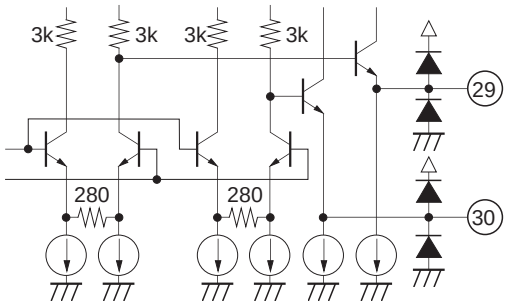


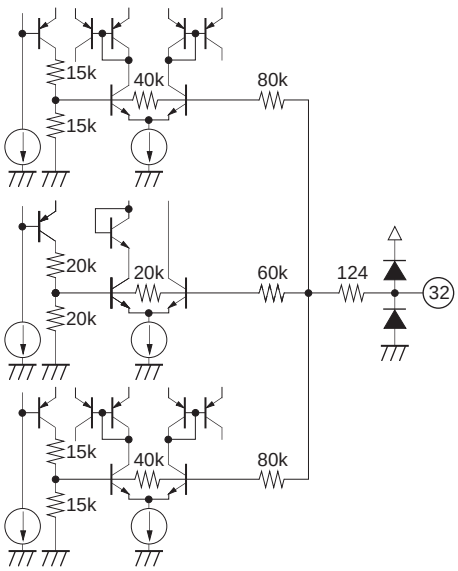
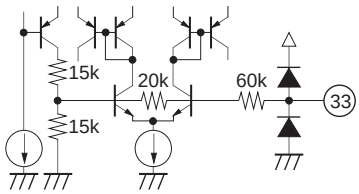
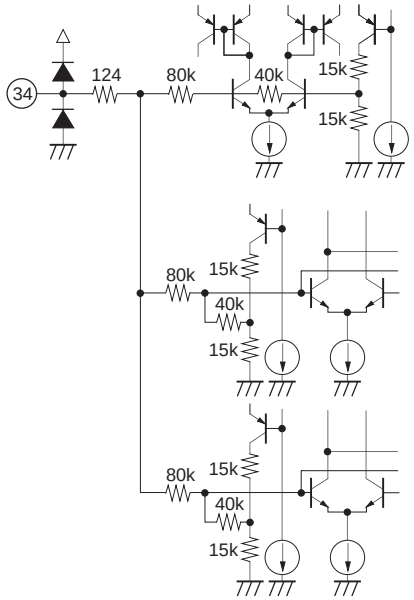
Pin Description

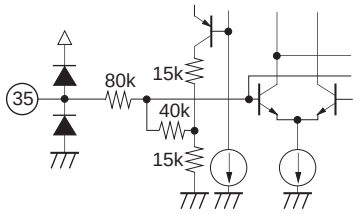
Pin No.	Symbol	I/O	Equivalent circuit	Description
1	LD	O		APC amplifier output.
2	PD	I		APC amplifier input.
3 4 5 6	A B C D	I I I I		Inputs of RF summing amplifier and focus error amplifier. When using a laser coupler: A + C = PD1 B + D = PD2
7	GND		—	Ground.

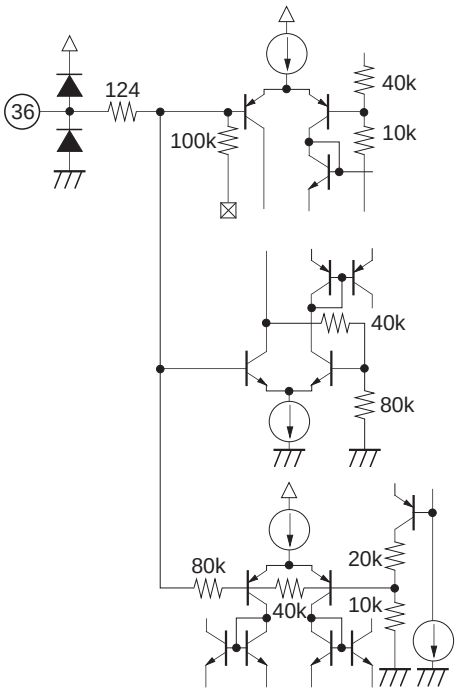
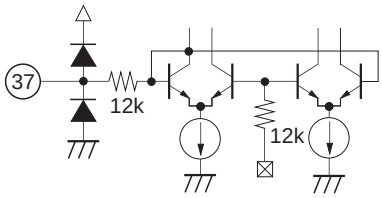
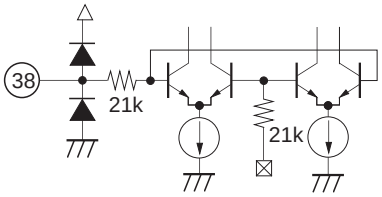
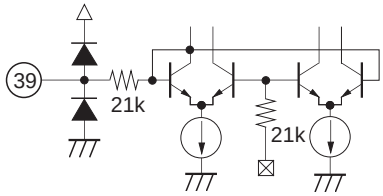
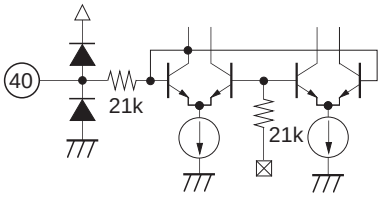
Pin No.	Symbol	I/O	Equivalent circuit	Description
8 9	E F	I I		Tracking error amplifier inputs.
10	TE 1	O		Tracking error amplifier inverted output.
11	AL IN	I		Alignment amplifier input.
12	AL	O		Alignment amplifier non-inverted output.
13	AL 1	O		Alignment amplifier inverted output.
14	CE IN	I		Center error amplifier input.
15	CE 1	O		Center error amplifier inverted output.
16	CE	O		Center error drive amplifier inverted output.

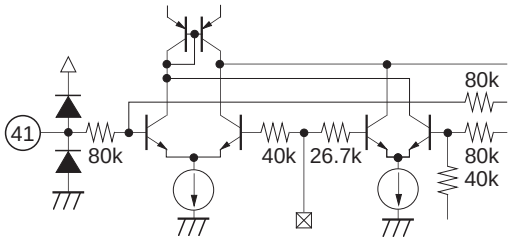
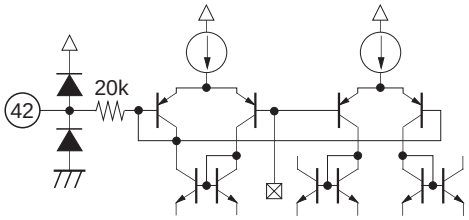
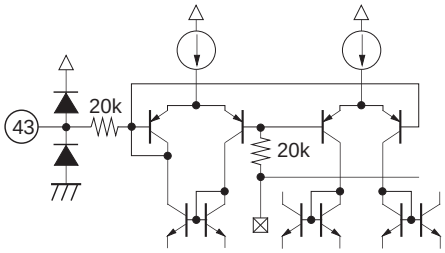
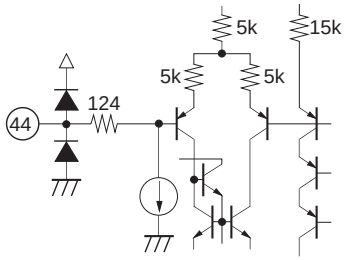
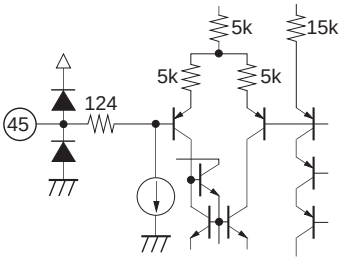
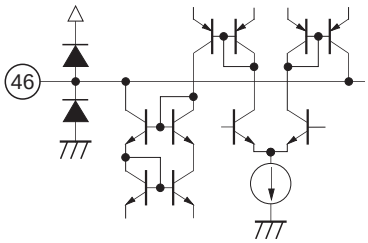
Pin No.	Symbol	I/O	Equivalent circuit	Description
17	TE	O		Tracking error amplifier non-inverted output.
18	TE BIAS	I		Tracking error amplifier bias adjustment.
19	FE BIAS	I		Focus error amplifier bias adjustment.
20	FE	O		Focus error amplifier non-inverted output.
21	PBH CNT	I		Mirror circuit peak hold and bottom hold time constant setting input.
22	BC C	I		Connects the capacitor that sets mirror circuit bottom hold time constant.
23	PH C	I		Connects the capacitor that sets mirror circuit peak hold time constant.
24	MIRR BIAS	I		Mirror circuit bias adjustment.

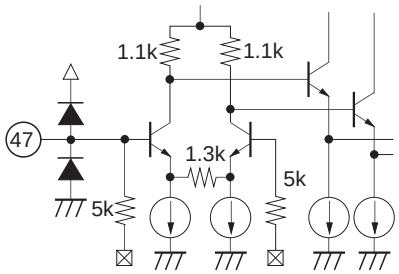
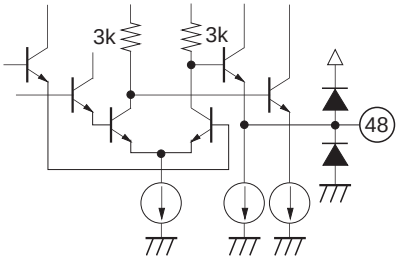
Pin No.	Symbol	I/O	Equivalent circuit	Description
25	MIRR	O		Mirror comparator output.
26	RF DC OUT	O		RF DC amplifier output. Eye pattern check point.
27	VC IN	I	—	Reference voltage input.
28	VC	O		(V_{CC} + GND)/2 voltage output.
29	RFO 1	O		RF AC amplifier output.
30	RFO 2	O		RF AC amplifier buffer switch output. ON when Pin 34 is connected to GND.
31	V_{CC}	—	—	Power supply.

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>32</td><td>RW SW</td><td>I</td><td> 
</td><td>CD-ROM/RW switching input.
RW when connected to Vcc,
ROM when connected to GND.</td></tr>
<tr><td>33</td><td>AGC SW</td><td>I</td><td> 
</td><td>AGC/VCA switching input.
AGC when connected to Vcc,
VCA when connected to GND.</td></tr>
<tr><td>34</td><td>MODE 1</td><td>I</td><td rowspan="2"> 
</td><td rowspan="2">Double-speed mode switching pins.
<table>
<tr><th>MODE 1</th><th>MODE 2</th><th>fc</th></tr>
<tr><td>L</td><td>X</td><td>× n</td></tr>
<tr><td rowspan="3">M</td><td>L</td><td>× 2n</td></tr>
<tr><td>M</td><td>× 4n</td></tr>
<tr><td>H</td><td>× 6n</td></tr>
<tr><td>H</td><td>X</td><td>× N</td></tr>
</table>
* X = L or M or H
n is determined by the external resistor connected to Pin 44.
N is determined by the external resistor connected to Pin 45 and the Pin 43 input voltage.

Pin 34 also serves as switching pin for the tracking error amplifier cut-off frequency and RFO2 output ON/OFF switching pin.
<table>
<tr><th>MODE 1</th><th>MODE 2</th><th>fc</th></tr>
<tr><td>L</td><td>20kHz</td><td>ON</td></tr>
<tr><td>M</td><td rowspan="2">250kHz</td><td rowspan="2">OFF</td></tr>
<tr><td>H</td></tr>
</table>
* L = GND, M = VC, H = Vcc</td></tr>
<tr><td>35</td><td>MODE 2</td><td>I</td><td> 
</td></tr>
</table>

Pin No.	Symbol	I/O	Equivalent circuit	Description
36	$\overline{\text{APC ON}}$	I		Switching pin for RF DC amplifier offset setting. No addition to RF DC amplifier when Medium (VC). Vcc/6 added to RF DC amplifier when Low (GND).
37	MIRR CNT	I		Mirror circuit LPF cut-off frequency setting input.
38	FE CNT	I		Focus error amplifier gain adjustment input.
39	TE CNT	I		Tracking error amplifier gain adjustment input.
40	AL CNT	I		Alignment amplifier gain adjustment input.

Pin No.	Symbol	I/O	Equivalent circuit	Description
41	VCA	I		RF DC and RF AC amplifier gain adjustment input. AGC circuit target voltage input when AGC SW is ON.
42	BST CNT	I		Equalizer circuit boost amount adjustment input.
43	FC H CNT	I		Cut-off frequency N adjustment input when Pin 34 is High.
44	FC CNT 1	I		Connects the external resistor that sets cut-off frequency n when Pin 34 is Low or Medium.
45	FE CNT 2	I		Connects the external resistor that sets cut-off frequency N when Pin 34 is High.
46	HOLD C	I		Connects the capacitor that sets AGC time constant.

Pin No.	Symbol	I/O	Equivalent circuit	Description
47	EQ IN	I		Equalizer circuit input.
48	RF AC OUT	O		RF AC summing amplifier non-inverted output.

Electrical Characteristics

(Ta = 25°C, V_{CC} = 1.9V, GND = VC, V_{EE} = –1.9V)

No.	Measurement item				SW conditions	Bias conditions (V)		Input	Output *IC pin No.		Ratings			
						E1	E2				Min.	Typ.	Max.	Unit
1	VC		Output voltage	V_{VCB}					28		–20.0	0.0	20.0	mA
2	Current consumption		Current consumption	I_{CC}					31		43.0	64.0	85.0	mA
3	Current consumption		Current consumption	I_{EE}					7		–85.0	–64.0	–43.0	mA
4	Offset voltage	RF DC	Output offset voltage 1	V_{RFD1}					26		–680.0	–560.0	–440.0	mV
5			Output offset voltage 2	V_{RFD2}	S16				↓		–640.0	–520.0	–400.0	mV
6			Output offset voltage 3	V_{RFD3}	S20-b				↓		–68.0	52.0	172.0	mV
7		RF AC	Output offset voltage 1	V_{RFA1}					48		–215.0	–135.0	–55.0	mV
8			Output offset voltage 2	V_{RFA2}	S16				↓		–210.0	–130.0	–50.0	mV
9		FE	Output offset voltage 1	V_{FE1}					20		–57.0	23.0	103.0	mV
10			Output offset voltage 2	V_{FE2}	S16				↓		–60.0	20.0	100.0	mV
11		TE	Output offset voltage 1	V_{TE1}					17		–210.0	–80.0	50.0	mV
12			Output offset voltage 2	V_{TE2}	S16				↓		–210.0	–80.0	50.0	mV
13		AL	Output offset voltage 1	V_{AL1}					12		–10.0	50.0	110.0	mV
14			Output offset voltage 2	V_{AL2}	S16				↓		–10.0	50.0	110.0	mV
15			Output offset voltage 3	V_{AL3}					13		–110.0	–50.0	10.0	mV
16			Output offset voltage 4	V_{AL4}	S16				↓		–110.0	–50.0	10.0	mV
17		CE	Output offset voltage	V_{CE}					16		–30.0	20.0	70.0	mV
18	RF DC		Voltage gain 1	G_{RFD1}	S2, S3, S4, S5			100kHz 80mVp-p	26		13.8	16.8	19.8	dB
19			VCA gain 1	G_{RFDV1}	S2, S3, S4, S5, S25		1.0	↓		G_{RFDV1} (TS) – G_{RFD1}	5.0	8.0	11.0	dB
20			VCA gain 2	G_{RFDV2}	S2, S3, S4, S5, S25		–1.0	↓		G_{RFDV2} (TS) – G_{RFD1}	–11.0	–8.0	–5.0	dB
21			Voltage gain 2	G_{RFD2}	S2, S3, S4, S5, S16			100kHz 18mVp-p		G_{RFD2} (TS) – G_{RFD1}	10.0	13.0	16.0	dB
22			VCA gain 3	G_{RFDV3}	S2, S3, S4, S5, S16, S25		1.0	↓		G_{RFDV3} (TS) – G_{RFD2} (TS)	5.0	8.0	11.0	dB
23			VCA gain 4	G_{RFDV4}	S2, S3, S4, S5, S16, S25		–1.0	↓	↓	G_{RFDV4} (TS) – G_{RFD2} (TS)	–11.0	–8.0	–5.0	dB

(Ta = 25°C, V_{CC} = 1.9V, GND = VC, V_{EE} = –1.9V)

No.	Measurement item			SW conditions	Bias conditions (V)		Input	Output *IC pin No.		Ratings			
					E1	E2				Min.	Typ.	Max.	Unit
24	RF DC	Output voltage High	V_{RFDH}	S2, S3, S4, S5			1.0V DC	26		990.0	1100.0	—	mV
25		Output voltage Low	V_{RFDL}	S2, S3, S4, S5			–1.0V DC	↓		—	–1790.0	–1680.0	mV
26	RF AC	Voltage gain 1	G_{RFA1}	S2, S3, S4, S5			100kHz 170mVp-p	48		0.7	2.7	4.7	dB
27		VCA gain 1	V_{RFA1}	S2, S3, S4, S5, S25		1.0	↓	↓	V_{RFA1} (TS) – G_{RFA1}	6.0	8.0	10.0	dB
28		VCA gain 2	V_{RFA2}	S2, S3, S4, S5, S25		–1.0	↓	↓	V_{RFA2} (TS) – G_{RFA1}	–10.0	–8.0	–6.0	dB
29		Voltage gain 2	G_{RFA2}	S2, S3, S4, S5, S16			100kHz 38mVp-p	↓	G_{RFA2} (TS) – G_{RFA1}	8.1	10.1	12.1	dB
30		VCA gain 3	V_{RFA3}	S2, S3, S4, S5, S16, S25		1.0	↓	↓	V_{RFA3} (TS) – G_{RFA2} (TS)	5.5	7.5	9.5	dB
31		VCA gain 4	V_{RFA4}	S2, S3, S4, S5, S16, S25		–1.0	↓	↓	V_{RFA4} (TS) – G_{RFD2} (TS)	–9.5	–7.5	–5.5	dB
32		Output voltage High	V_{RFAH1}	S2, S3, S4, S5			1.0V DC	↓		260.0	370.0	480.0	mV
33		Output voltage Low	V_{RFAL1}	S2, S3, S4, S5			–1.0V DC	↓		–730.0	–620.0	–510.0	mV
34	FE	Voltage gain 1	G_{FE1}	S2, S4			1kHz 189mVp-p	20		13.0	16.0	19.0	dB
35		Voltage gain 2	G_{FE2}	S3, S5			↓	↓		13.0	16.0	19.0	dB
36		VCA gain 1	G_{FEV1}	S3, S5, S22		1.0	↓	↓	G_{FEV1} (TS) – G_{FE2}	5.0	8.0	11.0	dB
37		VCA gain 2	G_{FEV2}	S3, S5, S22		–1.0	↓	↓	G_{FEV2} (TS) – G_{FE2}	–11.0	–8.0	–5.0	dB
38		Frequency response	F_{FE}	S3, S5			25kHz 189mVp-p	↓	F_{FE1} (TS) – G_{FE2}	–3.0	—	—	dB
39		Voltage gain 3	G_{FE3}	S2, S4, S16			1kHz 42mVp-p	↓	G_{FE3} (TS) – G_{FE1}	10.0	13.0	16.0	dB
40		Voltage gain 4	G_{FE4}	S3, S5, S16			↓	↓	G_{FE4} (TS) – G_{FE2}	10.0	13.0	16.0	dB
41		VCA gain 3	G_{FEV3}	S3, S5, S16, S22		1.0	↓	↓	G_{FEV3} (TS) – G_{FE4} (TS)	5.0	8.0	11.0	dB
42		VCA gain 4	G_{FEV4}	S3, S5, S16, S22		–1.0	↓	↓	G_{FEV4} (TS) – G_{FE4} (TS)	–11.0	–8.0	–5.0	dB
43		Bias characteristics 1	B_{FE1}	S11	1.0		↓	↓	B_{FE1} (TS) – V_{FE1}	–1290.0	–1180.0	–1070.0	mV
44		Bias characteristics 2	B_{FE2}	S11	–1.0		↓	↓	B_{FE2} (TS) – V_{FE1}	1070.0	1180.0	1290.0	mV
45		Output voltage High	V_{FEH}	S3, S5			1.9V DC	↓		1660.0	1770.0	—	mV
46		Output voltage Low	V_{FEL}	S3, S5			–1.9V DC	↓		—	–1680.0	–1570.0	mV

(Ta = 25°C, V_{CC} = 1.9V, GND = VC, V_{EE} = –1.9V)

No.	Measurement item			SW conditions	Bias conditions (V)		Input	Output *IC pin No.		Ratings			
					E1	E2				Min.	Typ.	Max.	Unit
47	TE	Voltage gain 1	G_{TE1}	S7, S18-c			1kHz 107mVp-p	17		17.9	20.9	23.9	dB
48		Voltage gain 2	G_{TE2}	S6, S18-c			↓	↓		17.9	20.9	23.9	dB
49		VCA gain 1	G_{TEV1}	S7, S18-c, S23		1.0	↓	↓	G_{TEV1} (TS) – G_{TE1}	4.8	8.3	11.8	dB
50		VCA gain 2	G_{TEV2}	S7, S18-c, S23		–1.0	↓	↓	G_{TEV2} (TS) – G_{TE1}	–12.1	–8.6	–5.1	dB
51		Frequency response 1	F_{TE1}	S7, S18-c			250kHz 107mVp-p	↓	F_{TE1} (TS) – G_{TE1} (TE)	–3.0	—	—	dB
52		Frequency response 2	F_{TE2}	S7			20kHz 107mVp-p	↓	F_{TE2} (TS) – G_{TE1} (TE)	–3.0	—	—	dB
53		Voltage gain 3	G_{TE3}	S7, S16, S18-c			1kHz 20mVp-p	↓	G_{TE3} (TS) – G_{TE1}	10.0	13.0	16.0	dB
54		Voltage gain 4	G_{TE4}	S6, S16, S18-c			↓	↓	G_{TE4} (TS) – G_{TE2}	10.0	13.0	16.0	dB
55		VCA gain 3	G_{TEV3}	S7, S16, S18-c, S23		1.0	↓	↓	G_{TEV3} (TS) – G_{TE3} (TE)	4.9	8.4	11.9	dB
56		VCA gain 4	G_{TEV4}	S7, S16, S18-c, S23		–1.0	↓	↓	G_{TEV4} (TS) – G_{TE3} (TE)	–12.2	–8.7	–5.2	dB
57		Bias characteristics 1	B_{TE1}	S10, S18-c	1.0		↓	↓	B_{TE1} (TS) – V_{TE1}	–890.0	–780.0	–670.0	mV
58		Bias characteristics 2	B_{TE2}	S10, S18-c	–1.0		↓	↓	B_{TE2} (TS) – V_{TE1}	670.0	780.0	890.0	mV
59		Output voltage High	V_{TEH1}	S7, S18-c			1.9V DC	↓		1550.0	1660.0	—	mV
60		Output voltage Low	V_{TEL1}	S7, S18-c			–1.9V DC	↓		—	–1760.0	–1650.0	mV
61	AL	Voltage gain 1	G_{AL1}	S8			1kHz 700mVp-p	12		–3.6	–0.6	2.4	dB
62		Voltage gain 2	G_{AL2}	S8			↓	13		–3.6	–0.6	2.4	dB
63		VCA gain 1	G_{ALV1}	S8, S24		1.0	↓	12	G_{ALV1} (TS) – G_{AL1}	4.3	8.0	11.5	dB
64		VCA gain 2	G_{ALV2}	S8, S24		–1.0	↓	↓	G_{ALV2} (TS) – G_{AL1}	–11.9	–8.4	–4.9	dB
65		Frequency response 1	F_{AL1}	S8			30kHz 700mVp-p	12	F_{AL1} (TS) – G_{AL1}	–2.0	—	—	dB
66		Frequency response 2	F_{AL2}	S8			↓	13	F_{AL2} (TS) – G_{AL3}	–2.0	—	—	dB
67		Voltage gain 3	G_{AL3}	S8, S16			1kHz 156mVp-p	12	G_{AL3} (TS) – G_{AL1}	10.0	13.0	16.0	dB
68		Voltage gain 4	G_{AL4}	S8, S16			↓	13	G_{AL4} (TS) – G_{AL3}	10.0	13.0	16.0	dB
69		VCA gain 3	G_{ALV3}	S8, S16, S24		1.0	↓	12	G_{ALV3} (TS) – G_{AL3} (TS)	4.5	8.0	11.5	dB
70		VCA gain 4	G_{ALV4}	S8, S16, S24		–1.0	↓	↓	G_{ALV4} (TS) – G_{AL3} (TS)	–11.9	–8.4	–4.9	dB

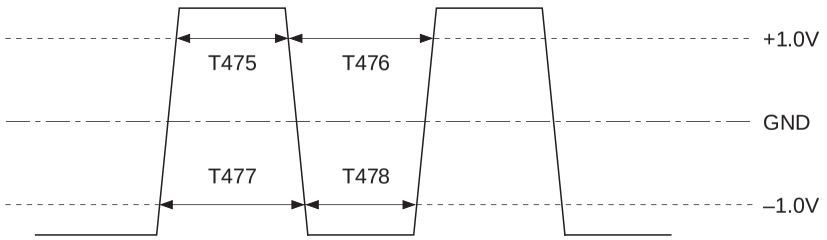
(Ta = 25°C, V_{CC} = 1.9V, GND = VC, V_{EE} = –1.9V)

No.	Measurement item			SW conditions	Bias conditions (V)		Input	Output *IC pin No.		Ratings			
					E1	E2				Min.	Typ.	Max.	Unit
71	AL	Output voltage High 1	V_{ALH1}	S8			1.9V DC	12		1580.0	1690.0	—	mV
72		Output voltage Low 1	V_{ALL1}	S8			–1.9V DC	↓		—	–1680.0	–1540.0	mV
73		Output voltage High 2	V_{ALH2}	S8			1.9V DC	13		—	–1720.0	–1580.0	mV
74		Output voltage Low 2	V_{ALL2}	S8			–1.9V DC	↓		1570.0	1690.0	—	mV
75	CE	Voltage gain	G_{CE}	S9			1kHz 260mVp-p	16		17.0	20.0	23.0	dB
76		Frequency response	F_{CE}	S9			30kHz 260mVp-p		F_{CE} (TS) – G_{CE}	–3.0	—	—	dB
77		Output voltage High	V_{CEH}	S9			1.9V DC			1680.0	1790.0	—	mV
78		Output voltage Low	V_{CEL}	S9			–1.9V DC	↓		—	–1580.0	–1090.0	mV
79	APC	Input voltage	V_{APCIN}	S1			adjust Input voltage	1	Output voltage = 0V	–1780.0	–1730.0	–1680.0	mV
80		Output voltage 1	V_{APC1}	S1			V_{APCIN} + 100mV			1650.0	1760.0	1870.0	mV
81		Output voltage 2	V_{APC2}	S1			V_{APCIN} – 100mV			–1180.0	–1070.0	–960.0	mV
82		Output voltage 3	V_{APC3}	S1, S20-c			V_{APCIN}	↓		1700.0	1800.0	—	mV
83	EQ	Voltage gain 1	G_{EQ1}	S29			1kHz 45mVp-p	29		16.5	19.0	21.5	dB
84		Voltage gain 2	G_{EQ2}	S29			↓	30		15.6	18.1	20.6	dB
85		Output voltage High 1	V_{EQH1}	S29			1.9V DC	29		240.0	560.0	880.0	mV
86		Output voltage Low 1	V_{EQL1}	S29			–1.9V DC	↓		–1410.0	–1130.0	–890.0	mV
87		Output voltage High 2	V_{EQH2}	S29			1.9V DC	30		590.0	840.0	1090.0	mV
88		Output voltage Low 2	V_{EQL2}	S29			–1.9V DC	↓		–1210.0	–880.0	–590.0	mV
89	AGC	Voltage gain 1	V_{AGC1}	S2, S3, S4, S5			100kHz 40mVp-p	29		19.0	22.0	25.0	dB
90		Voltage gain 2	V_{AGC2}	S2, S3, S4, S5, S17, S25		–1.0	↓			26.5	29.5	32.5	dB
91		Voltage gain 3	V_{AGC3}	S2, S3, S4, S5, S17, S25		–1.0	100kHz 100mVp-p			18.0	21.0	24.0	dB
92		Voltage gain 4	V_{AGC4}	S2, S3, S4, S5, S25		–1.0	↓	↓		11.5	14.5	17.5	dB

(Ta = 25°C, V_{CC} = 1.9V, GND = VC, V_{EE} = –1.9V)

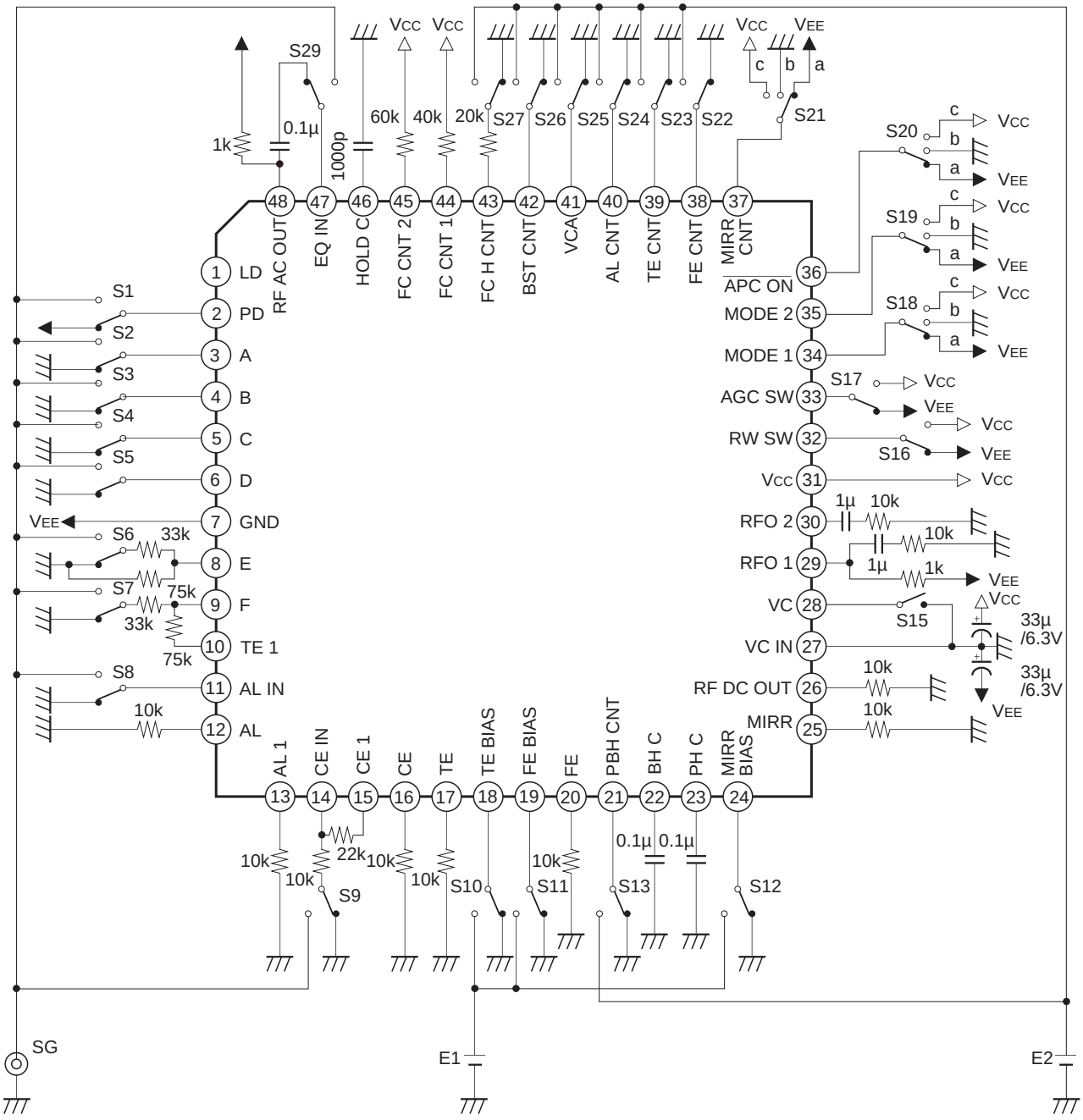
No.	Measurement item			SW conditions	Bias conditions (V)		Input	Output *IC pin No.		Ratings			
					E1	E2				Min.	Typ.	Max.	Unit
93	MIRR	Bias characteristics 1	B_{MIRR1}	S12, S21-b	1.0			25		1600.0	1710.0	—	mV
94		Bias characteristics 2	B_{MIRR2}	S12, S21-b	–1.0					—	–1585.0	–1475.0	mV
95		MIRR frequency response 1	F_{MIRR1}	S2, S3, S4, S5, S12, S21-b	0.1		30kHz 100mVp-p		See the figure below.	10.0	16.0	22.0	µs
96		MIRR frequency response 2	F_{MIRR2}	S2, S3, S4, S5, S12, S21-b	0.1					11.3	17.3	23.3	µs
97		MIRR frequency response 3	F_{MIRR3}	S2, S3, S4, S5, S12, S21-b	0.1					10.6	16.6	22.6	µs
98		MIRR frequency response 4	F_{MIRR4}	S2, S3, S4, S5, S12, S21-b	0.1					10.7	16.7	22.7	µs

MIRR frequency response measurement (T475 to T478)



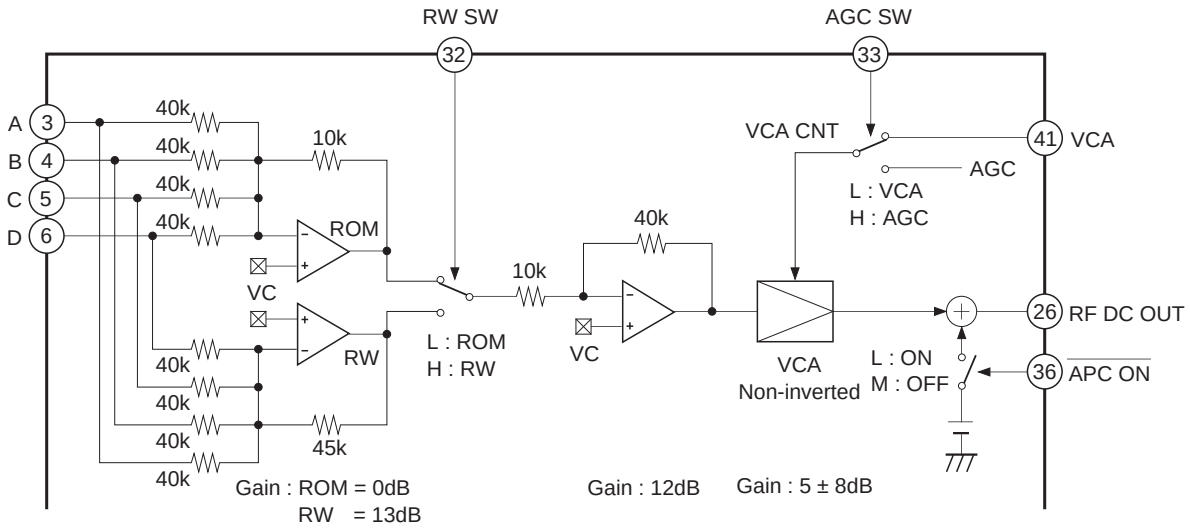
* T475 measurement value + T476 measurement value = 33.3µs.
* T477 measurement value + T478 measurement value = 33.3µs.

Electrical Characteristics Measurement Circuit



Description of Functions

RF DC



The RF DC block processes the RF DC signal that is used for the MIRR, FOK and DEFECT signals.
This block supports CD-ROM/RW, and the gain can be switched by Pin 32 (RW SW).
The gain during RW is 13dB higher than that during ROM.
ROM is selected when Pin 32 is Low, and RW when High.
This block has a VCA, and the total gain can be adjusted by Pin 41 (VCA).
The VCA has the same characteristics (control voltage – gain) as the RF AC block.

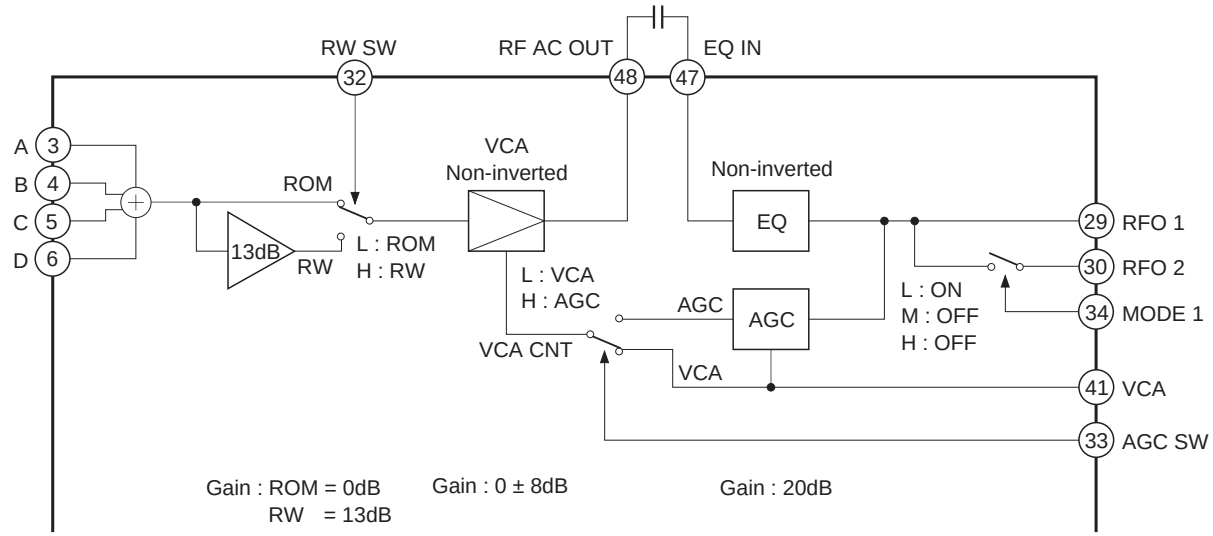
The total gain is ROM: 17 ± 8dB
RW: 30 ± 8dB

This block has a function for shifting the output DC voltage, and this function is switched by Pin 36 ($\overline{\text{APC ON}}$).
The DC voltage is shifted when Pin 36 is Low, and not shifted when Pin 36 is Medium.
When the DC voltage is shifted, the Pin 26 DC voltage equal to (Vcc-GND)/6 is shifted to the GND side.

The Pin 26 gain is as follows.

$$\text{RF DC OUT} = G_{\text{RF DC}} \cdot (A + B + C + D)$$

RF AC



The RF AC block processes the RF AC signal.
This block supports CD-ROM/RW, and the gain can be switched by Pin 32 (RW SW).
The gain during RW is 13dB higher than that during ROM.
ROM is selected when Pin 32 is Low, and RW when High.
This block has a VCA, and the total gain can be adjusted by the Pin 41 (VCA) voltage.
The VCA has the same characteristics (control voltage – gain) as the RF DC block.

The total gain is ROM: 20 ± 8dB
RW: 33 ± 8dB

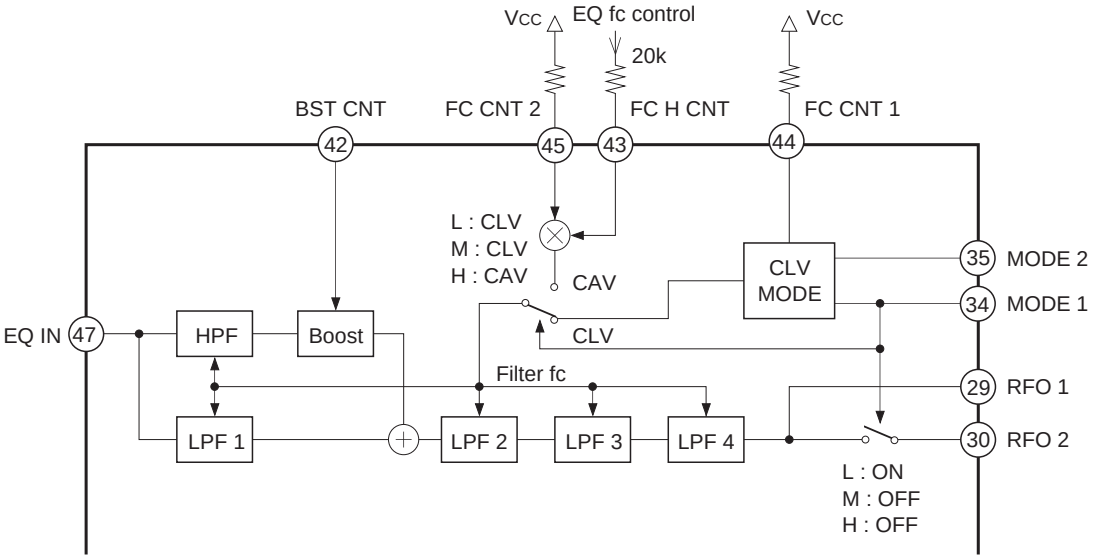
The capacitor values connected between this IC and the DSP can be switched , by using the Pin 30 (RFO 2) output.

The Pin 29 and 30 gains are as follows.

RFO 1 = $G_{RF\ AC} \cdot (A + B + C + D)$

RFO 2 = $G_{RF\ AC} \cdot (A + B + C + D)$

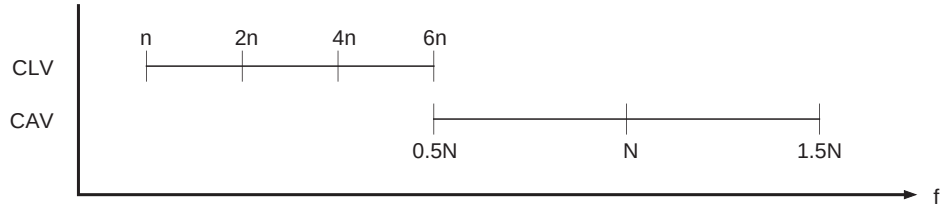
EQ



The EQ block is built into the RF AC system.
The cut-off frequencies of each filter are linked.
The cut-off frequencies are set by the external resistors connected to Pins 44 (FC CNT 1) and 45 (FC CNT 2), the Pin 43 (FC H CNT) voltage, and Pins 34 (MODE 1) and 35 (MODE 2).
The cut-off frequencies are set according to the following two systems.

CLV mode: When Pin 34 is Low, n, 2n, 4n and 6n are set by Pins 34 and 35 based on the cut-off frequency (fc = n) set by the external resistor connected to Pin 44.

CAV mode: When Pin 43 is VC, 0.5N to 1.5N is set by the Pin 43 voltage based on the cut-off frequency (fc = N) set by the external resistor connected to Pin 45.



The boost amount is set by the Pin 42 (BST CNT) voltage.

The transmittance for each filter of the EQ block is as follows.

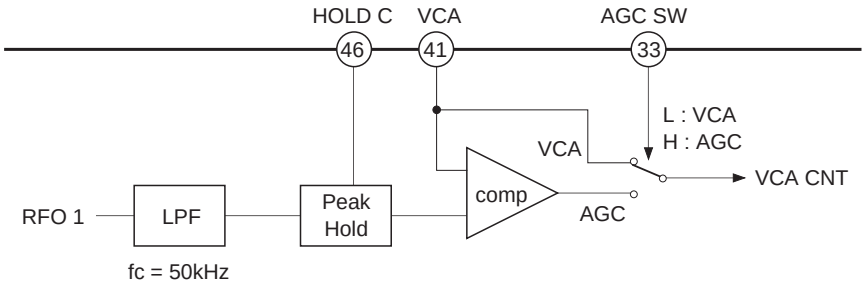
HPF: $(KS^2) / (S^2 + 3.22597S + 2.94933)$
LPF1: $(2.94933) / (S^2 + 3.22597S + 2.94933)$
LPF2: $(3.32507) / (S^2 + 2.75939S + 3.32507)$
LPF3: $(4.20534) / (S^2 + 1.82061S + 4.20534)$
LPF4: $(1.68536) / (S + 1.68536)$

R_{MIN} is 40kΩ for the external resistor connected to Pin 44, and 30kΩ for the external resistor connected to Pin 45.

Pin Settings and Cut-off Frequency

MODE 1 (Pin 34)	MODE 2 (Pin 35)	FC H CNT (Pin 43)	fc	mode
L	X	—	n	CLV
M	L		2n	
	M		4n	
	H		6n	
H	X	VC – 1V to VC to VC + 1V	0.5N to N to 1.5N	CAV

AGC



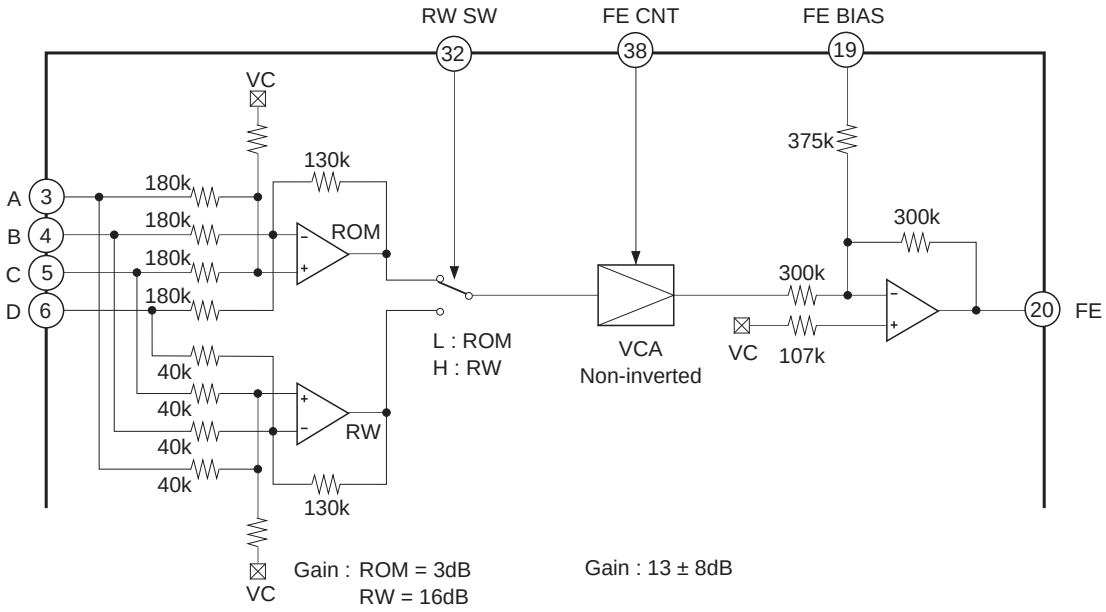
The AGC block sets the RF AC and RF DC gains.
AGC/VCA can be switched by Pin 33 (AGC SW).
VCA is selected when Pin 33 is Low, and AGC when High.

The following can be performed by the Pin 41 (VCA) voltage.

VCA: Gain adjustment
AGC: Output amplitude setting

Pin 46 (HOLD C) is used to connect a capacitor for setting the AGC time constant.

FE



The FE block processes the focus error signal.
This block supports CD-ROM/RW, and the gain can be switched by Pin 32 (RW SW).
The gain during RW is 13dB higher than that during ROM.
ROM is selected when Pin 32 is Low, and RW when High.
This block has a VCA, and the total gain can be adjusted by the Pin 38 (FE CNT) voltage.

The total gain is as follows.

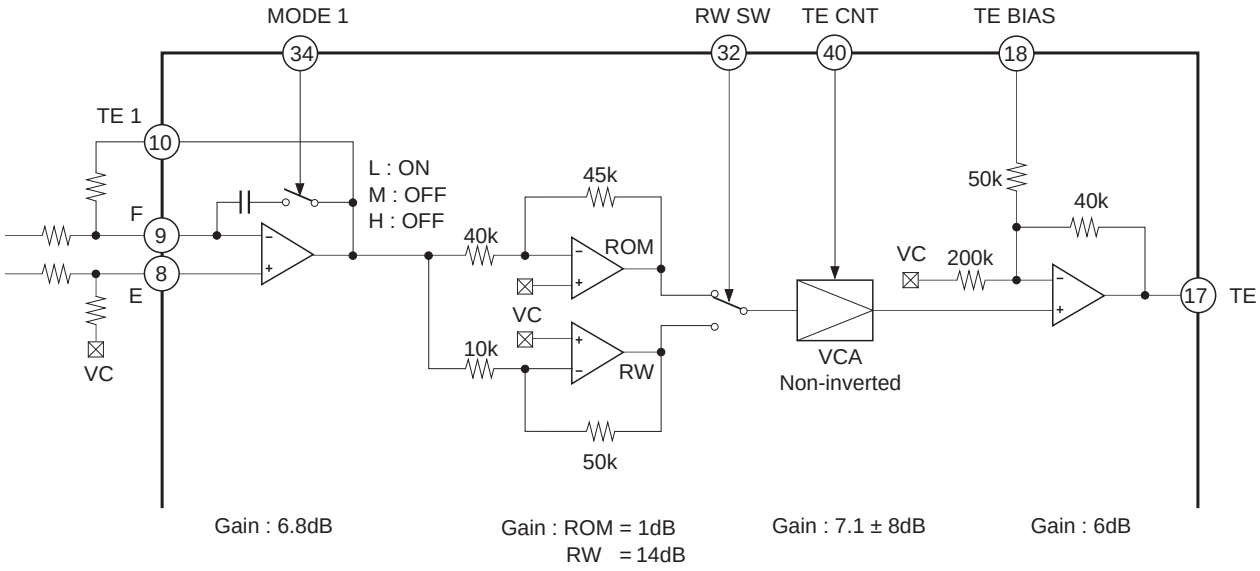
ROM: 16 ± 8dB
RW: 29 ± 8dB

The output DC voltage level can be adjusted by the Pin 19 (FE BIAS) voltage.

The Pin 20 gain is as follows.

$FE = G_{FE} \cdot (B + D - A - C)$

TE



The TE block processes the tracking error signal.
This block supports CD-ROM/RW, and the gain can be switched by Pin 32 (RW SW).
The gain during RW is 13dB higher than that during ROM.
ROM is selected when Pin 32 is Low, and RW when High.
This block has a VCA, and the total gain can be adjusted by the Pin 39 (TE CNT) voltage.

The total gain is as follows.

ROM: 20.9 ± 8dB

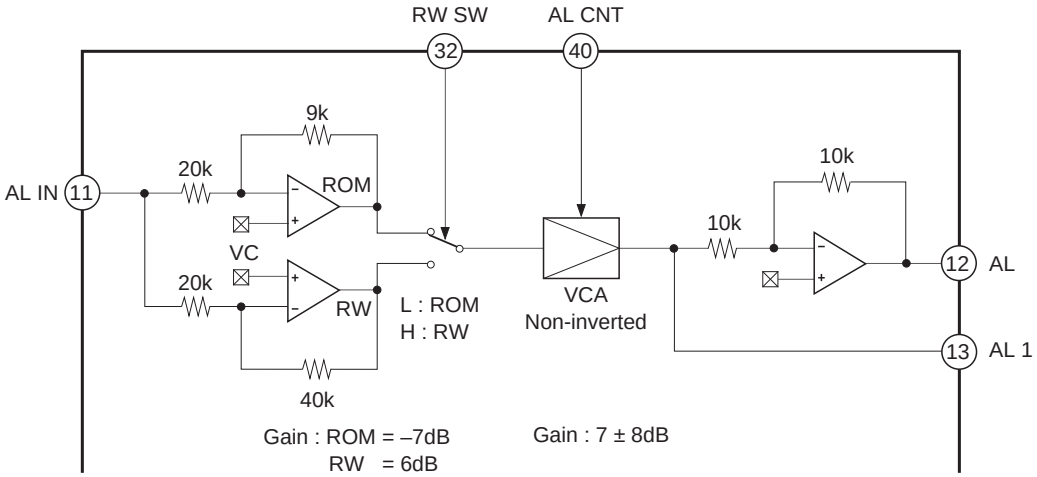
RW: 33.9 ± 8dB

The output DC voltage level can be adjusted by the Pin 18 (TE BIAS) voltage.
The LPF cut-off frequency can be switched by the Pin 34 (MODE 1) voltage.
fc = 20kHz when Pin 34 is Low, and fc = 250kHz when Medium or High.

The Pin 17 gain is as follows.

$TE = G_{TE} \cdot (F - E)$

AL



The AL block processes the alignment signal.
This block supports CD-ROM/RW, and the gain can be switched by Pin 32 (RW SW).
The gain during RW is 13dB higher than that during ROM.
ROM is selected when Pin 32 is Low, and RW when High.
This block has a VCA, and the total gain can be adjusted by the Pin 40 (AL CNT) voltage.

The total gain is as follows.

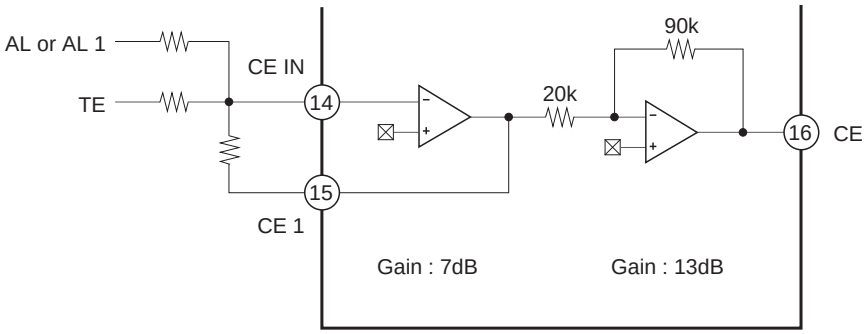
ROM: 0 ± 8dB
RW: 13 ± 8dB

Pin 12 (AL) is the non-inverted output, and Pin 13 (AL 1) is the inverted output with respect to the input.

The Pin 12 and 13 gains are as follows.

$AL = G_{AL} \cdot AL\ IN$
$AL\ 1 = -G_{AL} \cdot AL\ IN$

CE



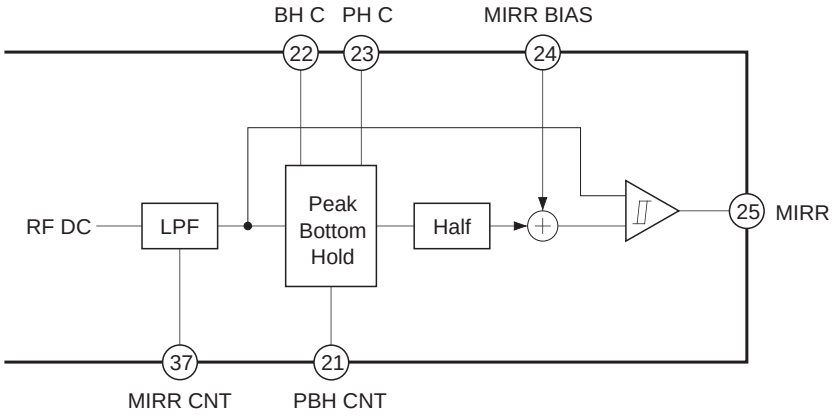
The CE block processes the center error signal.
The AL and TE signals are arithmetically amplified and output as the center error signal.
The total gain is 20dB.

The Pin 16 (CE) gain is as follows.

$CE = G_{CE} \cdot (AL + \alpha TE)$: straight optical path laser coupler

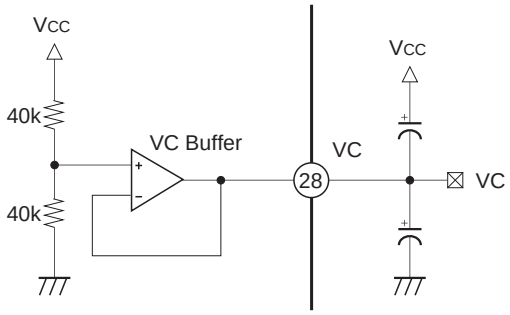
$CE = G_{CE} \cdot (AL\ 1 + \alpha TE)$: folded optical path laser coupler

MIRR



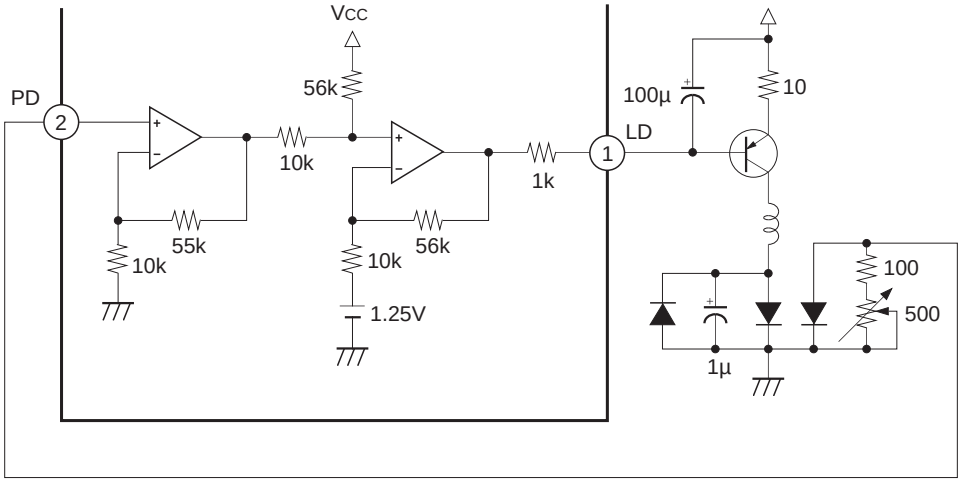
The MIRR block processes the MIRR signal.
The MIRR signal is generated from the RF DC signal.
The initial stage LPF is a third-order LPF, and separates the envelope and EFM signals.
The LPF cut-off frequency can be switched by the Pin 37 (MIRR CNT) voltage.
Pins 22 (BH C) and 23 (PH C) are used to connect capacitors for peak and bottom hold of the separated envelope signal.
The peak and bottom hold time constants are set by the Pin 21 (PBH CNT) voltage.
The DC voltage level of the mirror circuit can be adjusted by the Pin 24 (MIRR BIAS) voltage.

Center Voltage Generation Circuit



The center voltage VC = (Vcc + GND)/2 is output from Pin 28 (VC).
The maximum output current is about ±3mA.

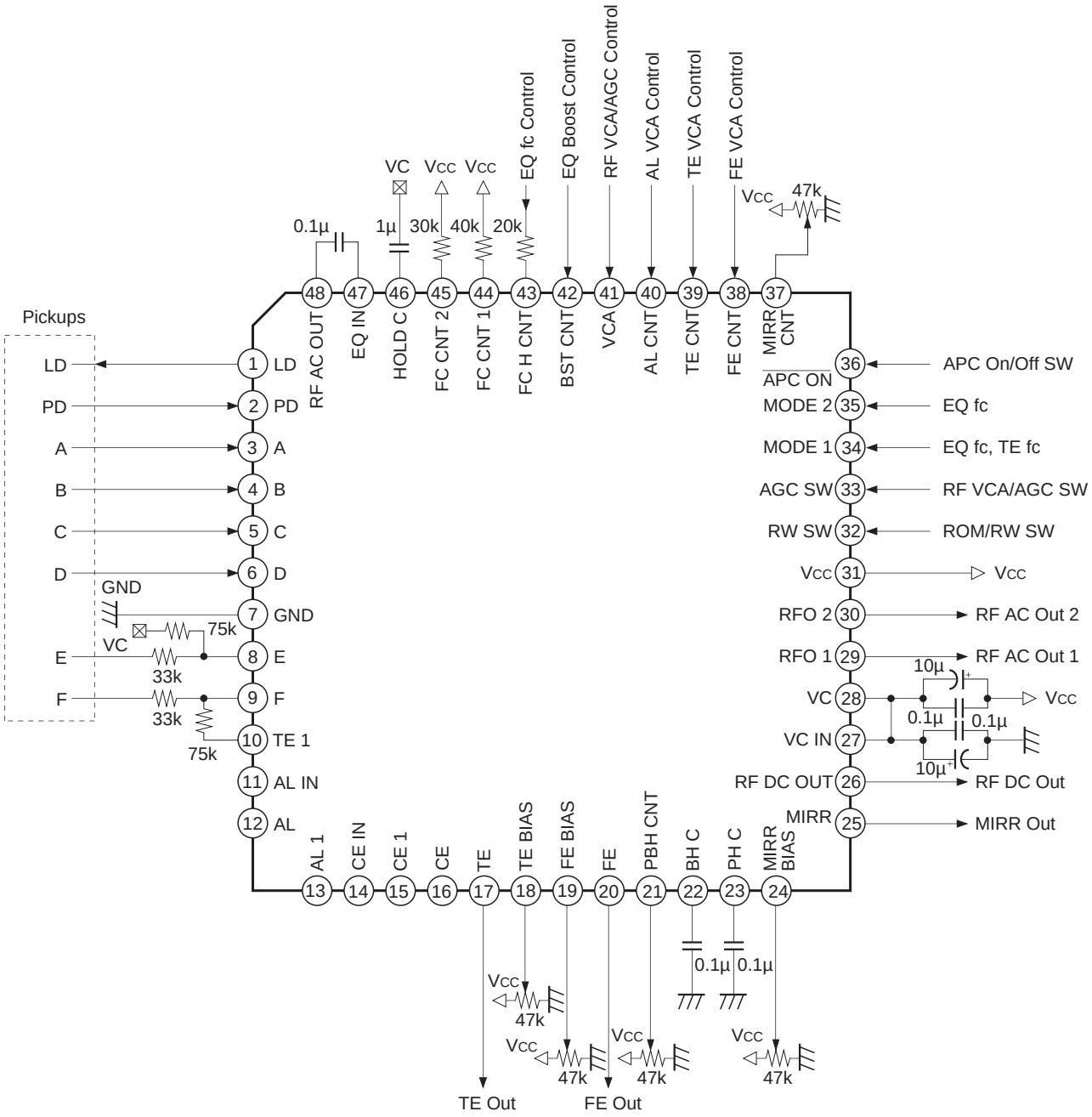
APC



When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics.
The APC circuit uses a monitor photodiode to control the laser diode current in order to maintain the optical power output at a constant level.

Application Circuit

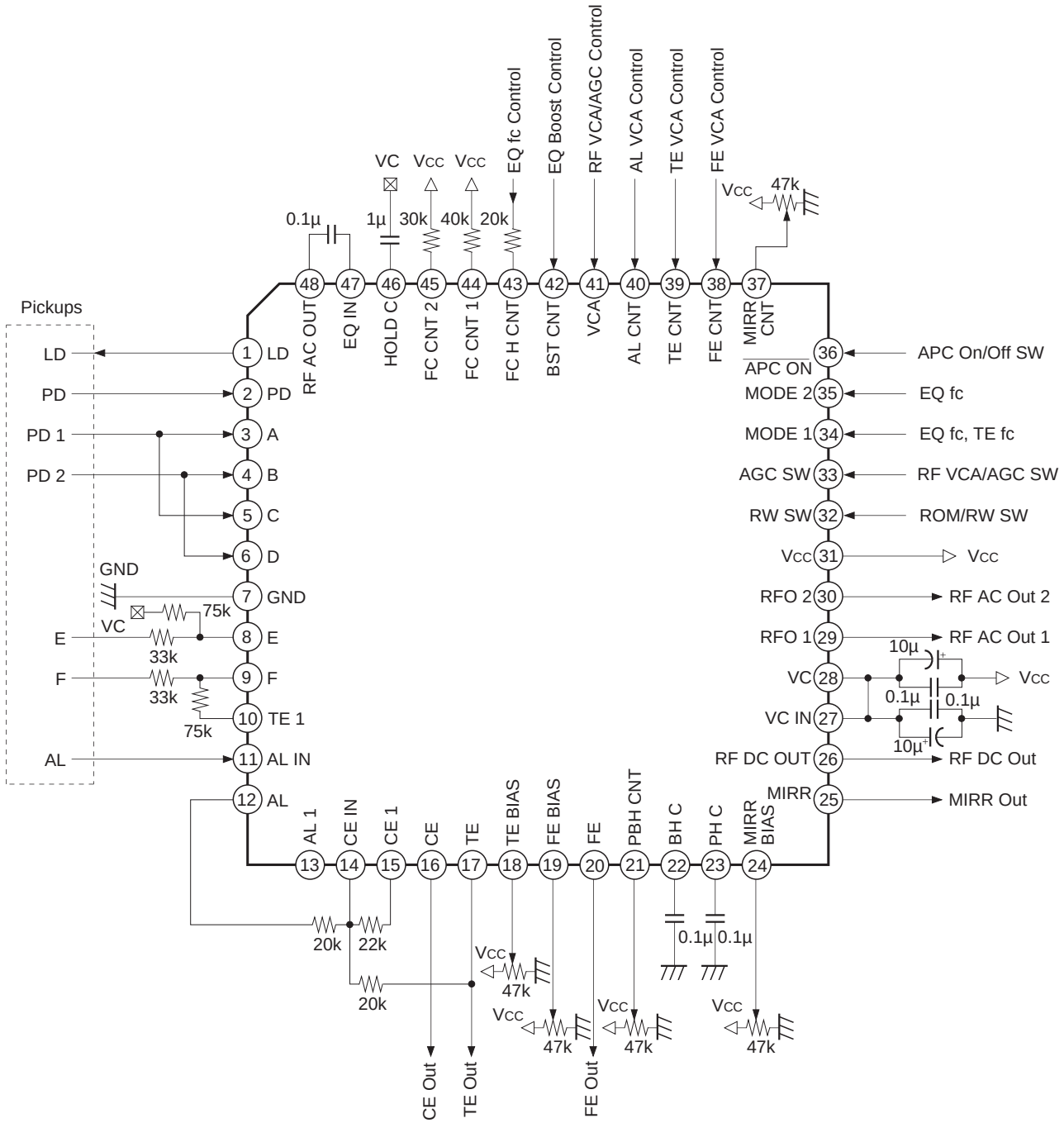
3 spots



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit

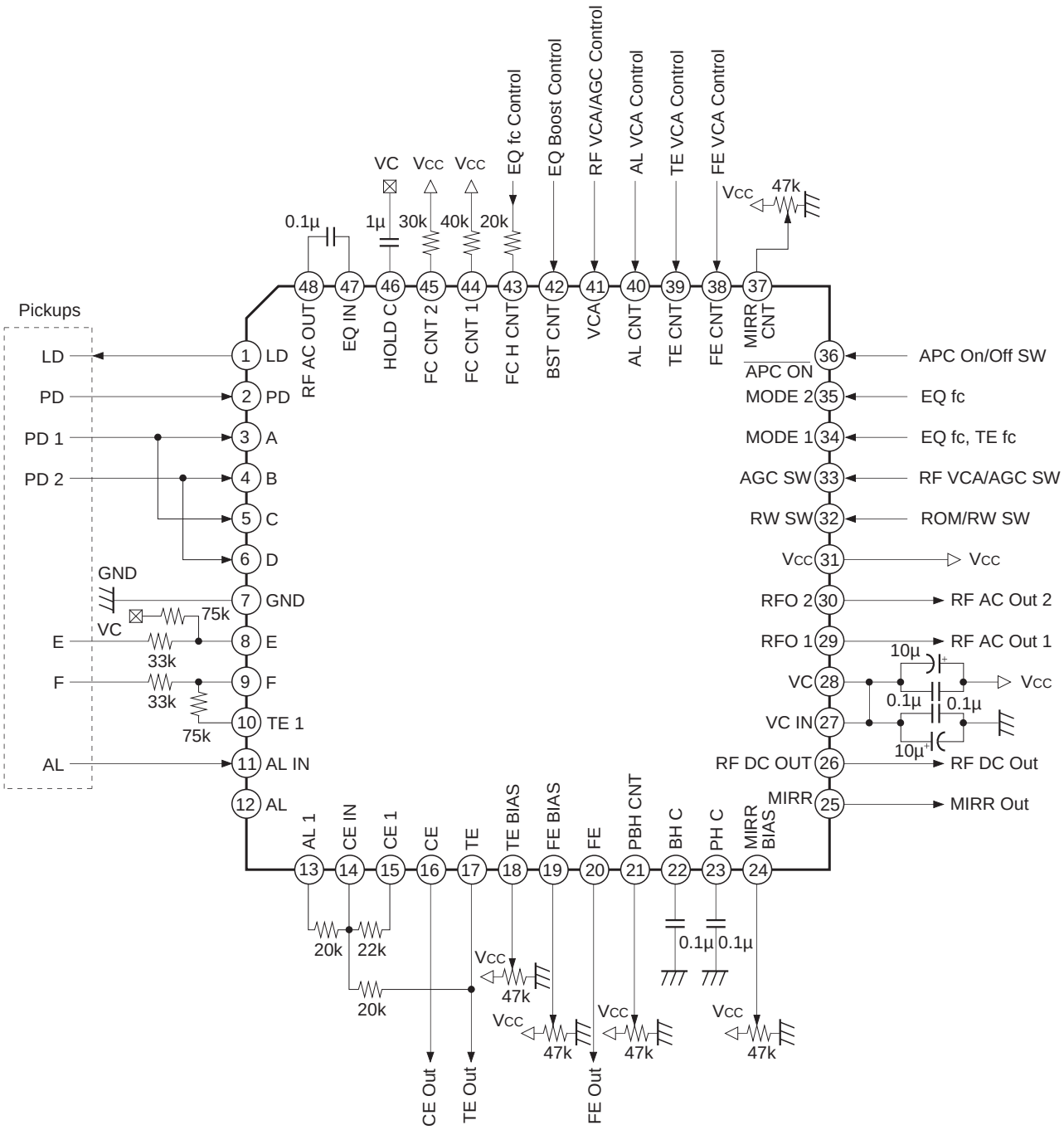
Laser coupler (straight optical path type)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit

Laser coupler (folded optical path type)

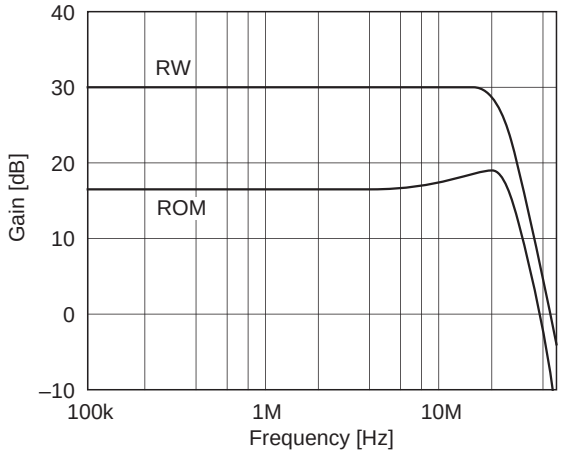


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

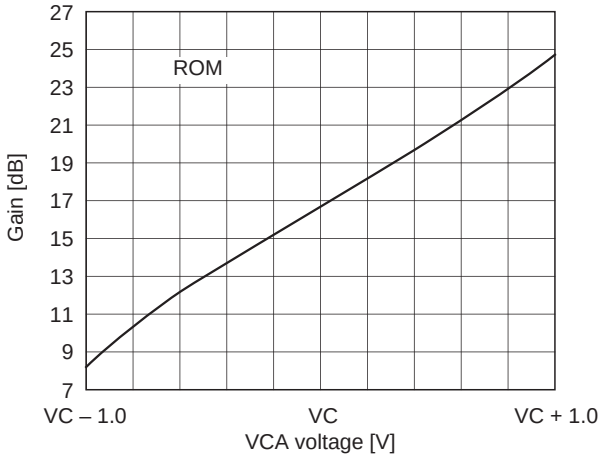
Example of Representative Characteristics (VC voltage reference)

RF DC Characteristics Graphs (Pin 26)

Frequency response

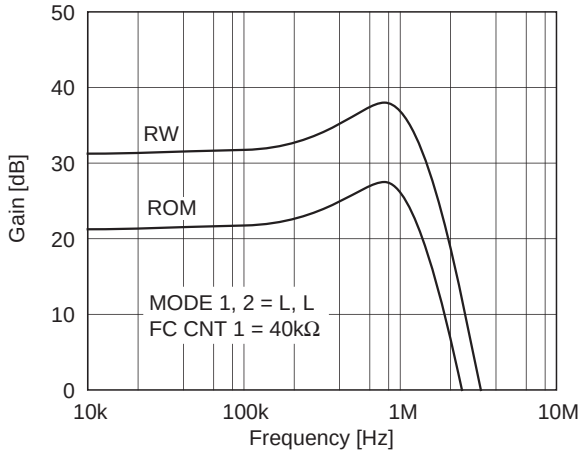


VCA characteristics

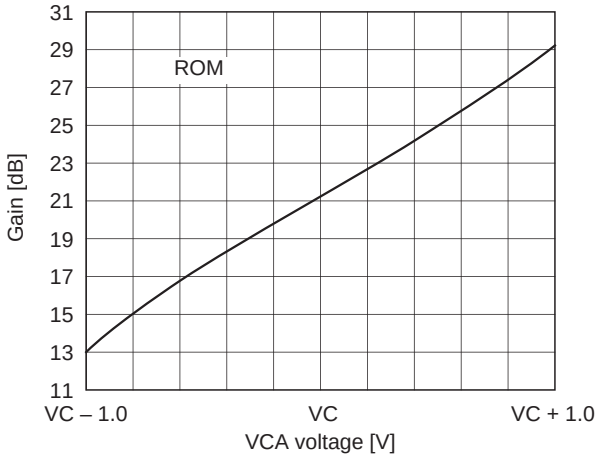


RF AC Characteristics Graphs (Pin 29)

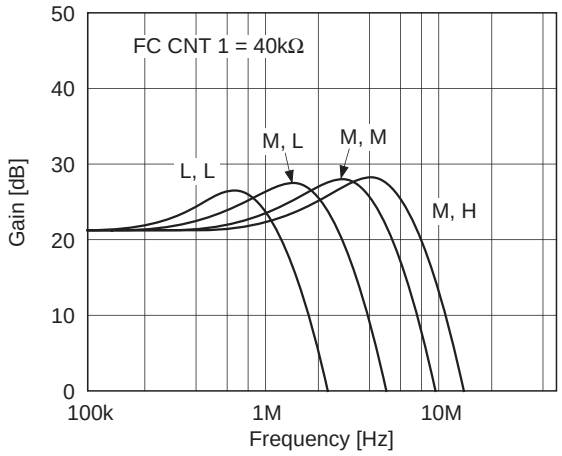
Frequency response



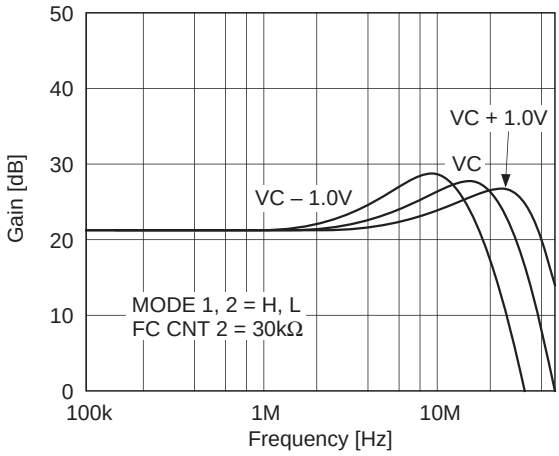
VCA characteristics



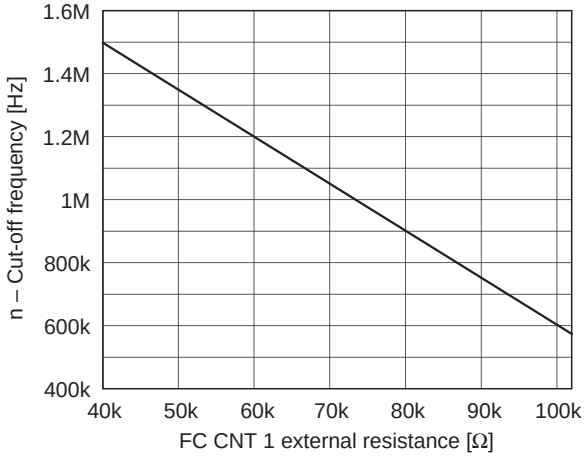
EQ characteristics (CLV)



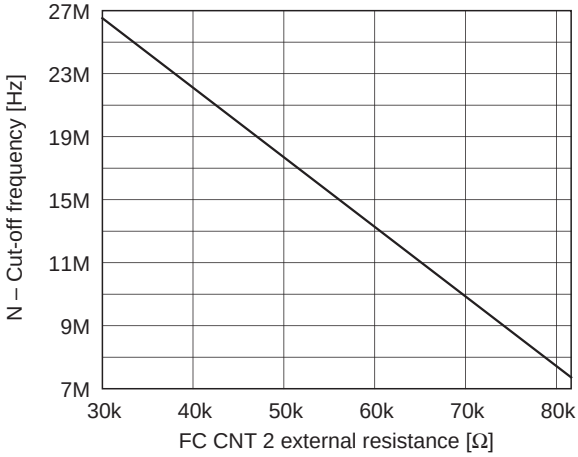
EQ characteristics (CAV)



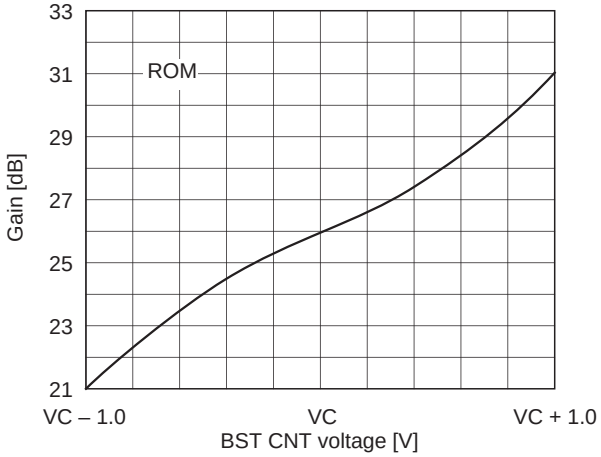
Cut-off frequency response 1



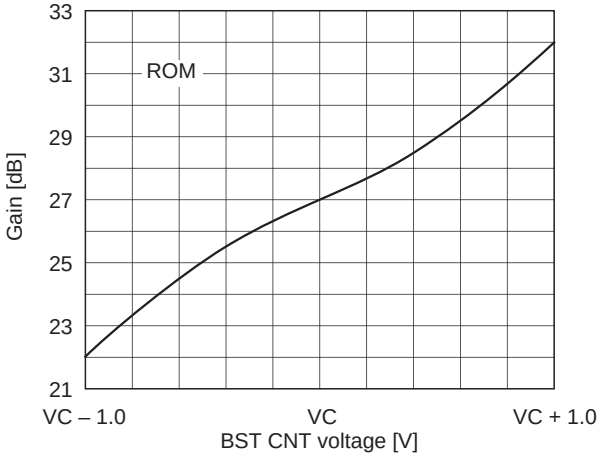
Cut-off frequency response 2



Boost characteristics (CLV)

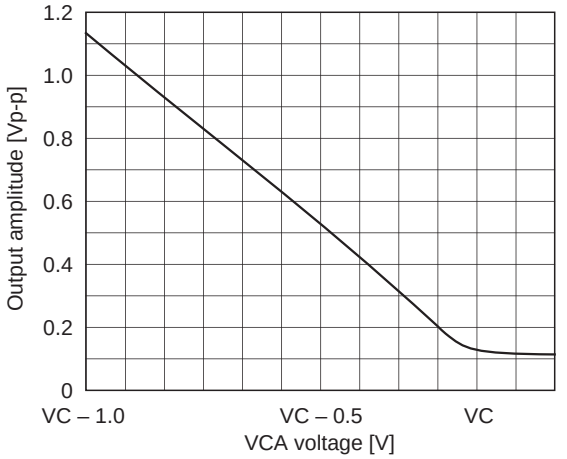


Boost characteristics (CAV)



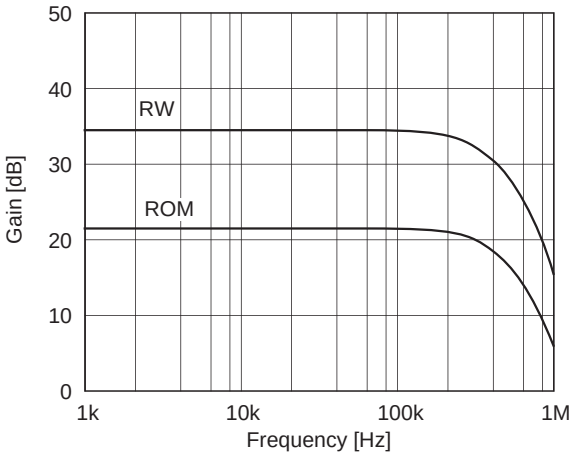
AGC Characteristics Graph (Pin 29)

Output amplitude characteristics

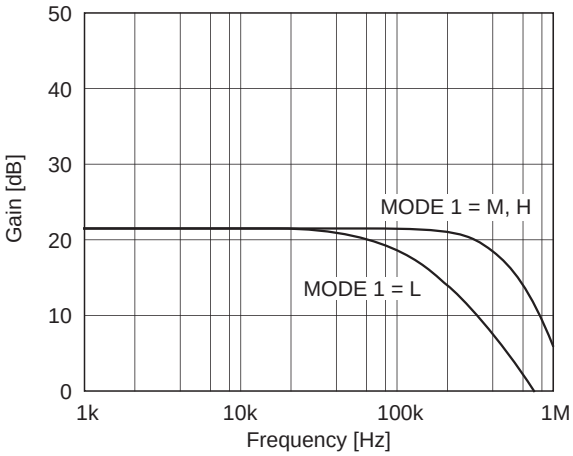


TE Characteristics Graphs (Pin 17)

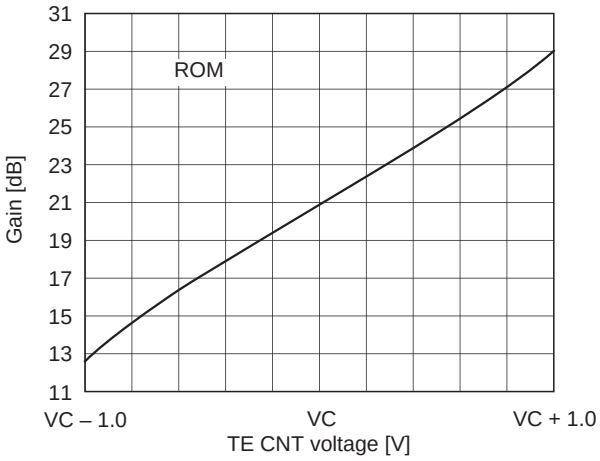
Frequency response 1



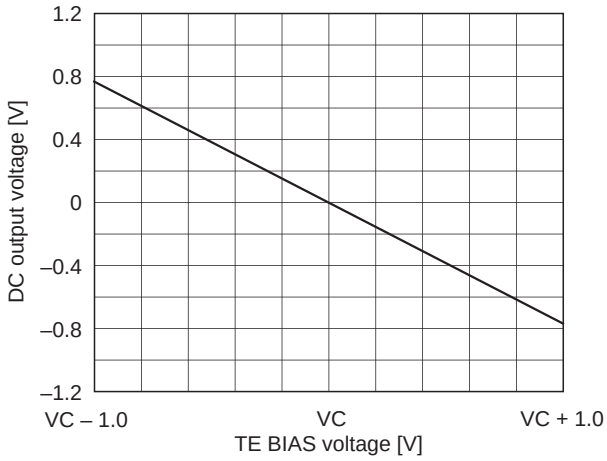
Frequency response 2



TE CNT characteristics



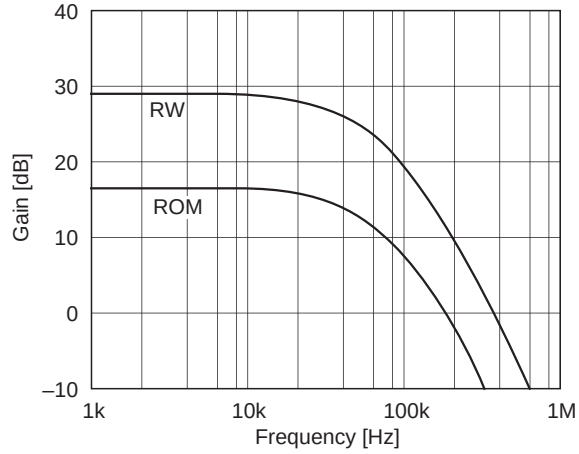
TE BIAS characteristics



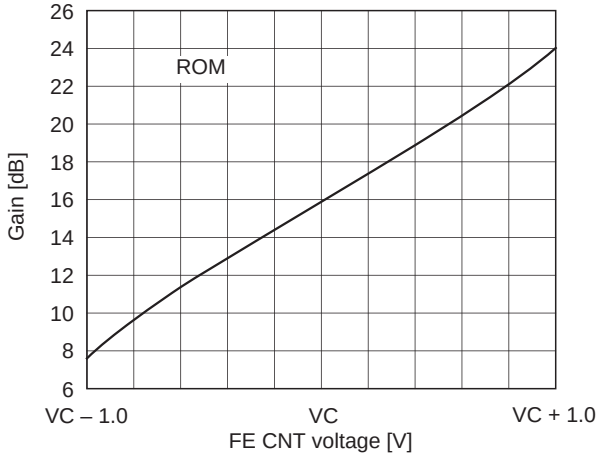
* TE BIAS voltage; DC output voltage is 0V at VC.

FE Characteristics Graphs (Pin 20)

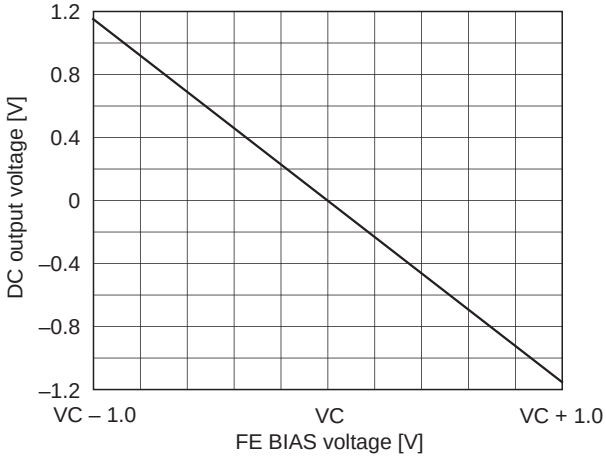
Frequency response



FE CNT characteristics



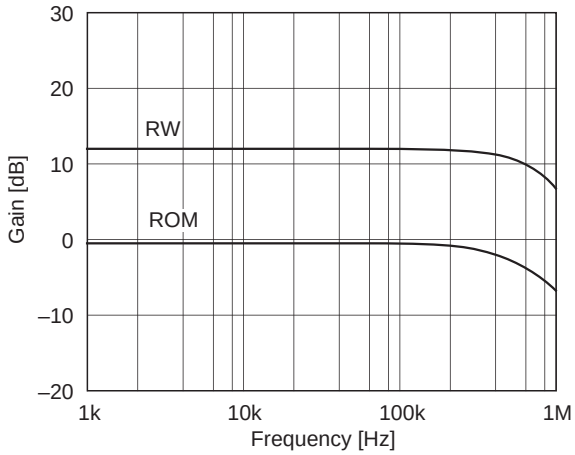
FE BIAS characteristics



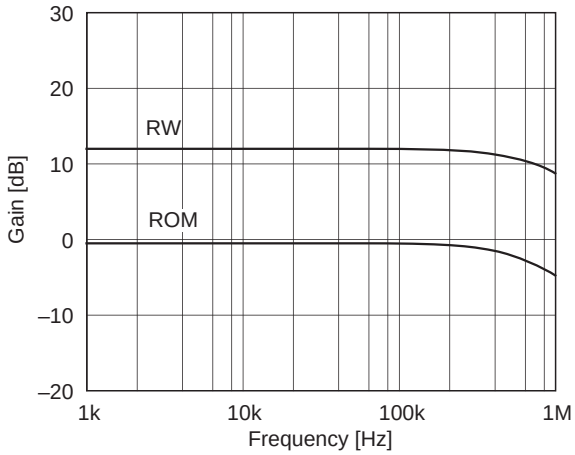
* FE BIAS voltage; DC output voltage is 0V at VC.

AL Characteristics Graphs (Pins 12 and 13)

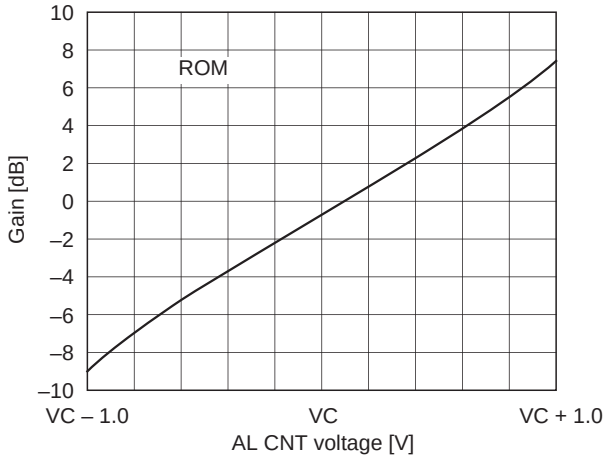
Frequency response (AL)



Frequency response (AL 1)

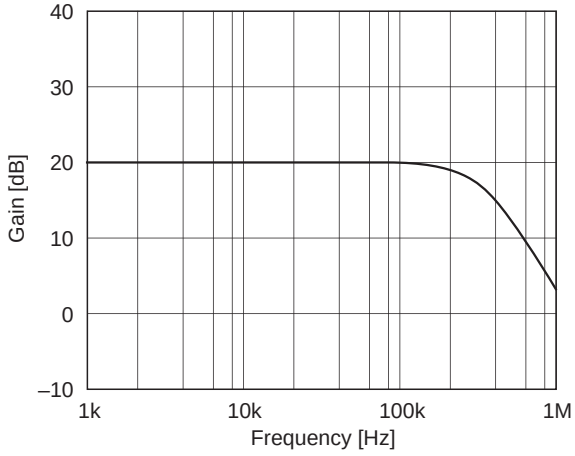


AL CNT characteristics



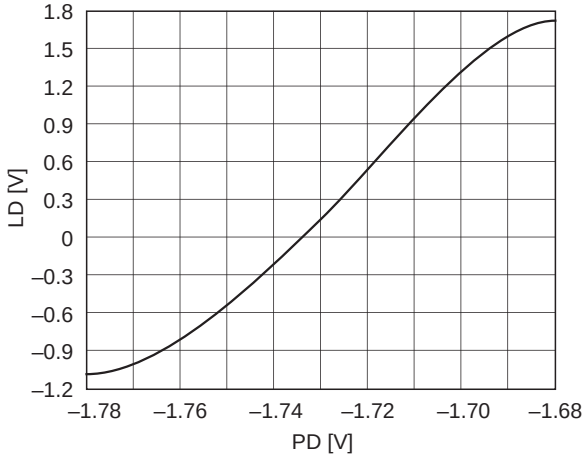
CE Characteristics Graph (Pin 16)

Frequency response



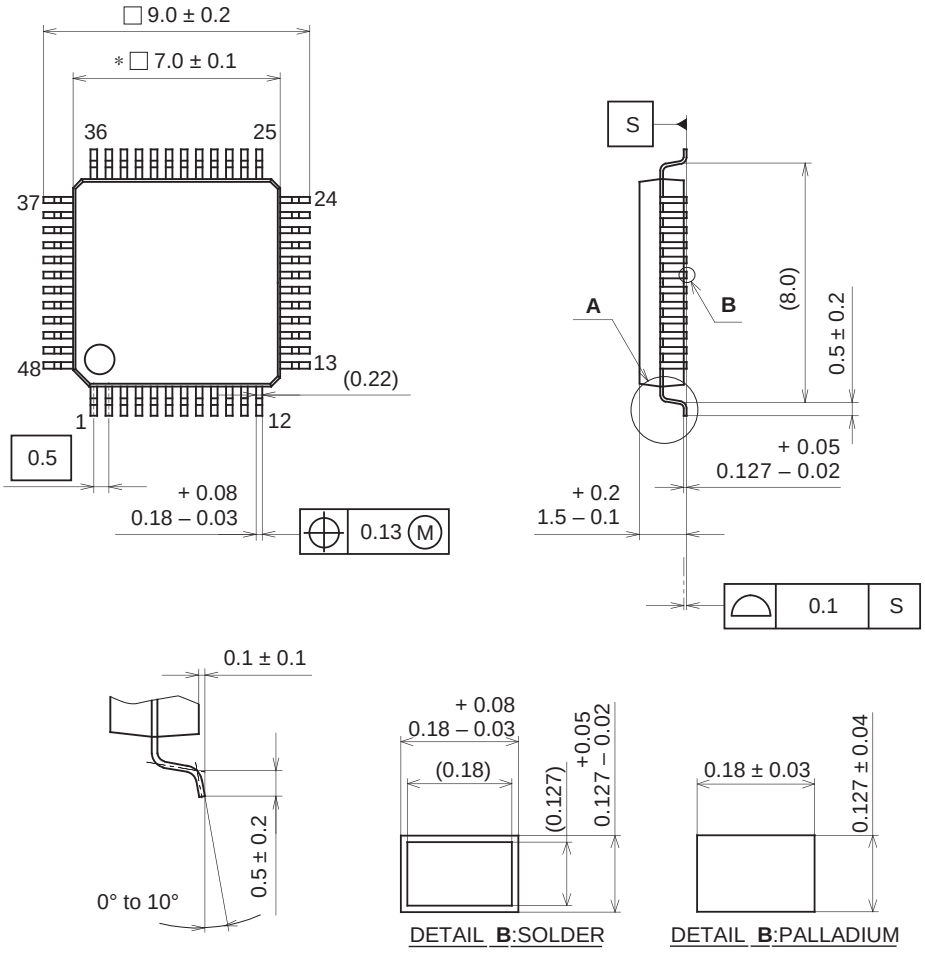
APC Characteristics Graph (Pin 1)

LD voltage vs. PD voltage



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g