



April 2000

**QFET™**

# FQD5N20 / FQU5N20

## 200V N-Channel MOSFET

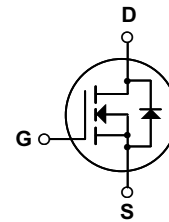
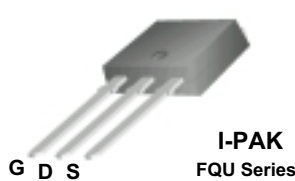
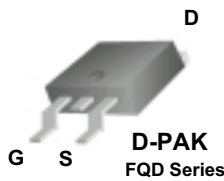
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, DC-AC converters for uninterrupted power supply, motor control.

### Features

- 3.8A, 200V,  $R_{DS(on)} = 1.2\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 6.0 nC)
- Low Crss ( typical 6.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQD5N20 / FQU5N20	Units
V <sub>DSS</sub>	Drain-Source Voltage	200	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	3.8	A
	- Continuous (T <sub>C</sub> = 100°C)	2.4	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	15.2	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	60	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	3.8	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *	2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)	37	W
	- Derate above 25°C	0.29	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	3.4	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	200	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.2	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.9 A	--	0.96	1.2	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1.9 A (Note 4)	--	2.85	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	210	270	pF
C <sub>oss</sub>	Output Capacitance		--	40	50	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	6	8	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 4.5 A, R <sub>G</sub> = 25 Ω  (Note 4, 5)	--	7	25	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	9	30	ns
t <sub>f</sub>	Turn-Off Fall Time		--	25	60	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 4.5 A, V <sub>GS</sub> = 10 V  (Note 4, 5)	--	6.0	7.5	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	2.2	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	3.8	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	15.2	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.8 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A, di <sub>F</sub> / dt = 100 A/μs (Note 4)	--	95	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.3	--	μC

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 6.3mH, I<sub>AS</sub> = 3.8A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 4.5A, di/dt ≤ 300A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

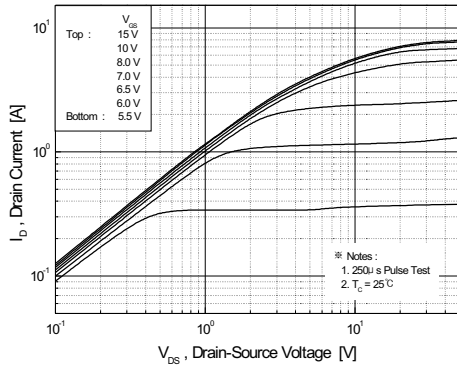


Figure 1. On-Region Characteristics

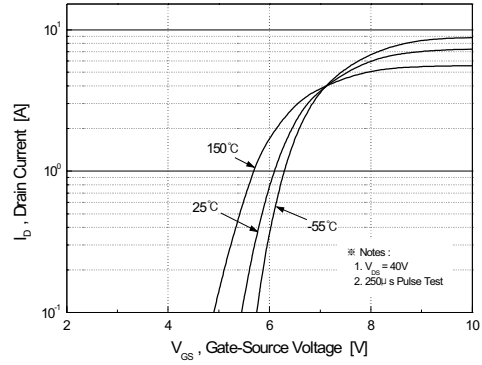


Figure 2. Transfer Characteristics

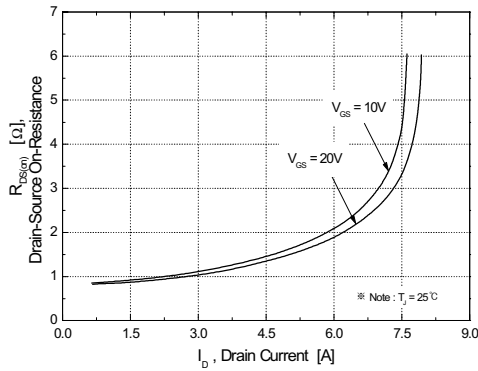


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

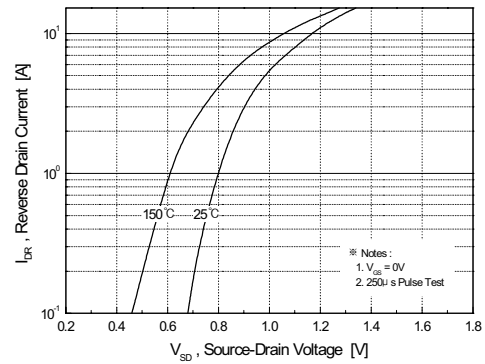


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

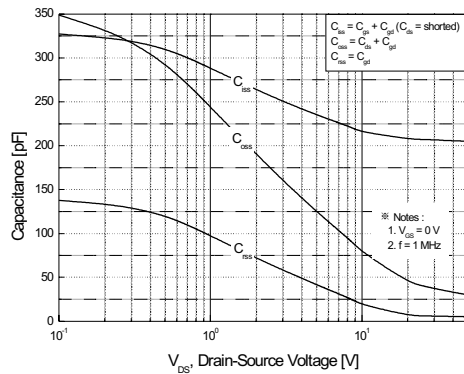


Figure 5. Capacitance Characteristics

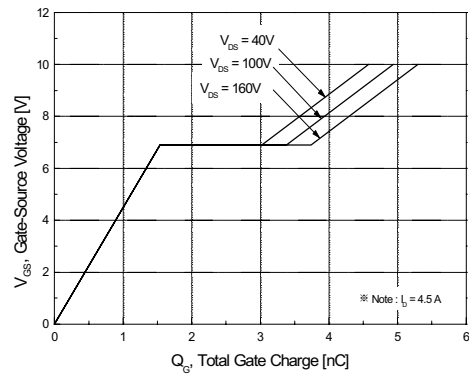
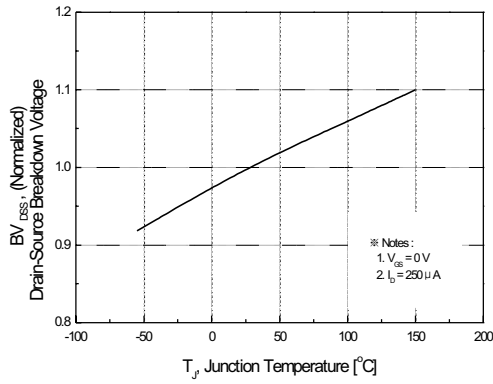
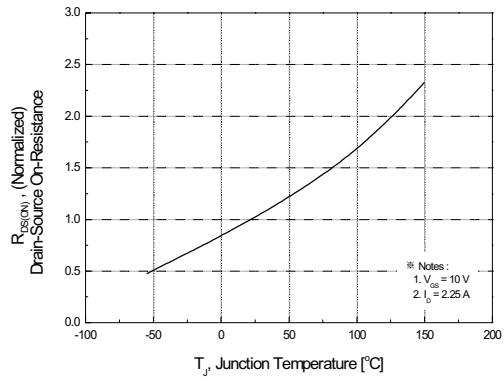


Figure 6. Gate Charge Characteristics

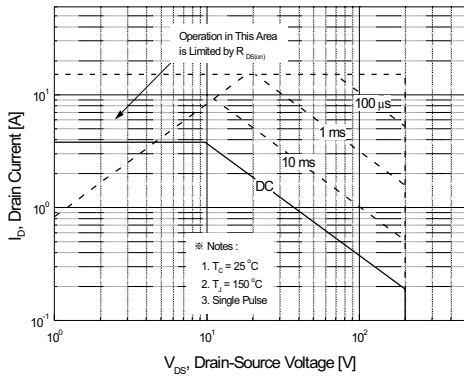
**Typical Characteristics** (Continued)



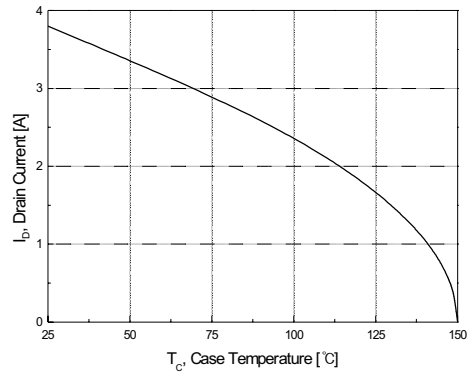
**Figure 7. Breakdown Voltage Variation vs. Temperature**



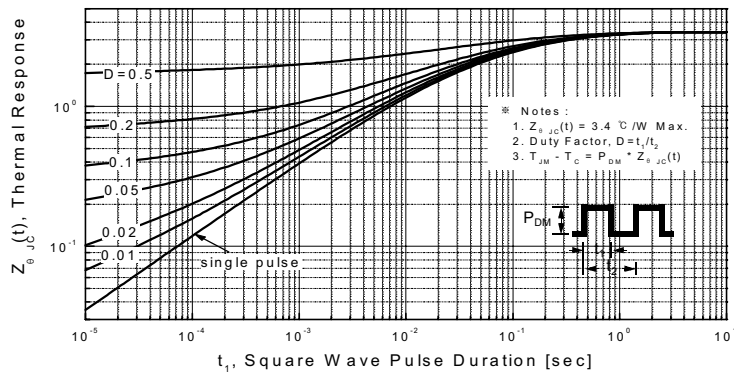
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

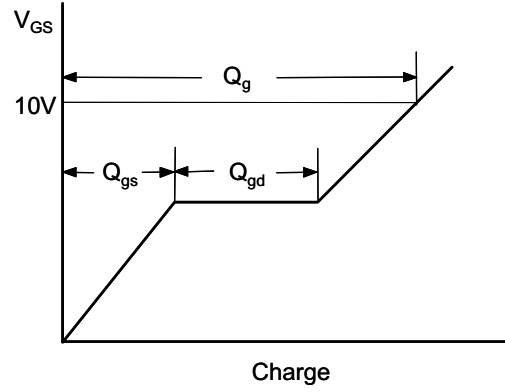


**Figure 10. Maximum Drain Current vs. Case Temperature**

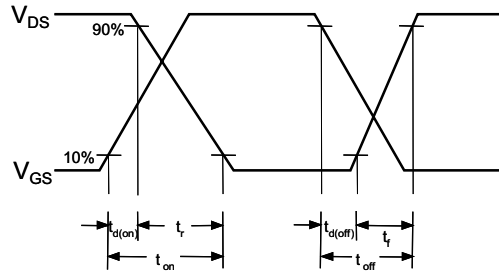
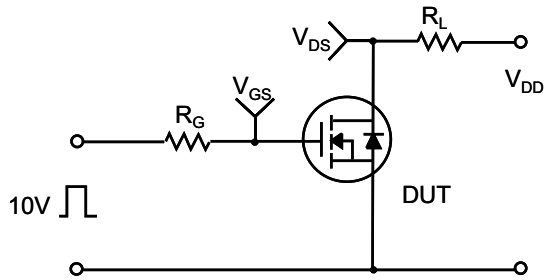


**Figure 11. Transient Thermal Response Curve**

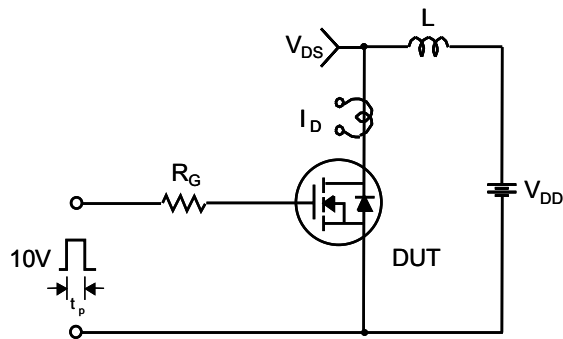
Gate Charge Test Circuit & Waveform



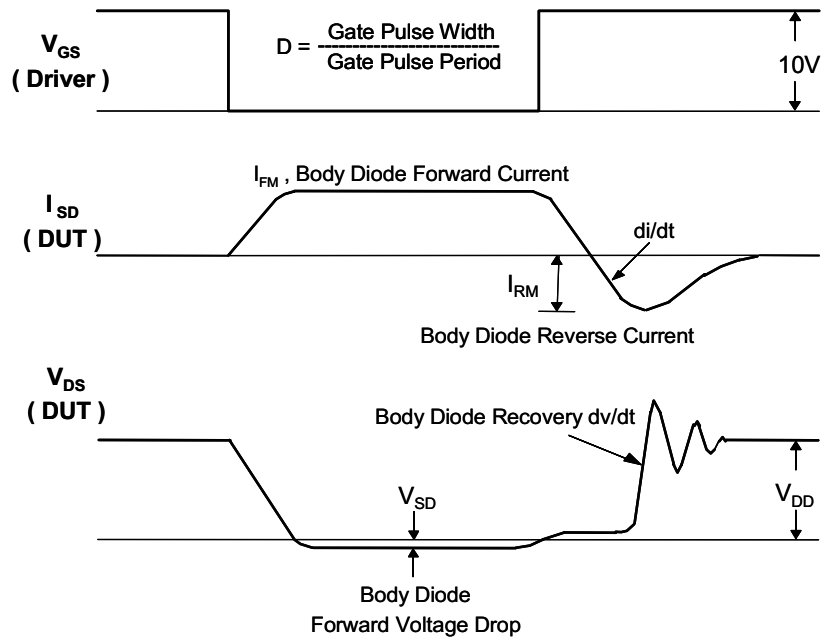
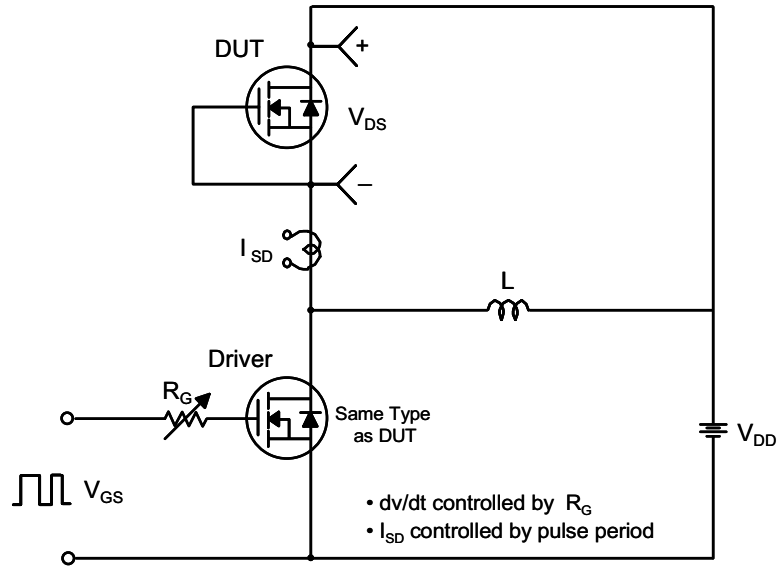
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

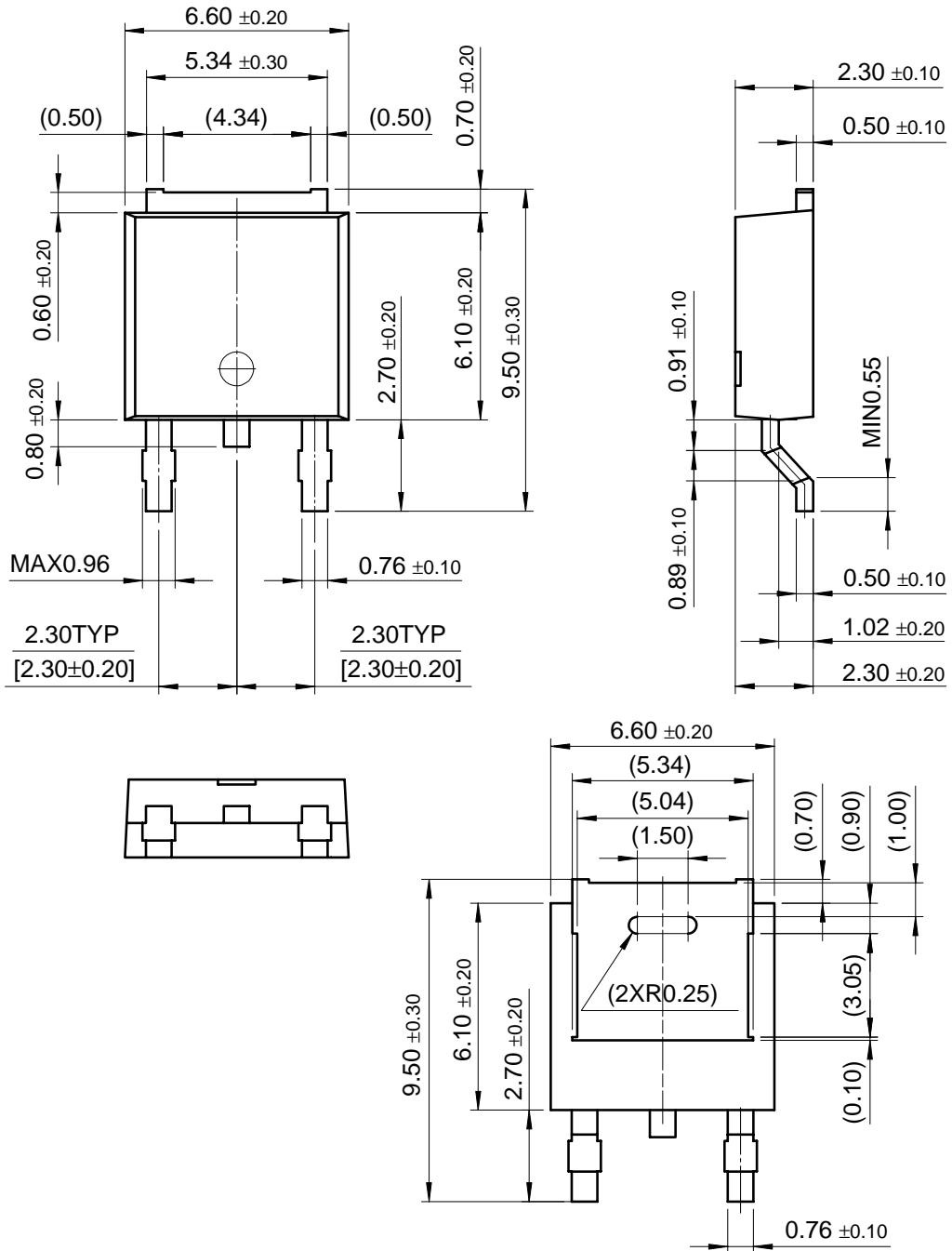


Peak Diode Recovery dv/dt Test Circuit & Waveforms



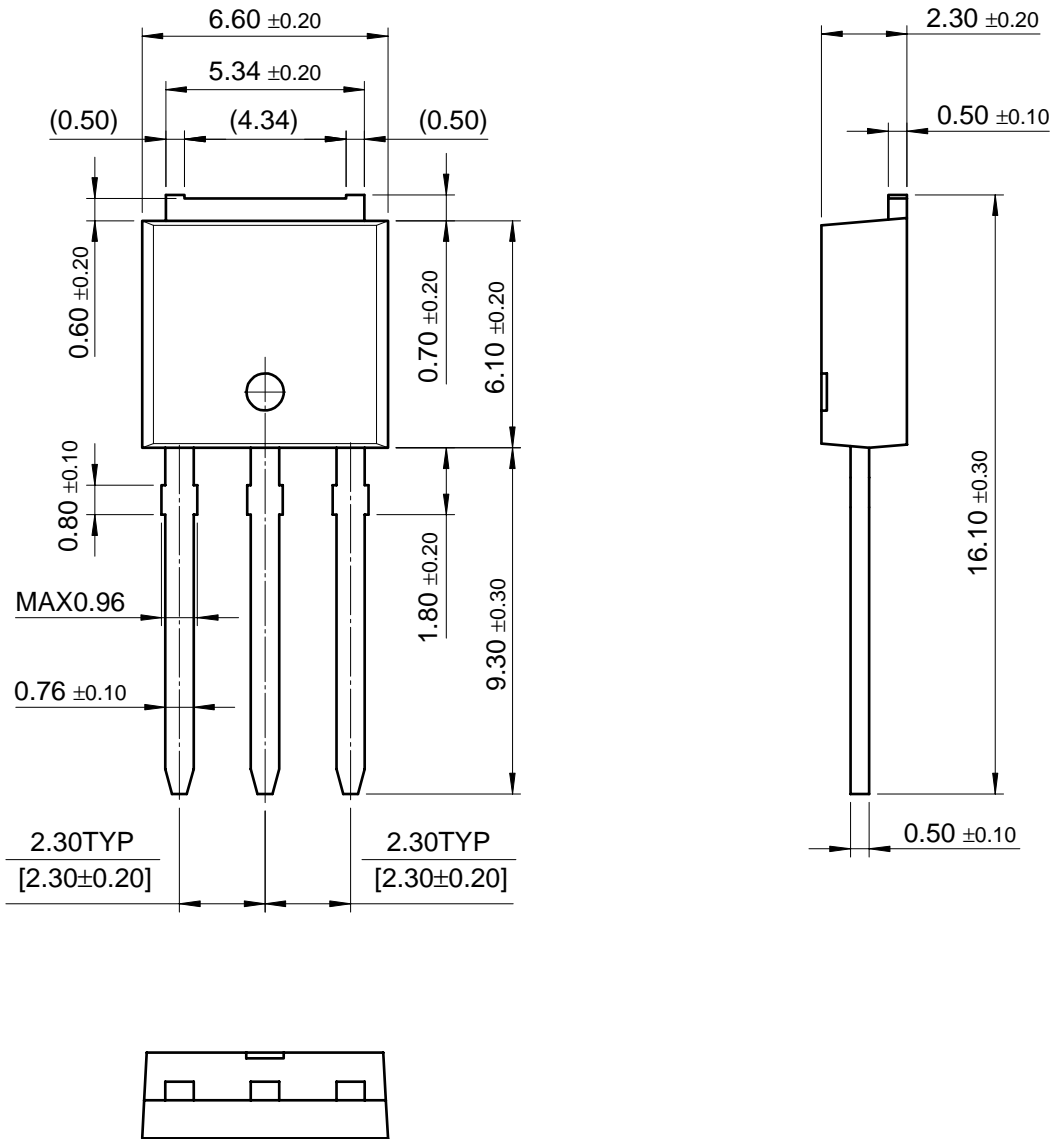
Package Dimensions

DPAK



Package Dimensions (Continued)

# IPAK



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