Data Sheet | January 1997 | File Number 2491.4

12 x 8 x 1 BiMOS-E Crosspoint Switch

The Intersil CD22M3493 is an array of 96 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range, V_{DD} to V_{SS}. Each of the 96 switches may be addressed via the ADDRESS input to the 7 to 96 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or logic zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD22M3493E	-40 to 85	40 Ld PDIP	E40.6
CD22M3493Q	-40 to 85	44 Ld PLCC	N44.65

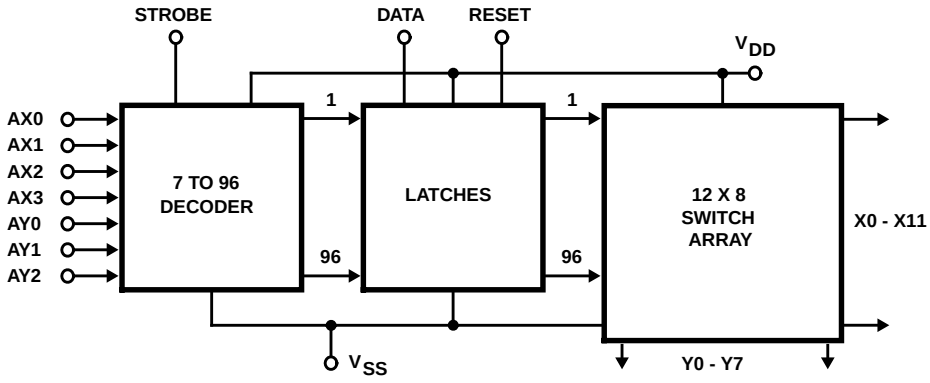
Features

- 96 Analog Switches
- Low R_{ON}
- Guaranteed R_{ON} Matching
- Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage . . . . . 4V to 16V
- Parallel Input Addressing
- High Latch Up Current . . . . . 50mA (Min)
- Very Low Crosstalk
- Pin and Functionally Compatible with the Following Types: SGS M3493, SGS M093, SSI 78A093A, and Mitel MT8812

Applications

- PBX Systems
- Instrumentation
- Analog and Digital Multiplexers
- Video Switching Networks

Block Diagram



Absolute Maximum Ratings

DC Supply Voltage (V_{DD}) (Referenced to VSS . . . . . -0.5V to 17V
Supply Voltage Range
For T_A = Full Package Temperature Range
V_{SS} = 0V, V_{DD} 4V to 16V
DC Input Diode Current, I_{IN}
For $V_I < V_{SS}$ -0.5V or $V_I > V_{DD}$ +0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For $V_O < V_{SS}$ -0.5V or $V_O > V_{DD}$ +0.5V . . . . . ±20mA
DC Transmission Gate Current . . . . . ±25mA
Power Dissipation Per Package (Po)
For T_A = -40°C to 85°C (PDIP) 500mW
For T_A = -40°C to 85°C (PLCC) 600mW

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
Plastic DIP Package	55
PLCC Package	43

Maximum Junction Temperature Plastic . . . . . .150°C
Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(PLCC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)
Package Type E and Q . . . . . -40°C to 85°C
DC Input or Output Voltage . . . . . Min = V_{SS} , Max = V_{DD}
Digital Input Voltage . . . . . Min = V_{SS} , Max = V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 85°C, V_{SS} = 0V, V_{DD} = 14V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	V_{DD} = 5V, Logic Inputs = V_{DD}	-	-	2	mA
		V_{DD} = 16V, Logic Inputs = V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}		2.4	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
Input Leakage Current, Digital	I_{IN}	Reset = Low (Note 2)	-	-	±10 (Note 3)	µA

Electrical Specifications

T_A = -40°C to 85°C, V_{SS} = 0V, V_{DD} = 14V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC CROSSPOINTS							
ON Resistance	R_{ON}	T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V	V_{DD} = 5V	-	40	70	Ω
			V_{DD} = 14V	-	22	45	Ω
ON Resistance	R_{ON}	T_A = -40°C to 85°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V	V_{DD} = 5V	-	-	80	Ω
			V_{DD} = 14V	-	-	55	Ω
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V, V_{DD} = 14V		-	4	10	Ω
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = -40°C to 85°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V, V_{DD} = 14V		-	-	10	Ω
OFF-State Leakage Current	I_L	|VX - VY| = 14V		-	-	±10 (Note 3)	µA

Electrical Specifications

T_A = 25°C, V_{SS} = 0V, V_{DD} = 14V, C_L = 50pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CROSSPOINTS					
Switch I/O Capacitance	V_{IN} = 7V, f = 1MHz	-	20	-	pF
Switch Feedthrough Capacitance	V_{IN} = 7V, f = 1MHz	-	0.2	-	pF
Propagation Delay Time (Switch ON) Signal Input to Output, t_{PHL} or t_{PLH}		-	30	100	ns

Electrical Specifications $T_A = 25^oC$, $V_{SS} = 0V$, $V_{DD} = 14V$, $C_L = 50pF$, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response Channel ON f = 20log (VX/VY) = -3dB		$C_L = 3pF$, $R_L = 75\Omega$, $V_{IN} = 2V_{P-P}$	-	50	-	MHz
Total Harmonic, THD		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F_{DT}		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	-95	-	dB
Frequency for Signal Crosstalk, f_{CT} Attenuation of:	40dB	$V_{IN} = 2V_{P-P}$, $R_L = 75\Omega$	-	10	-	MHz
	110dB	$V_{IN} = 2V_{P-P}$, $R_L = 1k\Omega$ || 10pF	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output		Control Input = $3V_{P-P}$ Square Wave, $t_R = t_F = 10ns$ $R_{IN} = 1K$, $R_{OUT} = 10k\Omega$ || 10pF	-	75	-	mV_{PEAK}

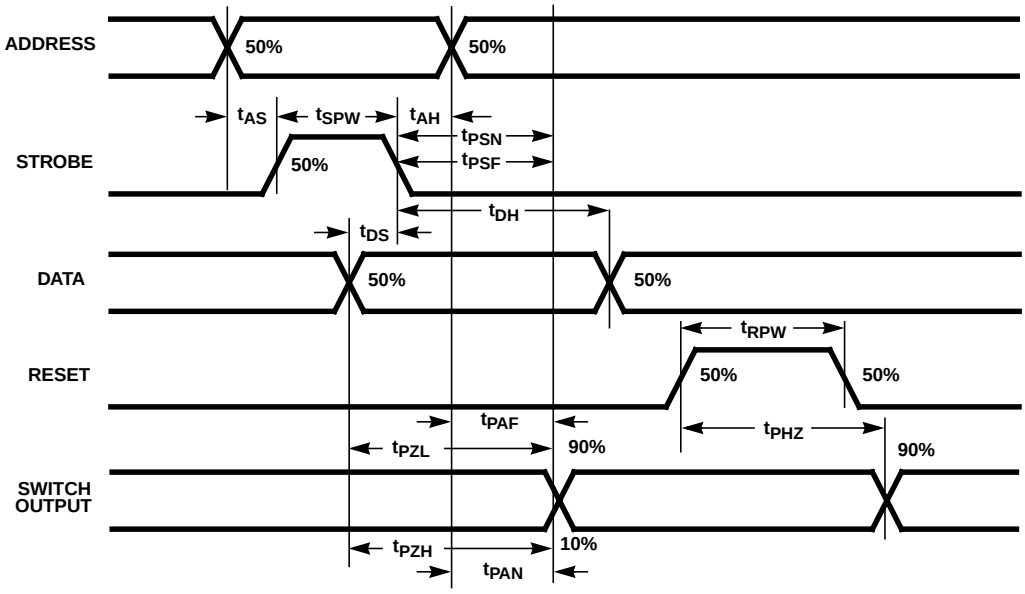
Electrical Specifications $T_A = 25^oC$, $V_{SS} = 0V$, $V_{DD} = 14V$, $R_L = 1k\Omega$ || 50pF, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CONTROLS						
Digital Input Capacitance	C_{IN}	$V_{IN} = 5V$, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output Switch Turn-ON	t_{PSN}		-	30	100	ns
Switch Turn-OFF	t_{PSF}		-	40	100	ns
DATA-IN to Output Turn-ON to High Level	t_{PZH}		-	30	100	ns
Turn-ON to Low Level	t_{PZL}		-	30	100	ns
ADDRESS to Output Turn-ON to High Level	t_{PAN}		-	30	100	ns
Turn-OFF to Low Level	t_{PAF}		-	25	100	ns
Setup Time DATA-IN to STROBE	t_{DS}		20	-	-	ns
ADDRESS to STROBE	t_{AS}		20	-	-	ns
Hold Time STROBE to DATA-IN	t_{DH}		20	-	-	ns
STROBE to ADDRESS	t_{AH}		10	-	-	ns
Pulse Width STROBE	t_{SPW}		30	-	-	ns
RESET	t_{RPW}		50	-	-	ns
RESET Turn-OFF to Output Delay	t_{PHZ}		-	100	200	ns

NOTES:

2. Reset $I_{IH} < 2mA$, Reset = $V_{DD} = 16V$.
3. At 25^oC Limit is ±100nA.

Timing Diagram



TRUTH TABLE X AXIS

X ADDRESS					
AX3	AX2	AX1	AX0	NOTE	X SWITCH
0	0	0	0		X0
0	0	0	1		X1
0	0	1	0		X2
0	0	1	1		X3
0	1	0	0		X4
0	1	0	1		X5
0	1	1	0	4	No Connect
0	1	1	1	4	No Connect
1	0	0	0		X6
1	0	0	1		X7
1	0	1	0		X8
1	0	1	1		X9
1	1	0	0		X10
1	1	0	1		X11
1	1	1	0	4	No Connect
1	1	1	1	4	No Connect

NOTE: 4. When X switch addresses are in these states, no change in status will occur in switches between any X and Y points.

TRUTH TABLE Y AXIS

Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an “X” address, a “Y” address, set “DATA” high, and switch “Strobe” from low to high. To break a connection, follow this same procedure with “DATA” low.:

Example:

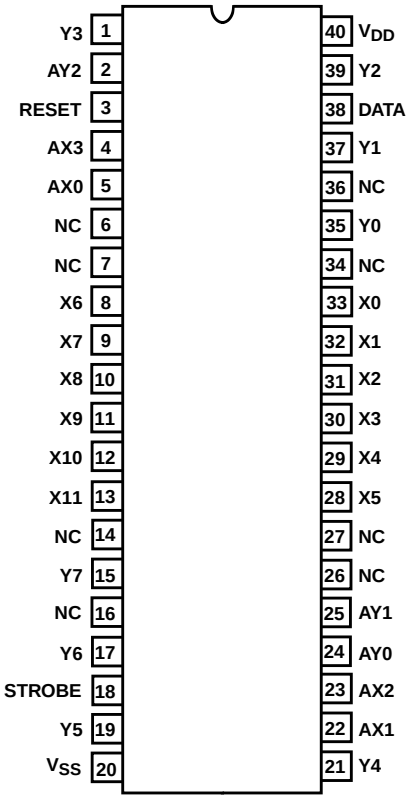
	DATA	X ADDRESS				Y ADDRESS		
		AX3	AX2	AX1	AX0	AY2	AY1	AY0
To connect switch X3 to switch Y4:	1	0	0	1	1	1	0	0
To connect switch X6 to switch Y7:	1	1	0	0	0	1	1	1
To break connection from X3 to Y4:	0	0	0	1	1	1	0	0

Pin Descriptions

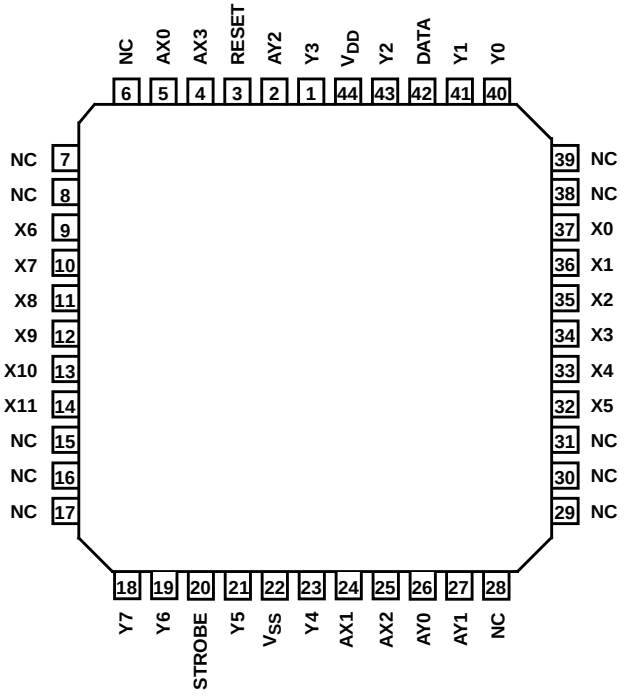
SYMBOL	40 LEAD PDIP PIN NO.	44 LEAD PLCC PIN NO.	DESCRIPTION
POWER SUPPLIES			
V_{DD}	40	44	Positive Supply
V_{SS}	20	22	Negative Supply
ADDRESS			
AX0 - AX3	5, 22, 23 and 4	5, 24, 25 and 4	X Address Lines. These pins select one of the 12 rows of switches. See the Truth Table for the valid addresses.
AY0 - AY2	24, 25 and 2	26, 27 and 2	Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.
CONTROL			
DATA	38	42	DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20	STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.
RESET	3	3	MASTER RESET. A high or one on this line opens all switches.
INPUTS/OUTPUTS			
X0 - X5 I/O X6 - X11	33 - 28 8 - 13	37 - 32 9 - 14	Analog or Digital Inputs/Outputs. These pins are the rows X0 - X11.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17 and 15	40, 41, 43, 1, 23, 21, 19 and 18	Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

Pinouts

CD22M3493 (PDIP)
TOP VIEW



CD22M3493 (PLCC)
TOP VIEW



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