FAIRCHILD SEMICONDUCTOR®

January 2003

FDZ208P

P-Channel 30 Volt PowerTrench® BGA MOSFET

General Description

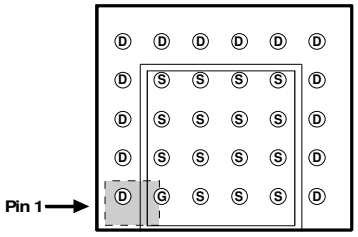
Combining Fairchild's advanced 30 Volt P-Channel Trench II Process with ± 25 Volts Vgs. Abs. Max Gate Rating for the ultimate low Rds Battery Protection MOSFET. This MOSFET also embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

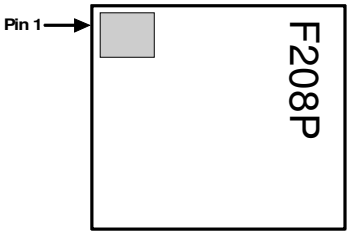
- Battery management
- Load switch
- Battery protection

Features

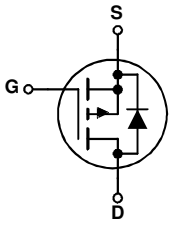
- –12.5 A, –30 V. $R_{DS(ON)}$ = 10.5 mΩ @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 16.5 mΩ @ V_{GS} = –4.5 V
- Occupies only 14 mm^2 of PCB area. Only 42% of the area of SO-8
- Ultra-thin package: less than 0.80 mm height when mounted to PCB
- 3.5 x 4 mm^2 footprint
- High power and current handling capability



Bottom



Top



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–30	V
V_{GSS}	Gate-Source Voltage		± 25	V
I_D	Drain Current – Continuous	(Note 1a)	–12.5	A
	– Pulsed		–60	
P_D	Power Dissipation (Steady State)	(Note 1a)	2.2	W
		(Note 1a)	1.0	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	56	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Ball	(Note 1)	4.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	0.6	°C/W

Package Marking and Ordering Information

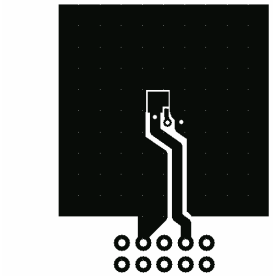
Device Marking	Device	Reel Size	Tape width	Quantity
208P	FDZ208P	7''	8mm	3000 units

Electrical Characteristics

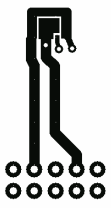
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V			–1	µA
I_{GSSF}	Gate–Body Leakage Current, Forward	V_{GS} = –25 V, V_{DS} = 0 V			–100	nA
I_{GSSR}	Gate–Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V			100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–1	–1.5	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –12.5 A V_{GS} = –4.5 V, I_D = –9.5 A V_{GS} = –10 V, I_D = –12.5A, T_J=125°C		9 13 11.7	10.5 16.5 15	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–30			A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –12.5 A		40		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz		2409		pF
C_{oss}	Output Capacitance			614		pF
C_{rss}	Reverse Transfer Capacitance			300		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		13	24	ns
t_r	Turn–On Rise Time			11	21	ns
$t_{d(off)}$	Turn–Off Delay Time			74	119	ns
t_f	Turn–Off Fall Time			42	68	ns
Q_g	Total Gate Charge	V_{DS} = –15 V, I_D = –12.5 A, V_{GS} = –5 V		25	35	nC
Q_{gs}	Gate–Source Charge			5		nC
Q_{gd}	Gate–Drain Charge			10		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.8	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.8 A (Note 2)		–0.7	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 12.5 A, d_{iF}/d_t = 100 A/µs		29.5		nS
Q_{rr}	Diode Reverse Recovery Charge			30.2		nC

Notes: 1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 56°C/W when mounted on a 1in² pad of 2 oz copper

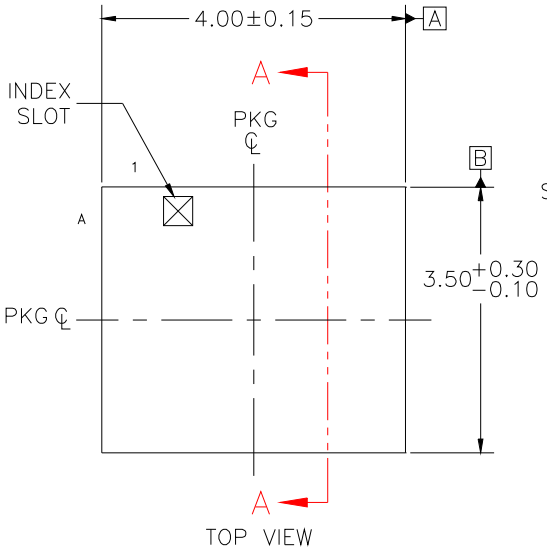


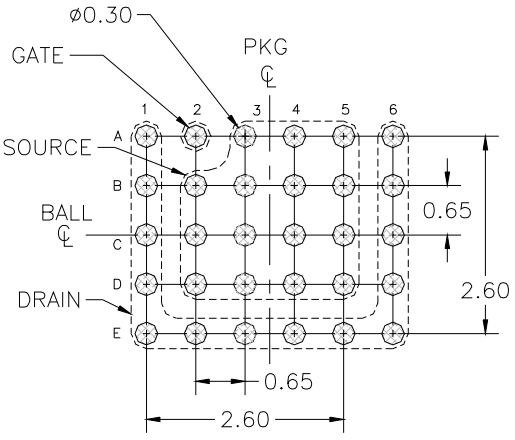
b) 119°C/W when mounted on a minimum pad of 2 oz copper

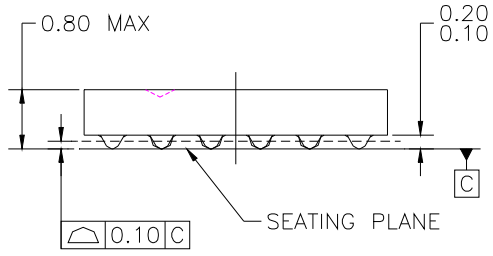
Scale 1 : 1 on letter size paper

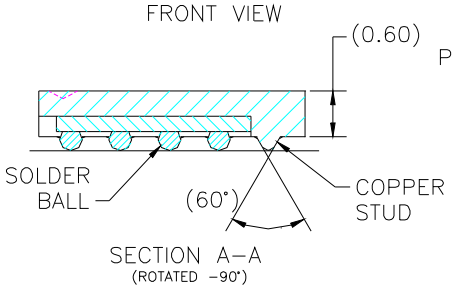
2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

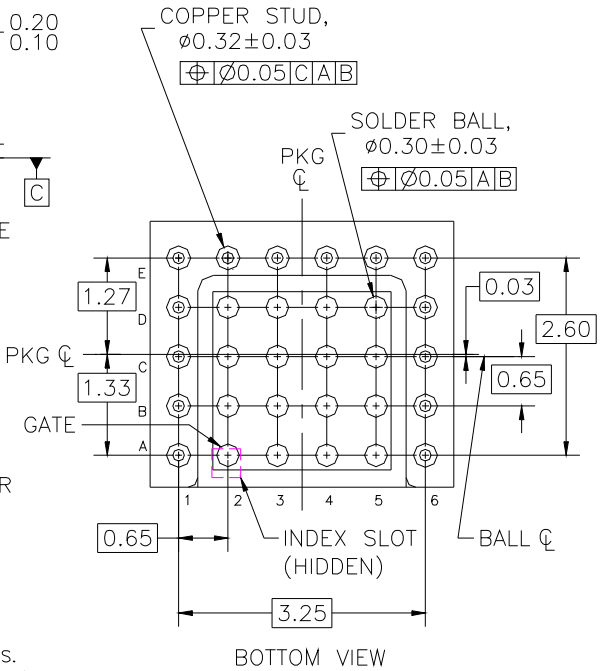
Dimensional Outline and Pad Layout











NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.

C) TERMINAL CONFIGURATION TABLE

POSITION	DESIGNATION	TYPE
A1,B1,C1,D1,E1, E2,E3,E4,E5,E6, D6,C6,B6,A6	DRAIN	COPPER STUD
A2	GATE	SOLDER BALL
A3,A4,A5,B2,B3, B4,B5,C2,C3,C4, C5,D2,D3,D4,D5,	SOURCE	

BGA16AREVC

Typical Characteristics

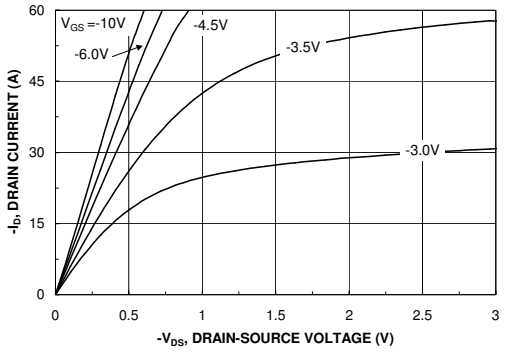


Figure 1. On-Region Characteristics.

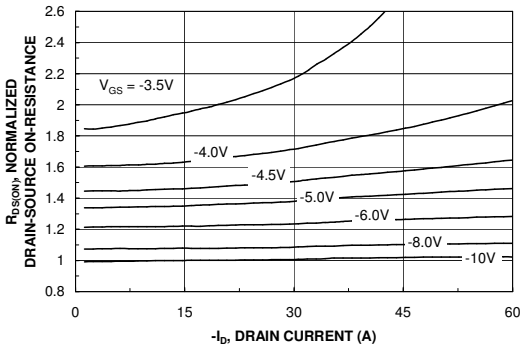


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

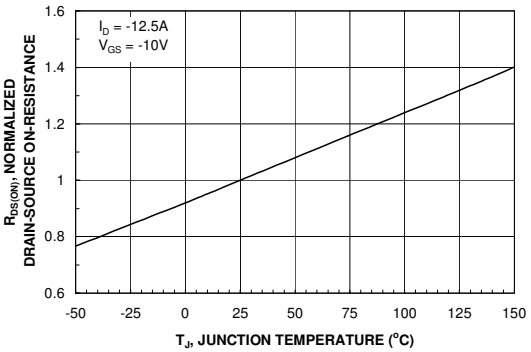


Figure 3. On-Resistance Variation with Temperature.

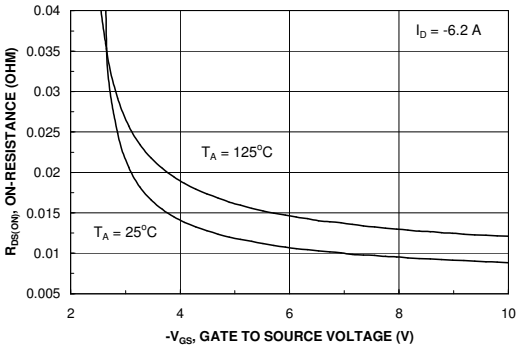


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

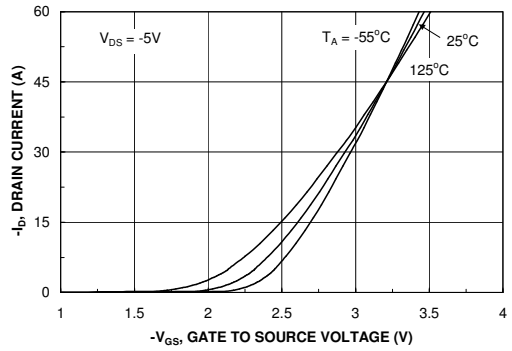


Figure 5. Transfer Characteristics.

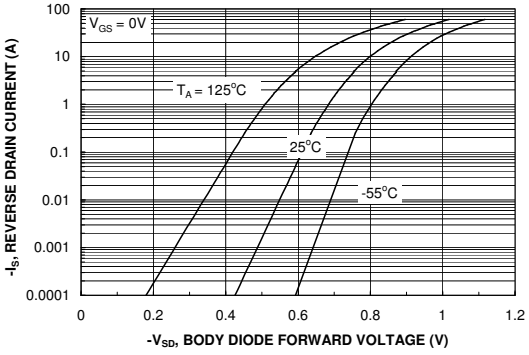


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

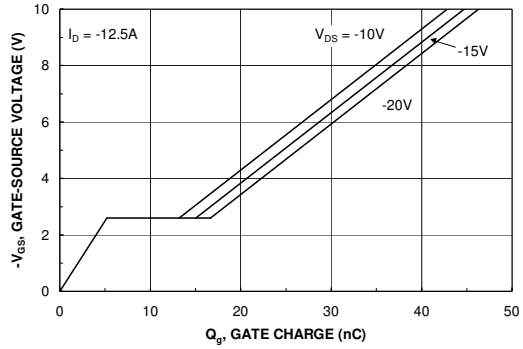


Figure 7. Gate Charge Characteristics.

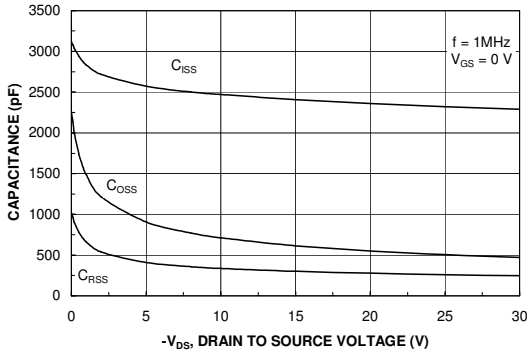


Figure 8. Capacitance Characteristics.

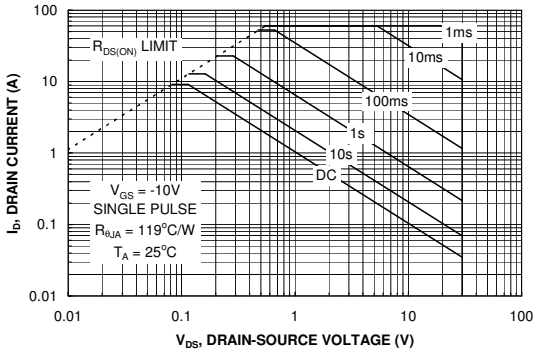


Figure 9. Maximum Safe Operating Area.

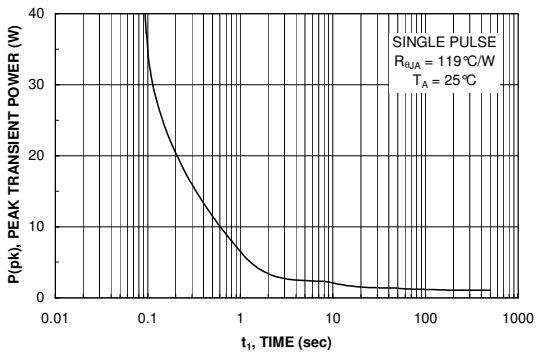


Figure 10. Single Pulse Maximum Power Dissipation.

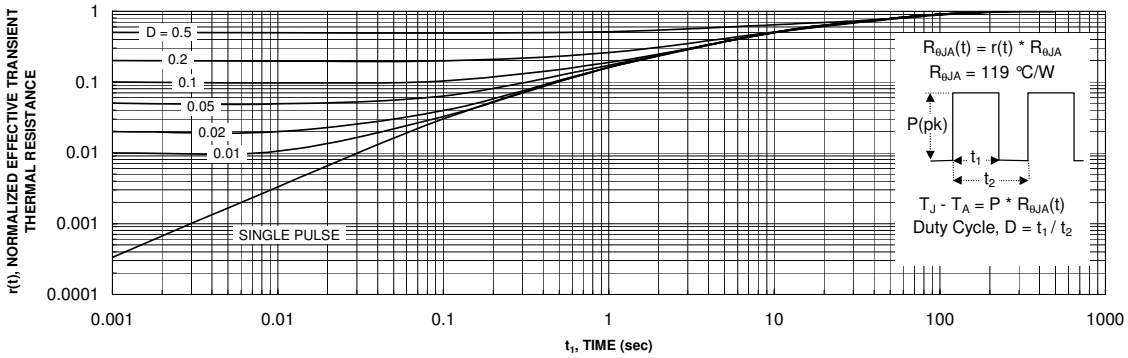


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E^2CMOS^{TM}	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
$EnSigna^{TM}$	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.