
2SJ319(L), 2SJ319(S)

Silicon P-Channel MOS FET

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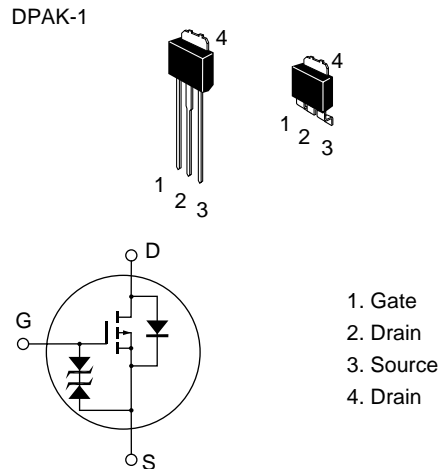
Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter

Outline



2SJ319(L), 2SJ319(S)

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---------------------|-------------|------|
| Drain to source voltage | V_{DSS} | -200 | V |
| Gate to source voltage | V_{GSS} | ±20 | V |
| Drain current | I_D | -3 | A |
| Drain peak current | $I_{D(pulse)}^{*1}$ | -12 | A |
| Body to drain diode reverse drain current | I_{DR} | -3 | A |
| Channel dissipation | Pch^{*2} | 20 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

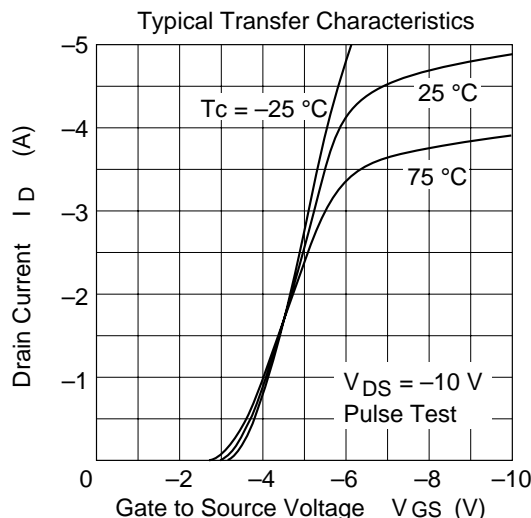
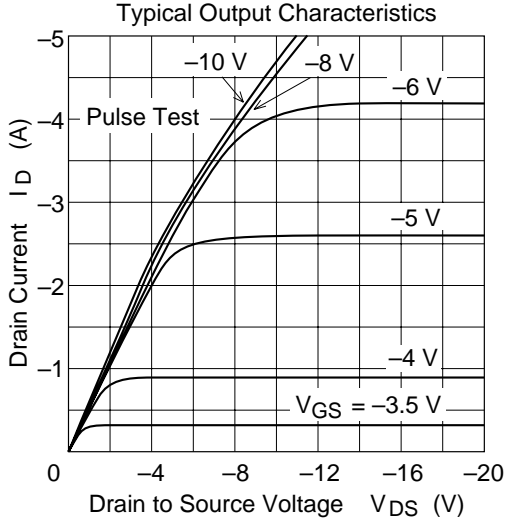
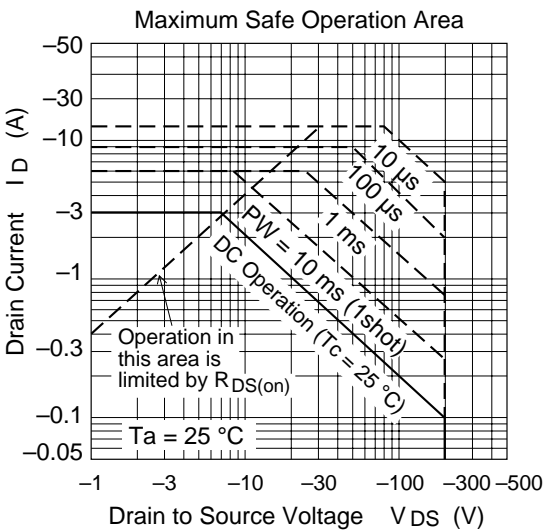
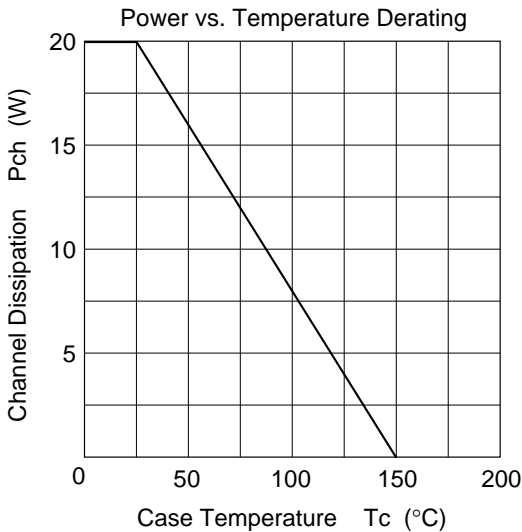
Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at $T_C = 25^\circ C$

Electrical Characteristics (Ta = 25°C)

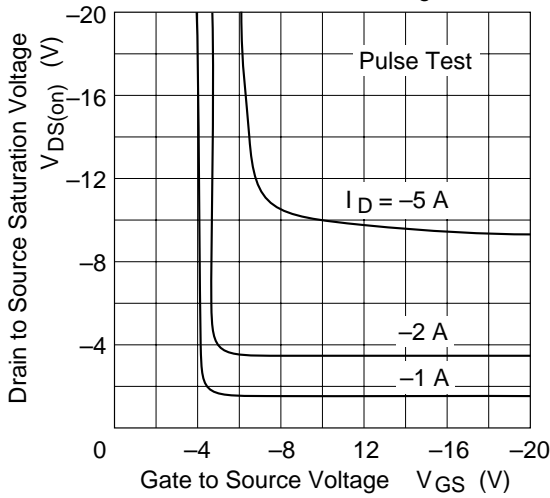
| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|------|-------|------|------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | -200 | — | — | V | $I_D = -10 \text{ mA}$, $V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±20 | — | — | V | $I_G = \pm 100 \mu A$, $V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ±10 | μA | $V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | -100 | μA | $V_{DS} = -160 \text{ V}$, $V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | -2.0 | — | -4.0 | V | $I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 1.7 | 2.3 | Ω | $I_D = -2 \text{ A}$, $V_{GS} = -10 \text{ V}^{*1}$ |
| Forward transfer admittance | $ y_{fs} $ | 1.0 | 1.7 | — | S | $I_D = -2 \text{ A}$, $V_{DS} = -10 \text{ V}^{*1}$ |
| Input capacitance | Ciss | — | 330 | — | pF | $V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, |
| Output capacitance | Coss | — | 130 | — | pF | $f = 1 \text{ MHz}$ |
| Reverse transfer capacitance | Crss | — | 25 | — | pF | |
| Turn-on delay time | $t_{d(on)}$ | — | 10 | — | ns | $I_D = -2 \text{ A}$, $V_{GS} = -10 \text{ V}$, |
| Rise time | t_r | — | 30 | — | ns | $R_L = 15 \Omega$ |
| Turn-off delay time | $t_{d(off)}$ | — | 40 | — | ns | |
| Fall time | t_f | — | 30 | — | ns | |
| Body to drain diode forward voltage | V_{DF} | — | -1.15 | — | V | $I_F = -3 \text{ A}$, $V_{GS} = 0$ |
| Body to drain diode reverse recovery time | t_{rr} | — | 180 | — | ns | $I_F = -3 \text{ A}$, $V_{GS} = 0$, $di_F/dt = 50 \text{ A}/\mu s$ |

Note: 1. Pulse test

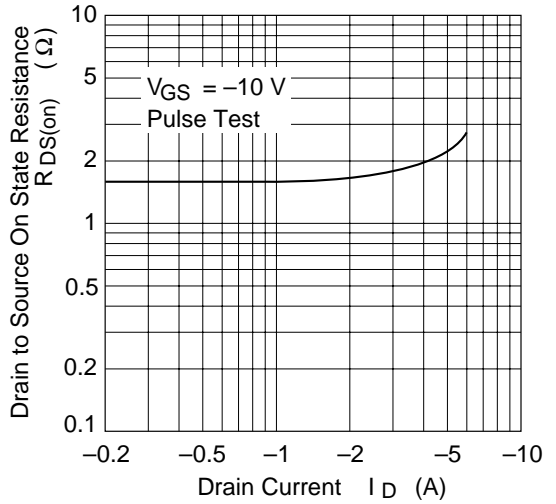
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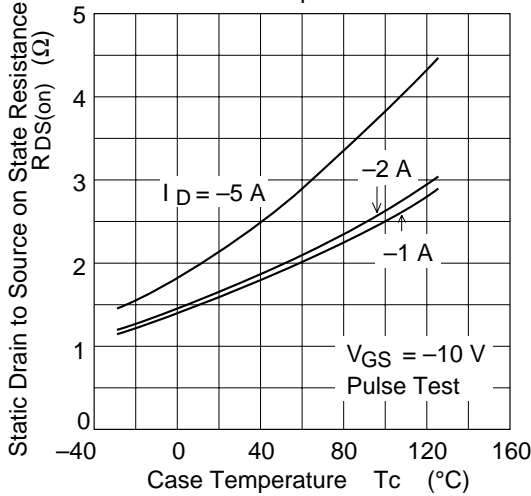
Drain to Source Saturation Voltage vs. Gate to Source Voltage



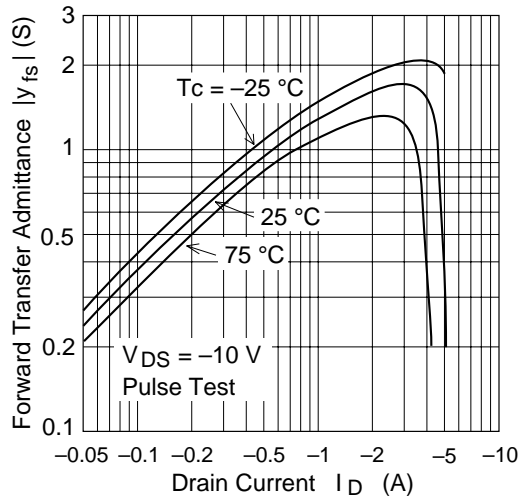
Static Drain to Source on State Resistance vs. Drain Current

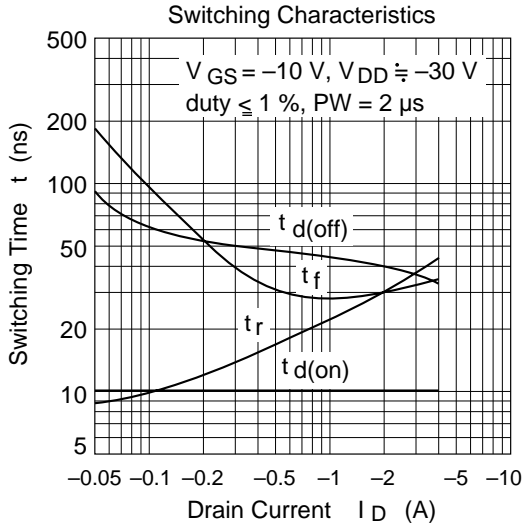
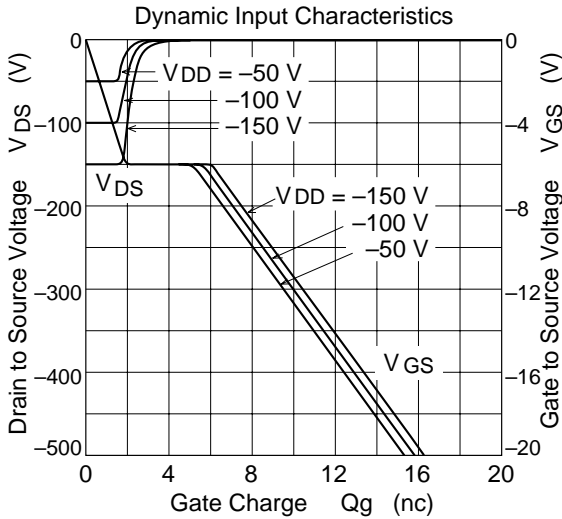
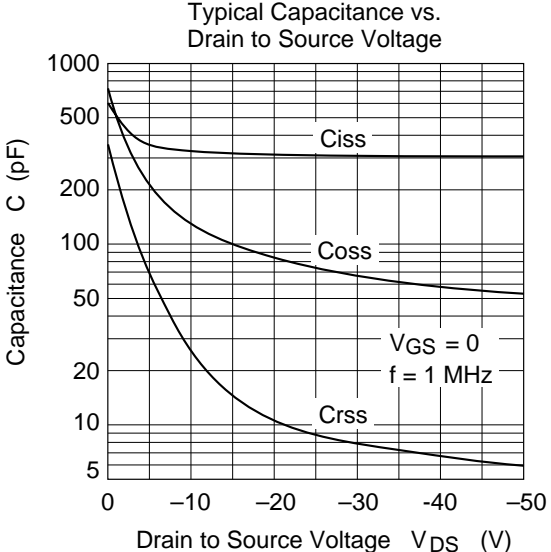
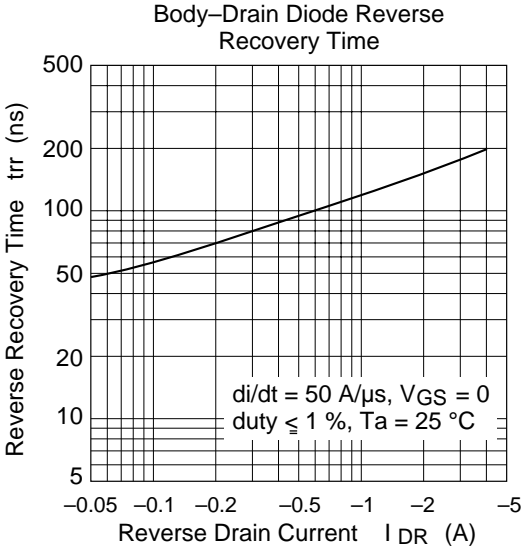


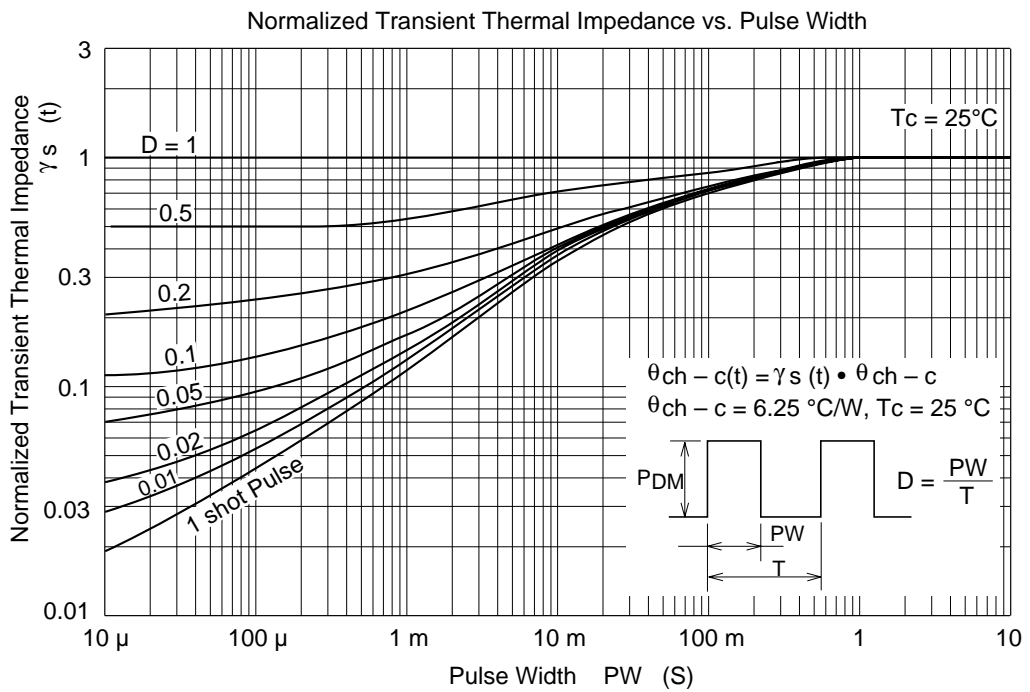
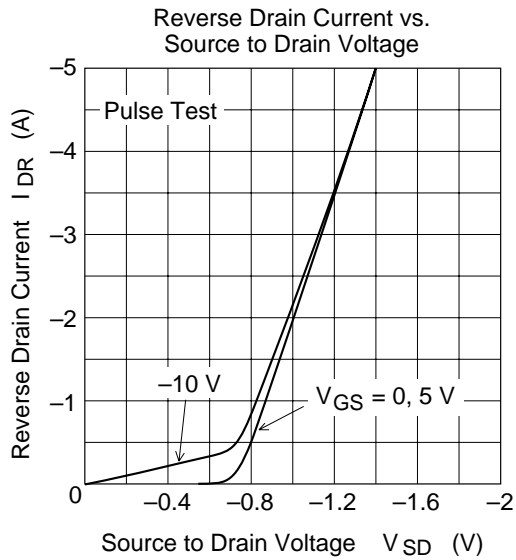
Static Drain to Source on State Resistance vs. Temperature



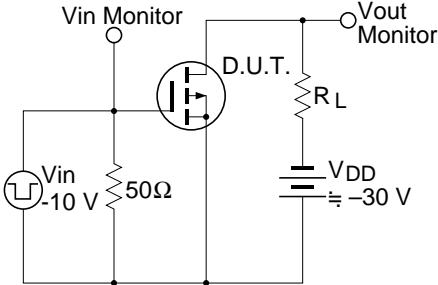
Forward Transfer Admittance vs. Drain Current



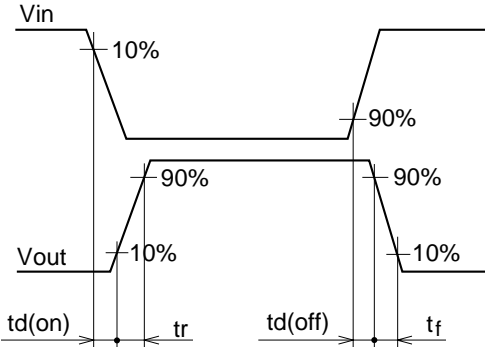


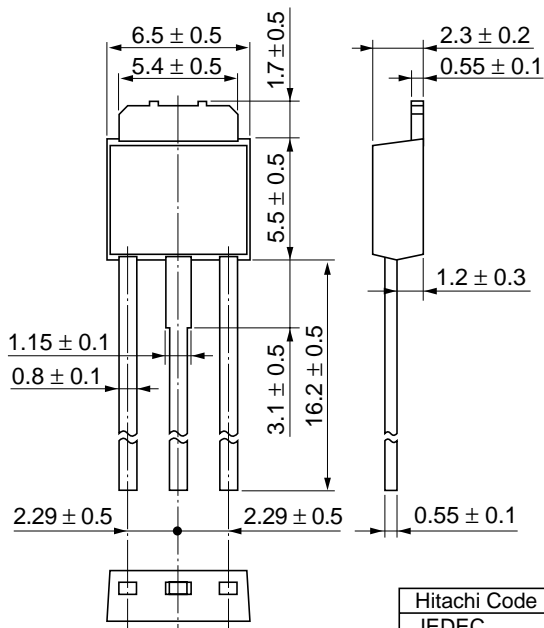


Switching Time Test Circuit



Waveforms





| | |
|--------------------------|--------------|
| Hitachi Code | DPAK (L)-(1) |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.42 g |

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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