

# 2SJ278

Silicon P-Channel MOS FET

# HITACHI

## Application

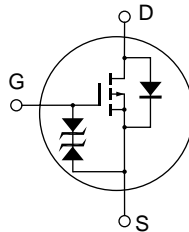
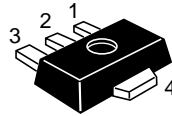
High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for switching regulator, DC-DC converter

## Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

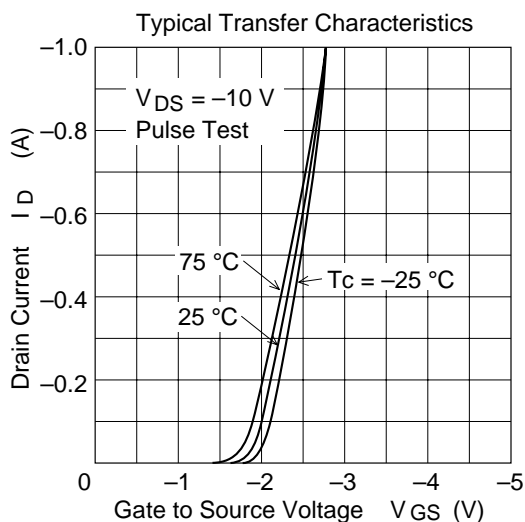
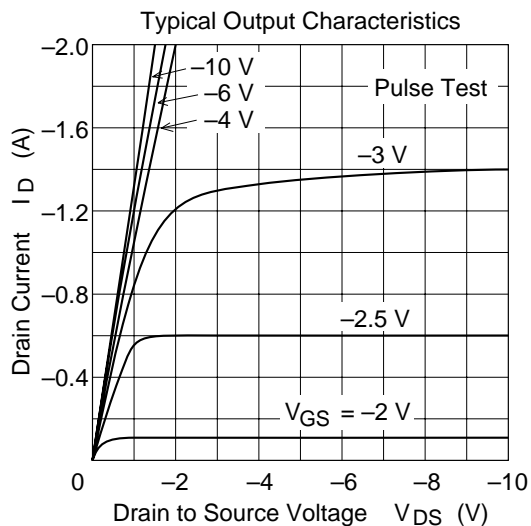
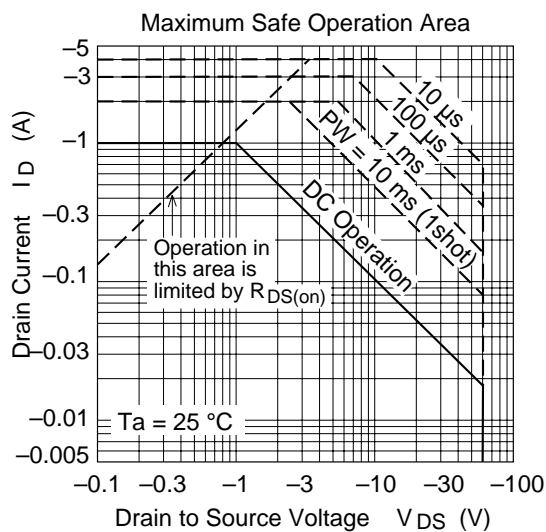
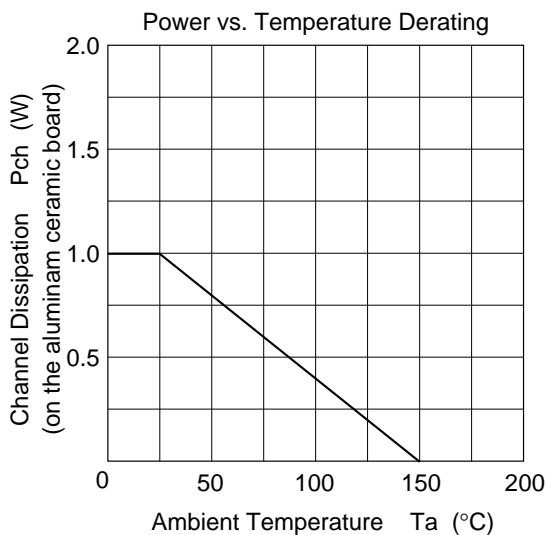
## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rated	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-1	A
Drain peak current	$I_{D(pulse)}^{*1}$	-4	A
Body to drain diode reverse drain current	$I_{DR}$	-1	A
Channel dissipation	$Pch^{*2}$	1	W
Channel temperature	$Tch$	150	°C
Storage temperature	$Tstg$	-55 to +150	°C

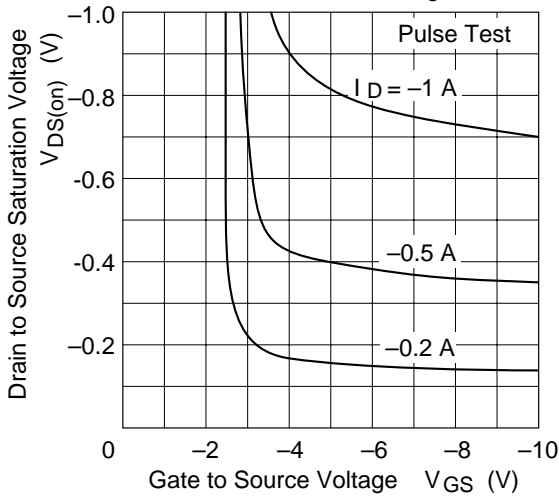
- Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
 2. Value on the alumina ceramic board (12.5×20×0.7 mm)  
 3. Marking is "MY".

## Electrical Characteristics (Ta = 25°C)

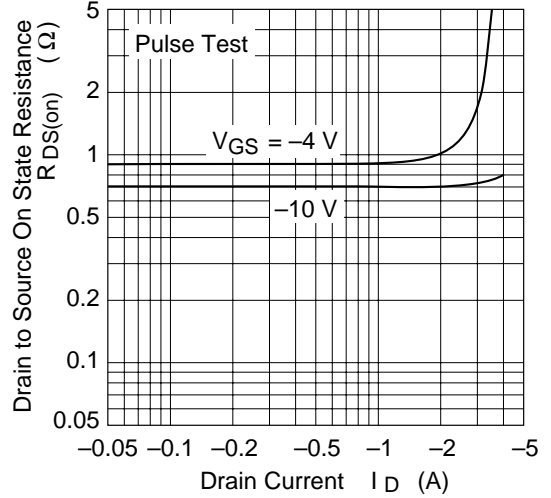
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	μA	$V_{DS} = -50 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.25	V	$I_D = -1 \text{ mA}$ , $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.83	Ω	$I_D = -0.5 \text{ A}$ , $V_{GS} = -10 \text{ V}^{*1}$
		—	0.9	1.2	Ω	$I_D = -0.5 \text{ A}$ , $V_{GS} = -4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	0.6	1.0	—	S	$I_D = -0.5 \text{ A}$ , $V_{DS} = -10 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	160	—	pF	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0$ ,
Output capacitance	$C_{oss}$	—	80	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	—	28	—	pF	
Turn-on delay time	$t_{d(on)}$	—	7	—	ns	$I_D = -0.5 \text{ A}$ , $V_{GS} = -10 \text{ V}$ ,
Rise time	$t_r$	—	8	—	ns	$R_L = 60 \Omega$
Turn-off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	$t_f$	—	25	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	-1.1	—	V	$I_F = -1 \text{ A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	90	—	ns	$I_F = -1 \text{ A}$ , $V_{GS} = 0$ , $di_F/dt = 50 \text{ A}/\mu s$



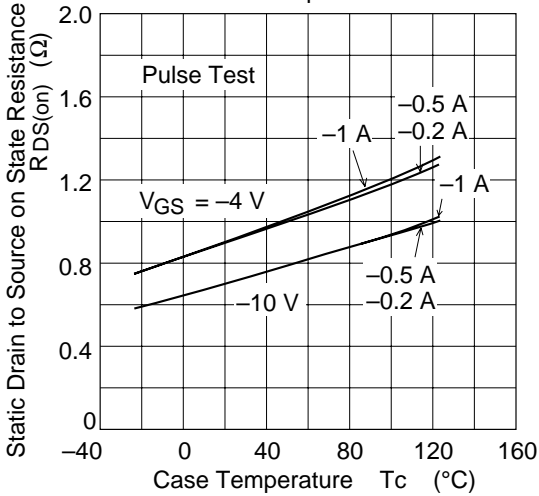
Drain to Source Saturation Voltage vs. Gate to Source Voltage



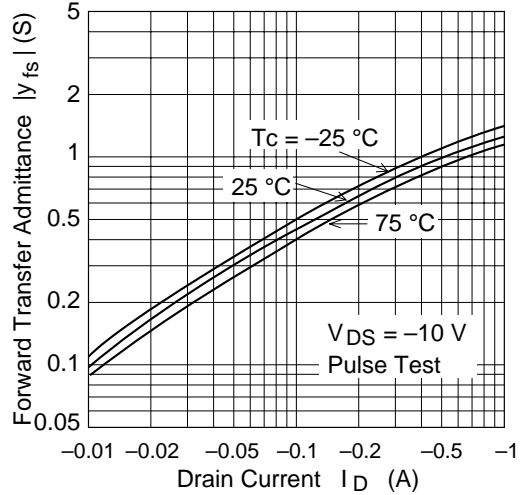
Static Drain to Source on State Resistance vs. Drain Current

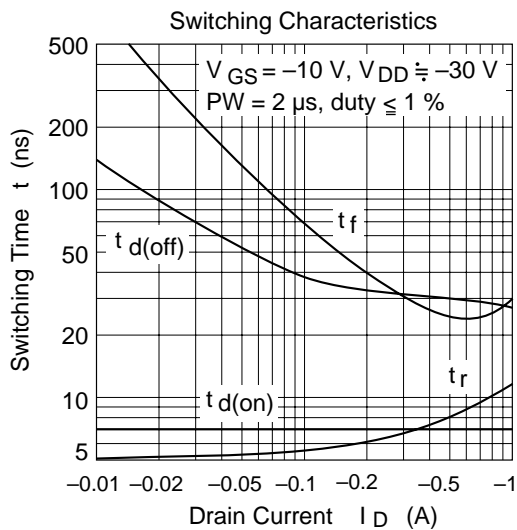
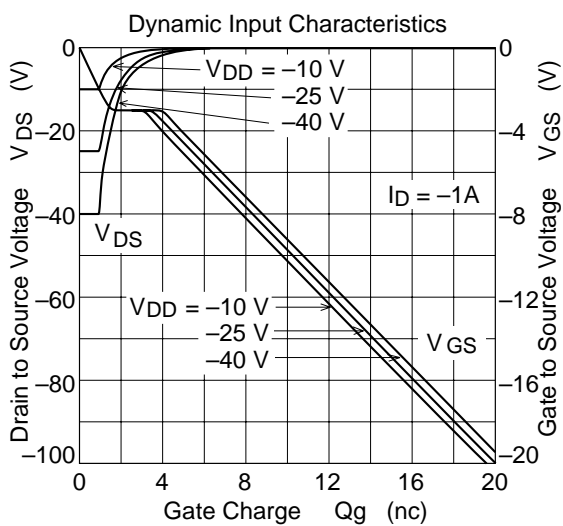
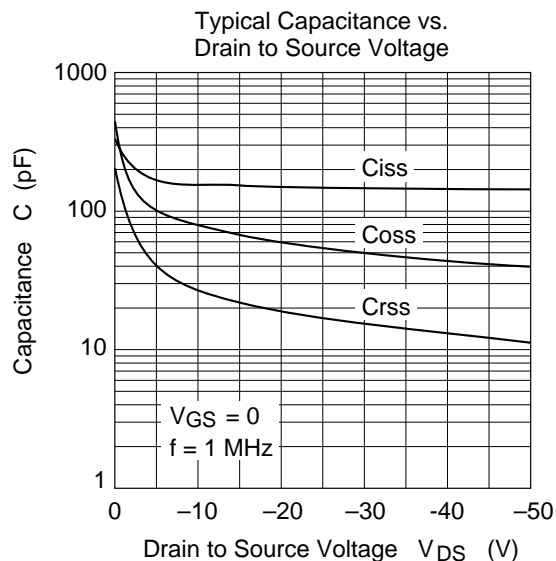
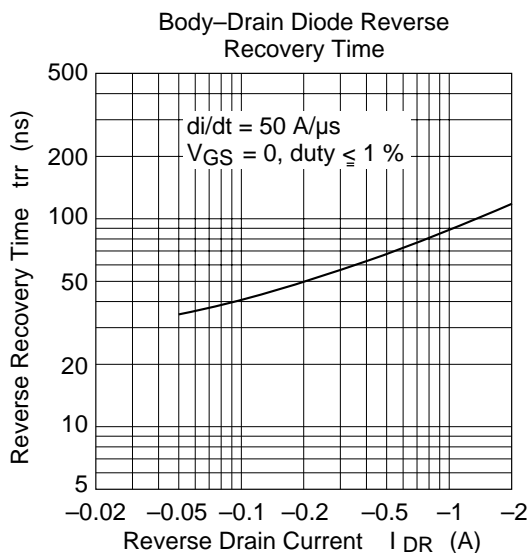


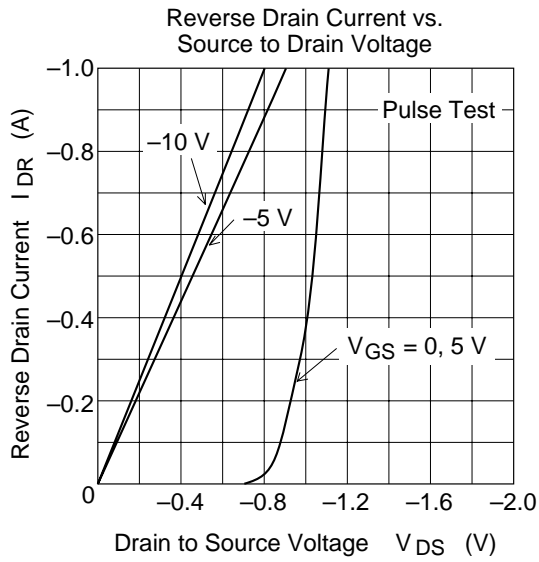
Static Drain to Source on State Resistance vs. Temperature



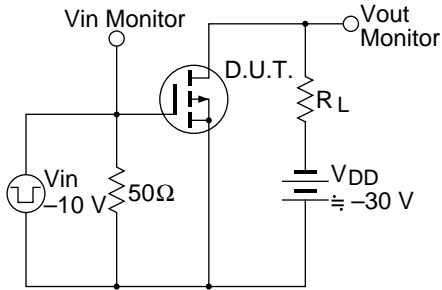
Forward Transfer Admittance vs. Drain Current



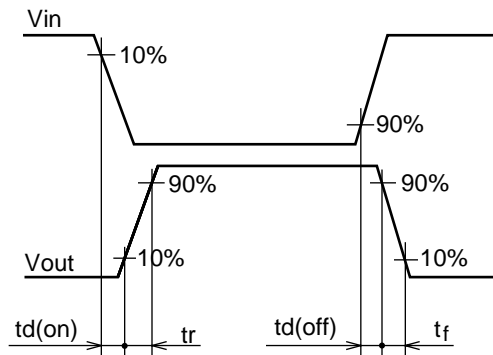


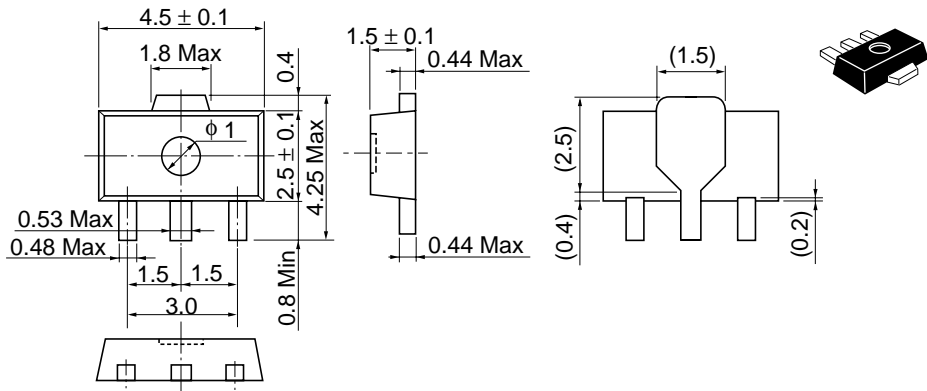


Switching Time Test Circuit



Waveforms





Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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